

A Novel QCA based Compact Scan Flip-flop for Digital Design Testing

Harshitha S., Dhanush T.N., Premananda B.S.



Abstract: Quantum-dot Cellular Automata (QCA) is an emerging technology used for computation at nano scale. It is an excellent alternative for the conventional CMOS technology. QCA provides us with low energy, high speed, faster switching speed and compact structures for logical circuits. Testing is the integral part of the design verification, scan flip-flop is used for device testing. It is used in processors for a built-in self-test. The objective of this paper is to design an optimized structure of a scan flip-flop which occupies less area and dissipates minimum energy compared to the previously designed architectures. The efficiency of the proposed structure is analyzed in terms of cell count, energy dissipation, and area occupied by the logical circuit. Proposed scan flip flop has a cell count of 32 and an energy dissipation of 0.0105 eV which is 20 % more efficient in terms of cell count and 29 % more efficient than the previous designs. The CAD tool, QCADesigner is used for design and simulation. Cells have a dimension of 18 nm in height and 18 nm in breadth and there is a distance of 2 nm between these cells. Bi-stable and coherence vector simulation engines are used in the tool for simulation.

Keywords: D Flip-flop, Multiplexer, QCA, Scan Flip-flop

I. INTRODUCTION

Moore's law states that the number of transistors which can be integrated on a single die doubles every two years. This law has been implemented since 1965 and has dictated the standards for manufacture of integrated circuits. Research indicates that the CMOS transistor could hit physical scaling limits which could be a hindrance to the process of aggressive packing of devices [1]. Breakthroughs in modern studies have significantly depicted that molecular transistors are a suitable choice in the near future. The creation of nanoscale devices which are highly compact and is capable of performing computational operations at a very high switching speed led to the development of Quantum Cellular Automata (QCA) [2]. Hence, QCA is the best alternative available for CMOS technology. The present CMOS based architecture consumes high power which inhibits energy efficient realization of complex circuits at nanoscale [3]. Hence, for attaining a higher computational power and for

obtaining a dense circuit, QCA is the best alternative available. The QCA cells cause shrinking of interconnects between the cells, which further increases the density of the device. Various logical operations can be realized in QCA which moves the data across cells using coulombic interactions [4]. It is based on encoding the binary information in the charge configuration within quantum dot cells [11]. QCA provides us with a unique technique of computation and data transformation. The two main components of QCA are Quantum-dot, which are nanotechnology structures made of semiconductors such as GaAs and Cellular automata, which is capable of self-reproduction because of the coulombic force of attraction present between the QCA cells.

Scan flip-flop consists of a D flip-flop and a multiplexer. A scan flip-flop is widely used for the purpose of built in self-test. It can be used to scan the internal chip of the processor and sense the existing fault before fabrication so that it can be rectified. This rectification of fault before fabrication will help us to reduce time and cost. A scan flip-flop has a wide range of application in device testing. Designing an optimized circuit with lesser of cell count will result in a decrease in the amount of energy dissipated, area occupied and further increases the processing speed.

Few of the recent low power technologies include Reversible logic, Adiabatic logic, and Quantum-dot Cellular Automata (QCA) technology. Reversible logic circuits must have one-to-one mapping between input vectors and output vectors; thus, the vector of output states can always be used to reconstruct the vector of input states. Limitation of reversible logic is that pre-defined reversible logic gates have to be created before implementation of actual circuits, which is both time consuming and critical for the design. Adiabatic circuits reduce power, but occupy large area and delay is also a critical factor and hence to overcome these problems QCA advantages have been discussed. Some of the adiabatic designs have been discussed in [7]

The paper proposes design and analysis of scan flip-flop. It is designed using an optimized structure of 2:1 multiplexer along with the D flip-flop. The aim is to reduce the number of cells in the circuit which further reduces the area required and energy dissipated by the circuit. The proposed QCA designs were designed and simulated using tool QCADesigner-E.

The rest of the paper is organized as follows, Section II describes the literature review in which different papers were analysed and the particular topics are discussed accordingly. Section III describes the QCA technology that is being used to design scan flip-flop at nanoscale level. Section IV discusses QCA logic and the components of scan flip-flop are discussed in section V. Section VI discusses the design of Scan flip-flop.

Revised Manuscript Received on October 30, 2019.

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Finally, the conclusion is presented in Section VII.

II. LITERATURE REVIEW

CMOS technology has always been a standard for industries to realize VLSI devices for the previous couple of decades because of its advantages such as miniaturization of devices with improved switching speeds, increased complexity and decreased consumption of power [1]. QCA is one amongst the most effective technologies planned as a replacement for CMOS technology in the coming future. QCA resolves most of the constraints levied by CMOS technology. QCA design provides us with lower energy dissipation and a higher processing speed at nano level. But one of the limitations of QCA is that, according to a research, the switching time of a QCA cell is at its finest in the order of few THz. Nevertheless, the actual speed might be lower. QCA circuit design has been extensively studied in recent years. However, there is no circuit design that exists for QCA. The presence of four clocks in place of a single clock which is used in CMOS urges the need for a set of concrete design rules. Unlike traditional CMOS technology, clock is required for sequential as well as combinational circuit in QCA. The clocking techniques and design of majority gates, binary wire and inverters are discussed in [1].

Three input coplanar majority gate and inverter structures were discussed in [1]. This design is further extended to realize a 2:1 multiplexer and its latency, area and energy dissipation parameters are discussed. The multiplexer architectures in [1] and [3] are improved using the same coplanar approach. The designs previously discussed were not efficient enough and hence it was improved by reducing the cell count which in turn reduced area and energy dissipated. Instead of using a coplanar cross wire of 45 or 90 degree we have chosen the conventional 180° cross wire.

The conventional D flip-flop architecture was referred having 30 cells in [3], 19 cells in [4] and 21 cells in [6]. These complex architectures were found to be inefficient when implemented on a large scale. This complexity was reduced by implementing a D flip-flop using the above mentioned optimized 2:1 Multiplexer. As a result, the cell count is further reduced. The realization of a compact JK flip-flop is mentioned in [12], but the implementation of scan flip-flop with a compact design of D flip-flop is considered to be more efficient.

A scan flip-flop can be constructed using the designed structures of 2:1 multiplexer and D flip-flop. QCA has its application at the nanoscale level. Thus, by integrating them, implementation at nano scale level can be achieved. The designed architecture is compared with the architecture in [3] which consists of 72 cells and the architecture in [6] which consists of 40 cells. The existing architecture is of lesser efficiency in terms of speed and energy consumption. This issue can be addressed by implementing our own architecture which is of greater efficiency when compared with the existing design.

III. QCA TECHNOLOGY

A. Quantum Dot

A single component known as a quantum cell is employed for designing all the components present in a circuit. The QCA cell comprises of four quantum dots situated within the corners of the cell and two active electrons [2]. The tunneling

junctions have potential barriers which are monitored by the locally induced electric fields that are elevated to prevent movement of the electron and lowered to support electron movement [5]. A secluded cell can have any one of the following three states. If the barriers are lowered and the mobile electrons are free to move onto any dot, it is said to be in null state. When the barrier is raised, it results in the formation of polarization state which serves to diminish the energy states of the cell. When $P = +1$, it denotes binary 1 and when $P = -1$, it denotes binary 0 [1]. The QCA cells are shown in Fig.1. The cells positioned close to each other are enforced into identical polarizations due to Coulombic interactions between the cells. Orientation of a quantum cell can be 90 degree or 45 degree based on the circuit design [1].

B. QCA Clocking

Clocking in QCA is not similar to the one used in CMOS and has an important role in monitoring the functioning of QCA logic. The clocking zones create an electric field which raises and lowers the potential barriers which allows the free electrons to flow through the cells. The computation takes place from current to the next in a successive order since the clocking zones are physically next to one another. They avoid non deterministic variations of QCA cells circuits. When compared to transistor-based circuits, the clocking in QCA has one clock cycle which comprises four clock signals, which are delayed by a clock signal among each other as shown in Fig. 2. A clocking scheme is adopted with four different phases known as switch, hold, release, and relaxes [4]. The clocking of QCA can be accomplished by controlling the potential barriers between neighboring quantum-dots.

During the initial phase known as the switch phase, the inter-dot barrier is gradually elevated which settles down the QCA cell and results in formation of either of the two ground polarization states as influenced by its neighboring cells [5]. In the second stage also known as hold phase, the inter-dot barrier is fixed at an elevated position which suppresses tunneling of electrons and maintains the present ground polarization condition of the QCA cell.

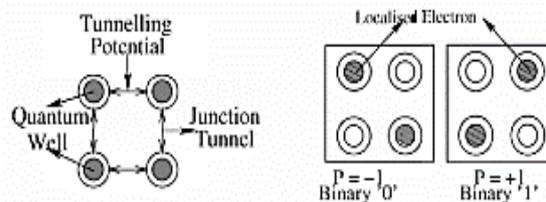


Fig. 1. QCA cell and its orientation [2]

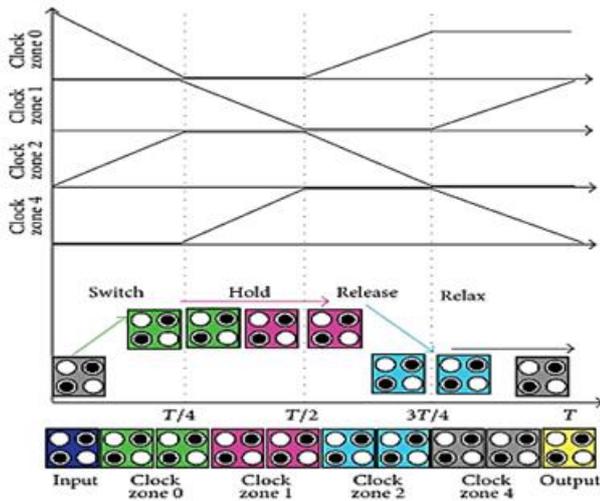


Fig. 2. QCA Clocking Zones [2]

The inter-dot barriers are lowered during the release and relax phases, subsequently the additional electrons in the cell get mobilized. During the last two phases, a QCA cell maintains an unpolarized state. Hence, a QCA cell's state is decided during its switch phase whereas the neighboring cells' polarization is determined during the switch phase and hold phase respectively. The adjacent unpolarized cells in their final phases do not affect the polarization of the cell [8]. The signals of the clock may be produced by the CMOS wires fixed underneath the QCA plane.

For proper functioning of the circuit, it is mandatory for the timing rules of QCA circuits to be obeyed. In the case of majority gates, the clocking zone of its output cell must be different than the rest of the cells which constitute the gate. For example, if the majority gate's output cells located in clocking zone 1, then the input cells are located in clocking zone 0. The least number of clocking zones has to be inculcated to obtain minimal circuit latency.

IV. QCA LOGIC

When two or more QCA cells are placed adjacently, a coulombic effect will be raised between the electrons due to harmonization of adjoining cells, which gives rise to alteration in the polarization of the adjacent cells. With QCA cells, primary logic gates can be implemented easily.

A. Majority Gate

A Majority gate is considered as a basic module in a QCA circuit. It comprises of 5QCA cells, 3 inputs and an output as depicted in Fig. 3. The gate's Boolean function is expressed as $M(X, Y, Z) = XY + YZ + XZ$, considering X, Y, Z as binary inputs and M to be a binary output by a majority gate. Here M denotes a majority function. The majority value of inputs X, Y and Z constitute the output of the majority gate [4]. The cells situated on the top, left and bottom position acts as input cells. The output cell adjusts to the intermediate cell which gives the output of the majority voter.

B. QCA Inverter

There two types of inverters that can be realized in QCA, a corner cell inverter and a robust inverter. The corner cell-based inverter consists of four QCA cells and a robust inverter consists of seven QCA cells as shown in Fig. 4. The

electrons in the QCA cells travel due to the repulsion caused by the Columbic forces and shifted cell will obtain the complement value of the previous cell. The cells positioned diagonal to each other tends to have opposite polarization due to repulsion between the electrons. Inversion can also be obtained by using 45° cells in which the neighboring cell will inherently have an inverted value of the data.

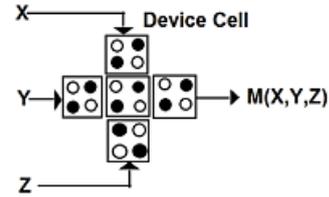


Fig. 3. Majority gate [4]

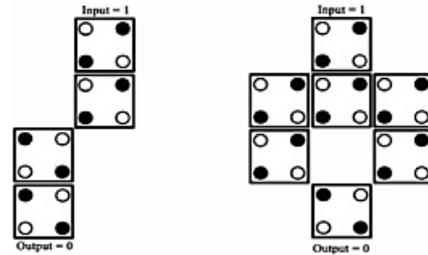


Fig. 4. QCA Inverters, Corner cell Inverter, and Robust inverter [13]

C. QCA Wire

A binary wire in QCA consists of a collection of cells in a single line to propagate the signal from one point to another point as shown in Fig.5. The cells are coupled to each other. The coulombic interaction helps in passing the logic values from one cell to another. Due to the electron repulsion between the cells, if the polarization of one cell changes, it enforces its neighbouring cell to change its state. The two types of binary wire orientations are 90° and 45° orientation which is shown in Fig. 5.

D. Wire Crossovers

The crossovers are a very integral part of the QCA design. As the number of cell usage increases in the integration of a digital circuit crossovers are used to decrease the complexity of the circuit. There are two methods adopted for crossing two wires in QCA. This includes Co-planar crossover and Multi-layer crossover. The Co-planar crossover is obtained by crossing a wire with an inverter chain. This crossing takes place in a single plane yet the two signals propagating through the cells will not affect each other. The second method, Multi-layer crossover employs multiple planes where each wire occupies a distinct plane given in [9].

V. COMPONENTS OF SCAN FLIP-FLOP

A scan flip flop is a sequential circuit which is formed as a result of cascading a D flip flop with a 2:1 Multiplexer. The design of these components of a scan flip flop is discussed in this section.



A. 2:1 Multiplexer

A multiplexer is a device which selects a signal and transmits it in a single output line. Multiplexers are for data transmission. In a 2:1 multiplexer, a single output is selected from the available 2 input signals [6]. To implement a multiplexer circuit, a logical AND gate and OR gate has to be designed using the majority gate circuit. If v and w are the two inputs, the select line helps in selecting v or was the output using the logic shown in Fig. 6.

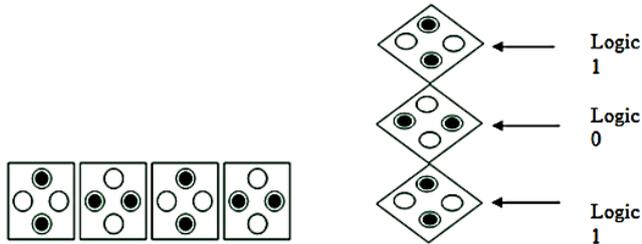


Fig. 5. QCA wires with 90° and 45° orientation [14].

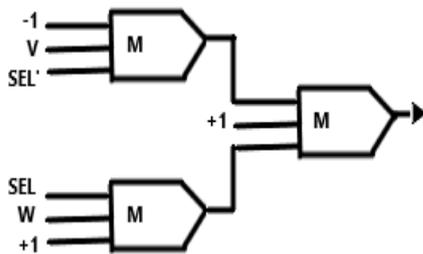


Fig. 6. 2:1 Multiplexer using majority gates [6]

The conventional approach of using two AND gates to multiply the input with the select line and an OR gate to add the outputs of the AND gate is implemented in the QCA design. In Fig. 7, I1 and I0 represent inputs and Sel represents select line in the designed 2:1 multiplexer whose output is represented by Y. The simulation result of the 2:1 multiplexer is shown in the Fig. 8 where the input signals I1 and I0 along with the select signal is mentioned and the expected output is obtained.

Table I, list the cell count, area, latency and energy dissipation of both previous architectures and the proposed architecture of 2:1 Multiplexer. It can be inferred from Table I that the proposed design is 39 % and 26 % more efficient in terms of cell count when compared with the designs proposed in [3] and [1] respectively. The energy dissipated is calculated using QCA Designer-E and the design implementation is done using QCA Designer 2.0.3. This efficiency in the proposed design is due to the removal of redundant cells. The designed multiplexer structure occupies least area of 0.0105 μm^2 and dissipates energy of amount 0.00902 eV. Hence, it is considered to be efficient when compared with the previously designed structures and can be used for constructing other modules.

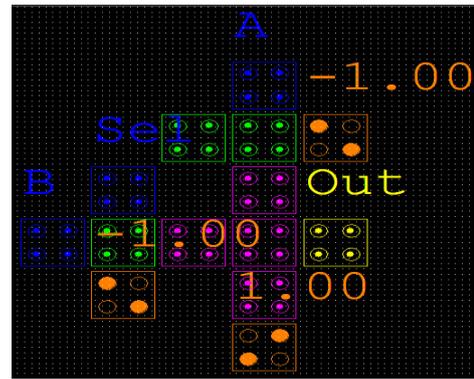


Fig. 7. QCA circuit of proposed of 2:1 multiplexer

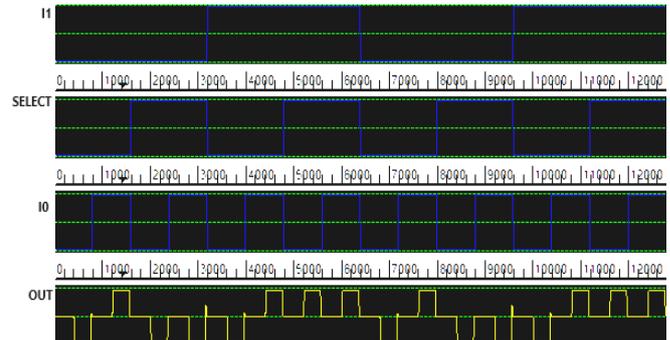


Fig. 8. Simulation results of 2:1 Multiplexer

Table I. Performance Analysis of 2:1 Multiplexer

2:1 Multiplexer	Cell Count	Area (μm^2)	Latency (clock cycle)	Energy Dissipation (eV)
[3]	23	0.04	2	0.0137
[1]	19	0.02	3	0.0151
[4]	18	0.017	2	0.0133
[5]	17	0.0217	2	0.0133
Proposed	14	0.0105	2	0.00902

B. D Flip-Flop

A flip-flop is a circuit that is used to store state information. A D flip-flop changes its state with respect to the input line when the clock is high. When the clock is kept at low, it holds the previous value. A SR flip-flop can be converted to a D flip-flop by tying the set to the reset through an inverter [10]. D flip-flop can be used to design shift registers, counters, memory, frequency dividers etc.

An optimized D flip-flop can be obtained from the proposed 2:1 multiplexer. The logic used in the QCA circuit is as shown in Fig. 9. The efficiency in the proposed design is due to removal of redundant cells and designs occupying less area. On incorporating the above design, the cell count decreases which further decreases the area occupied and the power dissipated by the circuit. In Fig. 10, C represents the clock, D is the data input and Out represents the output. The simulation results of the D flip flop are shown in the Fig. 11 where the input is given by D along with the clock signal CLK is mentioned and the expected output is obtained.

In Table II, the cell count, area, latency and energy dissipation of both previous architectures and the proposed architecture of D flip flop is listed. From Table II, it can be inferred to that the proposed design is 43 % and 35 % more efficient in terms of cell count when compared with the designs

proposed in [3] and [1] respectively.

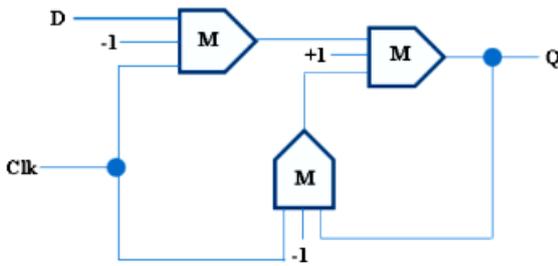


Fig. 9. Schematic of D Flip-flop in QCA [6]

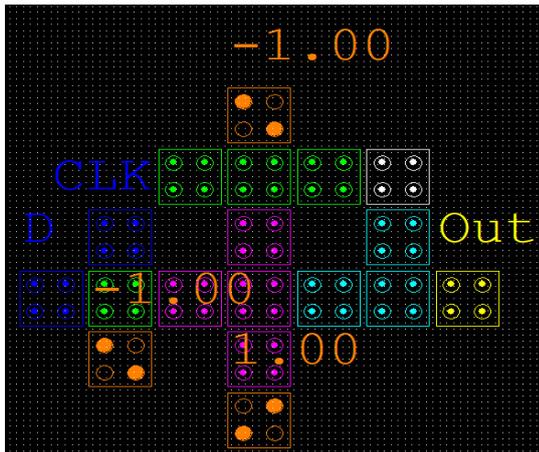


Fig. 10. QCA circuit of proposed D flip-flop.



Fig. 11. Simulation results of D Flip-flop

Table II. Performance analysis of D flip-flop

DFF	Cell Count	Area (μm^2)	Latency (clock cycles)	Energy Dissipation (eV)
[3]	30	0.03	4	0.0121
[1]	26	0.02	4	0.0133
[6]	21	0.024	4	0.01206
Proposed	17	0.0125	4	0.00598

The designed structure occupies the least area of 0.0125 μm^2 and dissipates energy of amount 0.00598 eV. Hence it is considered to be efficient when compared with the previously designed structures.

VI. DESIGN OF SCAN FLIP-FLOP

The main application of a scan flip-flop is to detect faults in a silicon chip. It is implemented in circuits to be tested. This in turn helps in reduction of time and cost as any fault detected can be rectified before fabrication. The main application of scan flip-flop is device testing. Scan flip-flop is a combination of a D flip-flop and a multiplexer where the multiplexer is positioned at the input where one

of the inputs of the multiplexer acts as a functional input D and the other input serves as the scan-in input. An enable pin is used to control the selection bit of the Multiplexer.

The proposed scan flip-flop is implemented using an optimized 2:1 Multiplexer and D flip-flop proposed in previous section. The Multiplexer is cascaded to the D flip-flop circuit to make it a scan flip-flop. The test data for the given circuit is loaded serially to observe the signal obtained at any specific node of the Circuit Under Test. The first mode of operation of a scan flip-flop is test mode in which the enable is set to high and the flip-flop is said to be in scan mode where test signal acts as the input to the flip-flop. The second mode of operation is the normal operation where enable is set to low and input data (D) acts as the flip-flop input.

The implementation of scan flip-flop is shown in Fig. 12 that consists of 32 cells. The inputs are represented as 'a', 'b' and 'sel'. The clock signal is given through the input pin 'Clk' and output pin is 'Out'. The simulation results of the Scan flip-flop are shown in the Fig. 13, where the input signals I1 and I0 along with the select signal is mentioned and the expected output is obtained. In Table III, performance analysis of scan flip-flop is shown where the cell count has been reduced from 72 to 40 in [6]. The proposed design has a better efficiency of 20 % when compared to the design in [6]. The proposed scan flip-flop structure has a cell count of 32 which decreased the area occupied by 29 % with respect to the design in [6].

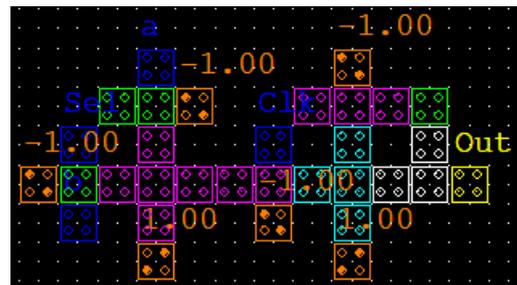


Fig. 12. Proposed QCA based Scan flip-flop

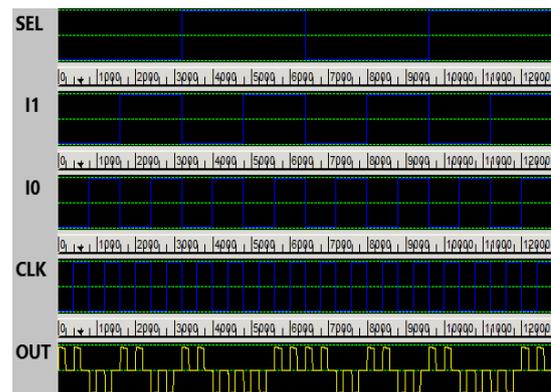


Fig. 13. Simulation result of proposed scan flip-flop

Table III. Performance analysis of scan flip-flop

SFF	Cell count	Area (µm ²)	Latency	Energy Dissipation (eV)
[3]	72	0.12	4	0.096
[6]	40	0.06	4	0.0188
Proposed	32	0.04	4	0.0105

VII. CONCLUSION

The designs proposed in this paper are designed using efficient design methodology where a 2:1 Multiplexer is used as a building block. QCA circuits such as latches, flip-flops and shift registers are realized and verified. The proposed 2:1 multiplexer is optimized and the cell count is reduced by 18 %, area is reduced by 49% and the energy dissipation is reduced by 32% when compared with the design in [5]. Similarly, the proposed D flip-flop has its cell count reduced by 19 %, area is reduced by 48 % and the energy dissipated is reduced by 51 % in comparison to the architecture in [6]. The proposed scan flip-flop architecture is reduced by 20 % in terms of cell count, the area is reduced by 33 % and the energy dissipation is reduced by 44 %. Thus, proposed scan flip-flop is efficient in terms of both cell count and energy dissipation. The proposed designs of 2:1 Multiplexer and D flip-flop along with an XOR gate and Shift register can be used to implement a compact pseudo random number generator.

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