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Nano Machine-based Hybrid 3D Network-on-Chip (NoC) using 18nm tsmc Technology

K.Balamurugan, R.Shijukumar

Abstract: Network-on-Chip paradigm is an emerging technology that provides communication between the Intellectual Property cores in System-on-Chip (SoC). The drastic development of nanotechnology supports the making of Intellectual property cores with small area, less power dissipation, improvement in latency and achieves high speed. The neural systems that emulate biological sensory capability on reconfigurable hardware are the key requirement in the field of Neuro-Engineering. Nano-neural connectivity technique is highly needed in order to implement reconfigurable Neural Networks (NNs) on-chip. This paper proposes a novel Nano Machine based Hybrid 3D Network-on-Chip for the emulation of a third-generation (3G) Neural Network model called Spiking Neural Network (SNN). This Hybrid Network-on-Chip uses a Nanomachine Transceiver with Carbon nanotube antenna which uses the novel pulse-based technique to transfer the packets between the subnet of NoC to reduce the latency. The experimental result of this work shows the improvement in latency of Nano machine-based NoC compared to the previously reported work for 18 nm TSMC technology.

***Keywords**: Network-on-Chip (NoC), System-on-Chip (SoC),CNT antenna, Wired Router, Wireless Router.*

I. INTRODUCTION

System-on-Chip (SoC) is a fast-growing technology in the chip manufacturing industry. In SoC, many numbers of Intellectual Property (IP) cores are integrated into a chip. The IP cores inside the chip are same or different. This SoCs are used as a very high-speed computing system,but power consumption is a major problem. Network-on-Chip (NoC) is a fast-growing technology for data communication in multicore SoC. In NoC, packets are transferred from one IP core to the other instead of sending signals to achieve high speed. The neurons and its connectivity show that routing of information around the brain. The software and hardware models can be analyzed using neural network techniques.The recent technology in neural network for the computation of neuron model is known as Spiking Neural Networks (SNNs)[1].

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* Correspondence Author
Dr.K.Balamurugan*, Professor, Electronics and Communication Engineering at Swarnandhra College of Engineering and Technology, Narsapur, Andhra Pradesh,India.Email: bala237115@gmail.com
R.Shijukumar, Senior R&D Engineer, Firmtech, Thiruvanathanpuram, Kerala, India. Email: r.shijukumar@gmail.com

This work explores the replication of conventional neural networks inside a single SoC called Neural Network System-on-Chip (NNSoC). The neuron interconnect system in Neural Networks (NNs) is similar to the on-chip communication system of NNSoC. The NNSoC architecture consists of spiking neuron models as Processing Element (PE) attached with the NoC routers and the channels are analogues to the synapses of neurons. The topology of NoC depends on the interconnection of neurons across the network [2] and the number of neurons can be assigned to each processor. Whereas, the transfer of spike between the neurons is considered as the transfer of packets between the IP cores over the interconnect. In this work, a Nano Machine based Hybrid NoC transceiver is designed by taking the advantages of both wired, and wireless communication and simulated using Hamster VHDL-AMS software. The comparison between wired router, wireless router and the hybrid router is done for various number of routers and the latency is calculated. In the other part of the work, the performance of the CNT antenna is determined by simulation.

A. Spiking neural networks

Artificial Neural Network provides the way for computational process in NoC. The First Generation[3] uses the multilayer perceptrons for its operation. A unique feature of this 1G is that it can only able to give digital output.

The Second-Generation (2G) is based on computational units that can provide a continuous set of possible output values using the weighted inputs. The output of this 2G sigmoid unit represents the current firing rate of a biological neuron[3]. In the conventional neural networks, there are interconnected units that receive the electric signal, called “action potential” for communication. In the terminology of neuroscience these units are called as ‘neurons’ and the connections are called as ‘synapses’. The aforementioned condition for spiking neural networks is the membrane potential threshold. The effect of crossing the threshold is a spike (action potential)[4]. This potential increases to the peak value and then decreases. The spike (action potential) is projected via synapses to all connected neurons which causes a slight change in its membrane potential[5].

The information communicated between neurons is encoded by the rate of spikes. The formulaic nature of spikes offers the potential to understand brain functions at a higher level than the neuron. The 3G SNN is inspired by neurobiological studies indicating that neural information is entirely encoded by firing rate. The Spiking neurons can communicate by using short pulses[6],[7].

B. Nano Machine based Hybrid NoC

Though NoC has many important advantages, it has a serious performance limitation such as high power consumption and latency. The traditional NoC with wired communication has a large number of functional nodes reduces its performance [8]. The wired line communication channel may cause more latency if it has a longer path, power consumption and low throughput[9]. Wireless offers an innovative solution to overcome thèse disadvantages. If the number of hops in a transmission path of a message is decreased, then the performance in latency, power dissipation and throughput can be improved[10].

In this work, a 8 x 8 mesh topology with 64 routers are used (i.e) number of routers, N= 64 for each layer of 3D NoC. The total number of routers are then divided by 4 to get 4 subgroups as illustrated in Fig.1 and each subgroup is numbered as I,II, III,IV.In the first subgroup the routers are numbered from 1 to 16.In the second subgroup the routers are numbered from 17 to 32.Similarly the third is from 33 to 48 and the fourth is from 49 to 64.

For example, router 1 is the source router wants to send the data to router 64 which is available in the IV subgroup. Once the destination is given the algorithm will work to determine the subgroup of the destination. If the destination router is available in the same subgroup then the algorithm will use the wired link for the data transfer. If the destination router is available in another subgroup then the source router sends the data to the Nanomachine router,which is available in the same subgroup.Tha nanomachine router will transmit the data through the wireless medium to other subgroups. The Wireless Nanomachine NoC (WNNoC) transceiver contains both transmitter and receiver as illustrated in Fig.2. In the transmitter, the digital data to be transmitted is given to a serializer. It is a Digital to Analog Converter (D/A) which converts digital data into its equivalent analog signal. The converted analog signal is then modulated with the center frequency in the range of THz. The modulated signal is given to a driver amplifier and then to the CNT antenna.It is proved that the Carbon Nanotubes (CNT) antenna is the better choice for WlessNoC [8,9].

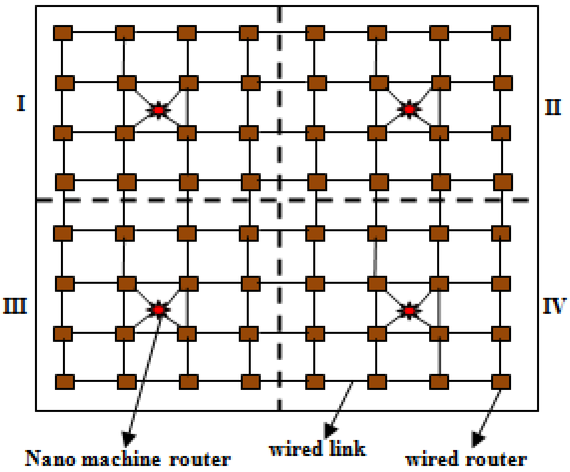

FIG.1 MESH TOPOLOGY OF A SINGLE LAYER OF 3D NOC

In this work, the CNT antenna has been used in a WNoC system. Since the frequency range is in THz, the size of the antenna will be small, so that the area overhead will be small. Previously reported work shows the bandwidth of Carbon nanotube antenna is around 500GHz [11],[12].This bandwidth can provide a higher data rate and it can also provide excellent directional properties. This high operating frequency causes skin effect and it will be ignored as the amount of skin effect is negligible which in turn reduces the power dissipation[13].

A novel technique called Time Divison-pulse based on-off Keying (TDPK) is used for wireless transmission and reception. In this technique, the asynchronous transmission of long pulses in the range of 10^{-18} seconds (attoseconds) is considered. The performance of the TDPK for the multicast network is also calculated in terms of the capacity of information. During the transmission of nano packets over a channel, the effect of propagation, the sources for noise and the statistics about the information are considered for getting effective results. Once the nanomachine router of the destination subgroup receives the signal, through the wired connection it will send the data to the destination router.

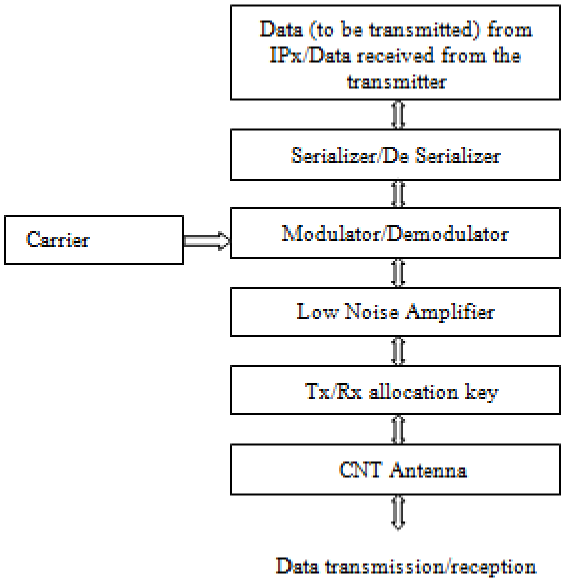

Fig. 2 Flow diagram of nano-machine Transceiver

In this work, a novel technique called Time Divison pulse-based on-off Keying (TDPK) is used to avoid various noise during transmission. A logical “1” is transmitted by using 10^{-18} second long pulse and the nanomachine remains silent when logical zeros transmitted for 10^{-18} second. When the nanomachine transceiver is silent for 10^{-18} second then it means the transmission of ‘0’ as shown in Fig.3If it is lesser than or greater than 10^{-18} second then it means that ‘no transmission’. In these two methods, energy consumption is reduced and the probable detection of an inappropriate symbol is lowered. The receiver declares the details about the packet transmission after receiving the pre-signal. In this technique constant length packets (32 bits) are used. Once the pre-signal is received at the receiver, it will count the number of bits in the packet received. Once the first transmitted pulse is received, the receiver nanomachine will wait for zepto second (10^{-21} second) to receive the next packet. Similarly, the transmitter nanomachine has to wait for zepto second (10^{-21} second) to send the next packet.This saves the power consumption of the network-on-chip. The nanomachine sends the packets to the other nanomachines during the time between transmissions.

The signal transmitted by a transmitter nanomachine during the time ‘t’ is given in equation (1),

$$NM_{Ti}(t) = \sum_{B=0}^{F-1} Amp_B \text{ x } T_S$$

(1)

where

$$T_S = T_p - T_I$$

F denotes the number of bits per packet, Amp_B denotes the Bth bit amplitude transmitted by the nanomachine transmitter. The value of Amp_B is either 0 or 1, T_S is the difference in the pulse time (10^{-18} second) and the time between two consecutive packet transmissions (10^{-21} second).

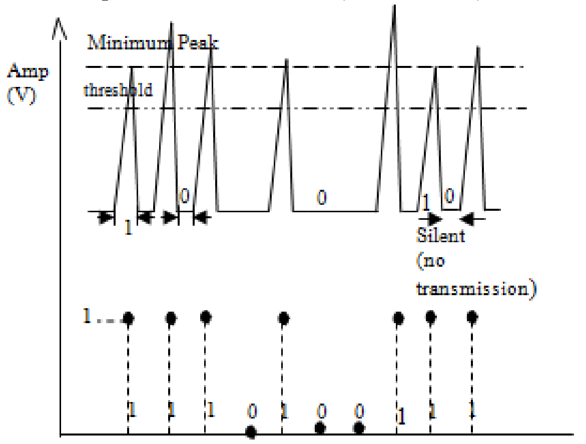

Fig.3 Action potential timing diagram of spike packets during data transmission

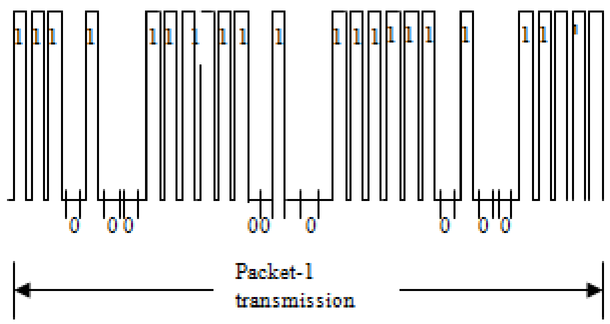

Fig.4 Discrete pulses of Action potential

The signal received by the receiver nanomachine at time't' is given in equation (2),

$$NM_{Rj}(t) = \sum_{B=0}^{F-1} \mathrm{Amp_B} \text{ x } \mathrm{T_S} \text{ x } \mathrm{h_{i,j}(t)} + \mathrm{A_{i,j}(t)}$$

(2)

where $h_{i,j}$ (t) is the Terahertz channel impulse response between the nanomachine i and j and $W_{i,j}$ (t) for the molecular absorption noise created between i and j. $h_{i,j}$ (t) depends on the specific medium conditions and distance between the transmitter i and the receiver j. Similarly, the molecular absorption noise $A_{ij}(t)$ purely depends on the transmission distance and nature of the transmission medium. The impulse response is the response of the signal which contains all single-frequency elements with unit magnitude. This method is also useful for multicast routing. The signal for multicast routing is exemplified in equation (3),

$$NM_{Rj}(t) = \sum_{N=0}^{N-1} \sum_{B=0}^{F-1} \mathrm{Amp_B} \text{ x } \mathrm{T_S} \text{ x } \mathrm{h_{i,j}(t)} + \mathrm{A_{i,j}(t)}$$

(3)

Here 'N' exemplifies the total number of the router in the NoC network. It should be noted that the time between transmissions Ts must be larger than $10^{-18.}$ So that the nanomachine transceiver can transmit or receive the spike packets without overlapping.

In order to utilize minimum power consumption during the transmission of packets from the transmitter to the receiver, a threshold voltage in the action potential of the spike and it is considered as '1'.Once the spike pulse reaches the threshold value it means a bit '1' is received. This threshold voltage is calculated according to the minimum peak value of the spike pulse received at the receiver side. Fig.4 illustrates the transmission of spike pulse represent 1 and 0.To transmit a '1' or '0' it needs 10^{-18} seconds and the time between consecutive 0s or 1s or 0s and 1s is 10^{-21} seconds and the time between two consecutive packets is also 10^{-21} seconds.

II. RESULT AND DISCUSSION

The simulation part of this work is done with Cadence software with 18 nm tsmc technology to achieve high-speed data transfer and Hamster VHDL-AMS software is used for analog simulation.

Fig.5 shows the output of the deserializer after the conversion of the received analog signal from the nanomachine receiver antenna. This deserializer converts the analog signal into discrete pulses. The binary data is extracted from these discrete pulses as shown in Fig.6.

Fig.5 Output of deserializer in the nanomachine receiver

Table 1: Comparison of Delay for Wired and Wireless Routers

No.of Routers	Latency[ns]		
	Wired NoC	Wireless NoC	Hybrid NoC
4	1.02	0.0000966	0.00732
8	3.2	0.0003	0.027
16	4.9	0.0004738	0.039
32	7.5	0.0007221	0.0676
64	9.2	0.00088	0.084

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128	12	0.00115	0.1111
256	14.77	0.00147	0.14345

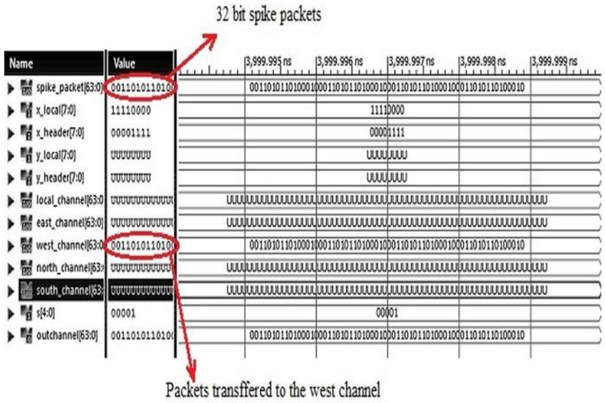

Fig.6 Received data of spike packets

The latency in nanosecond is obtained for various number of routers by simulation in 18nm tsmc technology. Table 1 shows the comparison of Latency (in terms of nanoseconds) of wired, wireless and hybrid NoC technology for 4, 8, 16, 32, 64, 128, 256 routers. It is shown that the wireless router has a reduced delay of nearly 1000 times when compared to that of wired router. The hybrid NoC platform which is used in this work has the advantage of achieving high-speed data transfer by the use of wireless router.

III. CONCLUSION

The proposed Nano Machine based Hybrid 3D Network-on-Chip works with the principle of Spiking Neural Network (SNN) technique.This architecture uses a Nanomachine Transceiver with Carbon nanotube antenna which uses the novel pulse-based technique to transfer the packets between the subnet of NoC to reduce the latency. The pulse-based technique improves the latency during packet transmission and reception in Nanomachine NoC compared to the previously reported work for 18 nm TSMC technology.

REFERENCES

1. Carrillo, Snaider, Jim Harkin, Liam J. McDaid, Fearghal Morgan, Sandeep Pande, Seamus Cawley, and Brian McGinley: 'Scalable hierarchical network-on-chip architecture for spiking neural network hardware implementations', *IEEE T Parall. Distr*.,vol.24,2013,pp. 2451–2461.
2. Harkin, Jim, Fearghal Morgan, Liam McDaid, Steve Hall, Brian McGinley, and Seamus Cawley: 'A Reconfigurable and Biologically Inspired Paradigm for Computation Using Network-On-Chip and Spiking Neural Networks', *Int. J. Reconf. Comput*., 2009, pp. 1–13.
3. K.Balamurugan,M.Vijayaraj,S.Jeba Thinaka, 'Performance analysis of CNT and Phased array antenna for wireless NoC using ANSOFT', International Journal of Applied Engineering Research**,** Volume 10,No.1 Feb 2015
4. Harkin, Jim, Fearghal Morgan, Steve Hall, Piotr Dudek, Thomas Dowrick, and Liam McDaid : 'Reconfigurable platforms and the challenges for large-scale implementations of spiking neural networks', in Proceedings - 2008 International Conference on Field Programmable Logic and Applications, FPL 2008, pp.483–486.
5. Maass, W,Networks of spiking neurons: 'The third generation of neural network models, *Neural Network's,vol.10*, 1997, pp. 1659–1671.
6. Maguire, L. P., T. M. McGinnity, B. Glackin, A. Ghani, A. Belatreche, and J. Harkin: 'Challenges for large-scale implementations of spiking neural networks on FPGAs', *Neurocomputing*,vol.71,2007, pp.13–29
7. Pande, Sandeep, Fearghal Morgan, Seamus Cawley, Tom Bruintjes, Gerard Smit, Brian McGinley, Snaider Carrillo, Jim Harkin, and Liam McDaid: 'Modular neural tile architecture for compact embedded hardware spiking neural network', *Neural Processing Letters*, vol.38, 2013, pp. 131–153.
8. Pande, Sandeep, Fearghal Morgan, Gerard Smit, Tom Bruintjes, Jochem Rutgers, Brian McGinley, Seamus Cawley, Jim Harkin, and Liam McDaid : 'Fixed latency on-chip interconnect for hardware spiking neural network architectures', *Parallel Computing*,vol.*39*,2013,pp. 357–371.
9. Vijayaraj M, Balamurugan K : 'Performance oriented docket-NoC (Dt-NoC) scheme for fast communication in NoC', *J Semicond Technol Sci*., vol.16, 2016,pp.359–66.
10. Ganguly, Amlan, Kevin Chang, Sujay Deb, Partha Pratim Pande, Benjamin Belzer, and Christof Teuscher, Scalable hybrid wireless network-on-chip architectures for multicore systems, *IEEE T Comput.*, vol.60,2011,pp. 1485–1502.
11. Jornet, J. M. & Akyildiz, I. F., Information capacity of pulse-based Wireless Nanosensor Networks, in 2011 8th Annual IEEE Communications Society Conference on Sensor, Mesh and Ad Hoc Communications and Networks, SECON 2011,pp. 80–88.
12. Deb, S., Ganguly, A., Pande, P. P., Belzer, B. & Heo, D: 'Wireless NoC as interconnection backbone for multicore chips: Promises and challenge',. *IEEE J. Emer and Selected Topics in Circuits and Systems*, vol.2,2017,pp.228–239.
13. Saxena, V., Wu, X., Srivastava, I., & Zhu, K., 'Towards Neuromorphic Learning Machines Using Emerging Memory Devices with Brain-Like Energy Efficiency*', Journal of Low Power Electronics and Applications*, vol.8, 2018, pp.34-44.

AUTHORS PROFILE

Dr.K.Balamurugan received his PhD degree in Network-on-Chip (NoC) from Anna University Chennai. He Obtained his Bachelors of Engineering degree from Manonmanium Sundaranar University and Masters Degree from Anna University, Chennai. He has 15 years of Teaching and Research experience in the field of NoC/SoC. Currently he is working as Professor in the Department of Electronics and Communication Engineering at Swarnandhra College of Engineering and Technology, Narsapur, Andhra Pradesh. He has published his research papers in the field of VLSI Design/NoC in various National, International Journals and Conferences.

R.Shijukumar obtained his Bachelors of Engineering degree from Manonmanium Sundaranar University and received his first Master degree in Applied Electronics and the second Master degree in VLSI Design from Anna University,Chennai.He started his career as Lecturer in Engineering.He worked as Assistant Professor in various Engineering Colleges and then he switchedover to Industry.Currently he is working as a senior R&D Engineer at FIRMTECH, Thiruvananthapuram, Kerala, India. He has published research papers in the area of VLSI and Embedded systems in International Journals.He has presented his research work in many International conferences around the world.