International Journal of Engineering and Advanced Technology (IJEAT)
ISSN: 2249-8958 (Online), Volume-9 Issue-1, October, 2019

Technological Developments in Direct Grid Connected Power Converters for Solar PV Power Plants

Devineni Gireesh Kumar, Aman Ganesh

Abstract*: Most of the countries in the world are concentrating on renewable energy generation, due to day-day increase in population increasing the energy demand, also to make their environment sustainable. With the many of features, use of megawatts rating solar photovoltaic (PV) power plants are becoming more popular for upgrading the existing power generation throughout the world. Moreover, among the existing renewable energy generations, solar power is the primary choice to meet the rapidly increasing demands; since solar PV plant installing time is relatively quick, say about in 3- 4 months, compared to conventional (thermal, hydro & diesel) plants which may require about 3-4 years. The low voltage (270–700V) power converters require a filter and a step-up transformer for interconnecting the local grids with solar PV power plants. The advances in power converters without transformers and filters have recently become more attractive for solar PV power plants connected directly to grid. The study of this article describes the essential requirement and the technological developments in the design of power electronics converters, together with their modulation schemes to integrate solar power directly with standard power grid. This article, review ongoing research activities and the probable directions for the future research in developing inverters for cost-efficient grid connected solar PV plants.

Keywords: PV Power Plant, Power converter, Solar Photovoltaic, MPPT, MLI, H-Bridge, Transformer less inverter.

I. INTRODUCTION

Technological advancement and cost effectiveness are the two major factors; make use of solar energy to meet the increased energy demands [1], [2]. During 2007 to 2017 there is 83% of cost reduction in solar panels are noticed, which steers to decrease the cost of generation from solar PV panels. The cost of generation dropped to 73%, from INR 24.82 to INR 6.89 per kWh during 2010–2017. It is anticipated that the cost further dropped to below INR 4.12 per kWh for 2023. Thus the multi-megawatt rating PV energy has become into reality. The standard solar power plants mainly consist of PV modules, which are physically exposed to environment to convert sun radiation into DC power. One of the major component of solar plant is power modulator (Power converter), which convert the dc-dc and dc to ac), a medium voltage transformer (normally of 3.3 to 33kV, to feed the low power from solar plants to medium voltage grid), the switchgear and protection apparatus. Usually the rural areas are best choice for the installation multi-megawatt solar plants, located away from living area for the crisis of land availability for longer periods. For example, 1000 MW solar park situated in Karnool, India requires 5932.32 acres (24km^2) of land where 4 meters of 320W solar panel s are attached to power converters and 220/33 kV transformer s to supply solar power to the 33 kV grid. Figure.1 shows the conventional model of grid integrated solar modules [2]–[5]. This article provides the overview of research trends in power converter systems, their control systems and future study directions towards RES grid inclusion for reliable and cost-effective operation of solar photovoltaic energy plants energy converters. The review also focuses on prospects, key and technical difficulties in the operation of solar photovoltaic.

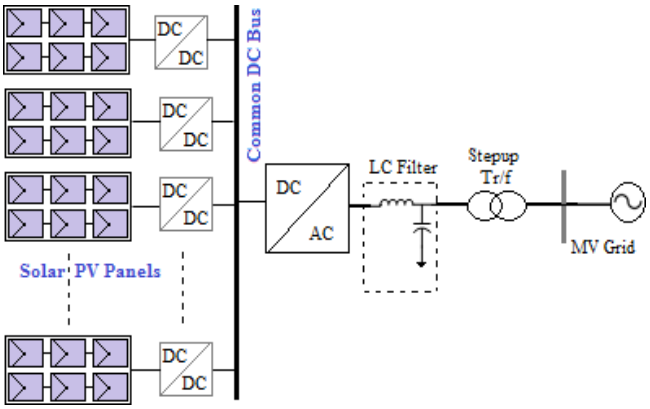


Fig.1. Common grid integration of solar PV with low voltage inverter.

II. FUNCTIONS & OBJECTIVES OF THE ARTICLE

A. Function of Article

- Literature organization.
- Identifying grid connected inverter design approaches

Revised Manuscript Received on October 30, 2019.
* Correspondence Author
Devineni Gireesh Kumar*, Research Scholar, School of Electronics and Electrical Engineering, Lovely Professional University, Phagwara, Punjab, India. Email: gireeshkumar.d@bvrit.ac.in
Dr. Aman Ganesh, Professor, School of Electronics and Electrical Engineering, Lovely Professional University, Phagwara, Punjab, India.
Email: aman.23332@lpu.co.in

- Describe techniques for optimum MLI switching angle control for various dc link voltages and changes in the modulation index.
- Identifying switching methodologies for multi level solar PV inverters.
- Identifying research gaps and recommending fresh fields of studies.

B. Objectives of the Article

- Provide effective galvanic isolation for solar PV panels to protect from transient faults in the grid.
- Study the methods of leakage current elimination in solar PV arrays due to stray capacitance effect.
- To comply with grid codes, design an efficient multilevel inverter is to produce high-quality output waveform with little harmonics.
- Make the primary circuit and control circuit more compact to decrease switching losses and enhance the effectiveness of the inverter.
- Compare different optimization techniques adopted for switching of semiconductor devices and possibility of their applications to multi level inverters.

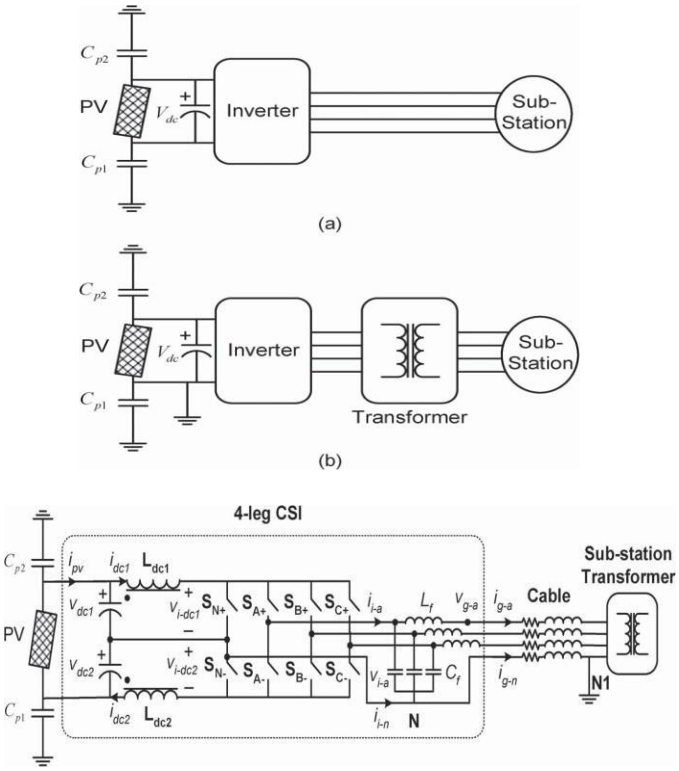
III. DEVELOPMENTS IN DC TO AC POWER CONVERTER TOPOLOGIES

While the development of medium voltage converters for multiple applications such as motor drives, solid state transformers and solar photovoltaics presents some prevalent difficulties, there are particular difficulties for large-scale photovoltaic solar systems that render the overall converter and control circuit complicated. The theory of multilevel inverters was first introduced in 1971, as a substitute to the series connected power electronic switching devices for MV industrial applications [6]. During the 1971-1981 era, three kinds of multilevel inverter topologies were suggested, including neutral point clamped (NPC), flying capacitor (FC) and cascaded H-bridge (CHB)[6]-[8]. The concept of a three-level NPC converter has become more common and still commercially available due to its simple circuit configuration. However, the rise in NPC levels considerably increases the number of clamping diodes. [9], [10]. The inverse retrieval times of the clamping diode render this topology not feasible to develop a medium voltage converter of high level [11]. Like this, the topology of NPC, the topology of the FC is too inadequate for MV and HV applications because it uses a large number of condensers requiring circuits for prior charging and balancing [9], [11]. Furthermore, a large dc link capacitor needs for single cell topology, limits its application to medium and high voltages, particularly to solar PV applications, where different PV panels is to be connected in series [12], [13]. These huge number of series connected PV panels will decrease the overall system efficiency due to common MPPT and series resistance [14].

Modular structures have been developed by cascading the full bridge inverters, named multi-cell multilevel CHB converter topology, which provides MPPT operation at module level and scalable to various voltage levels. Also, clamping diodes and capacitors are not used by CHB topologies [11]. Even so, the CHB is get rid of the more number of series PV modules, however due to continuous variation of module parameters and the partial shading will cause the mismatch problems [15]–[18]. These mismatch problems creates imbalance and resulting to low quality of power to the grid [19]. While using CHB converters for PV applications, this module mismatch is another challenge compared to the use of converters in solid state transformers (SST) [20]–[23] and solid state motor drives [24], [25].

A. Direct Grid Connected Transformer less Inverters

High demands are placed on the effectiveness and life of grid linked PV inverters. The current source inverter (CSI) provides excellent performance compared to voltage source inverter for the solar photovoltaics due to its reduced dc link capacitor. Although, using the traditional 3-phase PWM current source inverter, an increased earth leakage current is injected into the grid. To nullify this leakage current, an isolation transformer is needed between AC grids and PV modules. Therefore the system's price and size is improved and the general effectiveness is reduced. A modified CSI (4-arm) current source inverter is suggested in figure (2) to address the above constraints [26]. The suggested CSI nullifies the leakage current of the earth without use of isolation transformer that increases overall efficiency and reduces system cost compared to the conventional CSI-based solar grid.



(c)

Fig.2. Grid-connected system configurations

(a) Line diagram of direct grid connection.
(b) Line diagram of grid connection with isolation tr/f.
(c) Direct grid connected modified 4-leg VSI.

The quasi-Z-source inverter (qZSI) can decrease or increase the input voltage without any dc to dc converter, thus becoming a common inverter topology, so it can be used for transformer less topology. Due to its one stage conversion the qZSI is a great option for an effective, transformer less grid-tied inverter. Although, owing to absence of galvanic isolation, the common mode current is a significant issue in transformer fewer topologies. A modified pulse width modulation (PWM) approach is suggested [27], Uses two extra semiconductor switches to control the qZSI to reduce the common mode current. There are four characteristics of this topology: 1) Use phase-leg shoot-through to increase dc voltage to a specific voltage level, eliminating the use of dc-dc converter; 2) Eliminates PWM's dead time and anticipates freewheeling action through additional switches; 3) Reduces the current of the common mode by reshaping the PWM and adding additional switches to the inverter output; and 4) Eliminates the conduction of H-bridge body diode, which has lower reverse recovery characteristics. This qZSI topology is an effective control of reactive power.

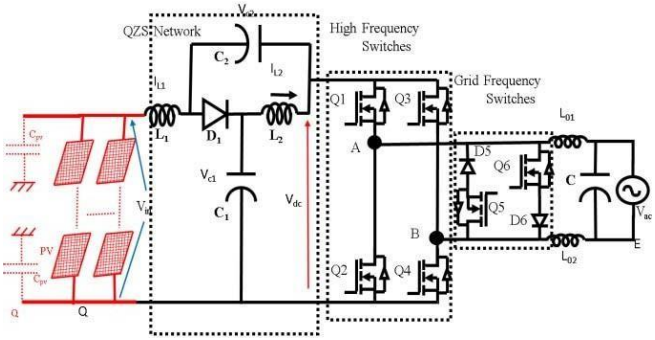


Fig:3. Quasi z-source inverter with extra switches.

Two series connected solar PV sub-arrays are controlled by single phase direct grid integrated transformer less converter [28]. These two arrays operate at the corresponding MPP when they are open to varying atmospheric conditions. The total series of connected panels in the sub-array is decreased to half, while two sub-arrays are connected in series. Reducing the amount of series linked PV modules within the sub-array results in improving the actual magnitude of energy abstracted from the sub-array while sub-array modules are subjected to variable atmospheric conditions. The inverter structure ensures that the common mode voltage does not hold elements of high frequency, thus minimizing the magnitude of the leakage current in the solar panels well within the permissible limit. A thorough design analysis is performed by deriving its small signal model. The topology of the scheme is shown in figure (4).

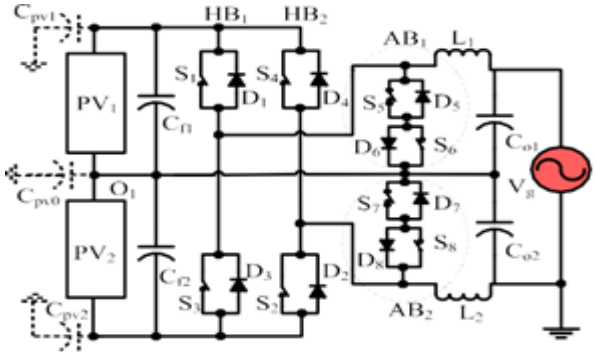


Fig:4. Combined half-bridge inverter with AC bypass

A single-stage inverter system is described in [29] for grid-connected PV systems. This inverter topology boosts low-voltage solar power and also converts solar PV energy (DC) to high-quality AC power that can be directly connected to the grid in a single stage, while tracking the maximum power from the PV panels is also possible. The current waveform with total harmonic distortion is limited to supply the grid as per the IEEE-519 standard. The topology shown in figure (5), has several valuable characteristics such as, excellent use of the solar PV array, higher efficiency, cheaper price and compact size. In addition, this topology allows the PV array into the grid as a variable source, thereby enhancing the overall system security.

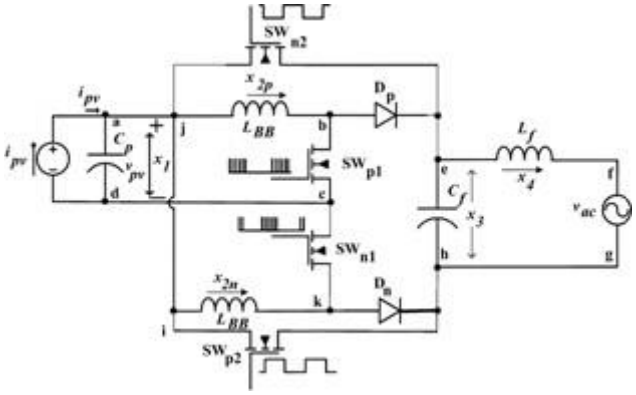


Fig.5. Single stage grid connected inverter topology.

In [30], a novel topology for photovoltaic (PV) energy converters is developed. This is a transformer-less configuration with grounded PV array film condensers. The topology is designed to minimize the complexity of the circuit, remove the currents of ground leakage, and enhance reliability. This topology attains the reasonable efficiency about > 97%, by the key enabling technology uses Silicon Carbide SiC transistors.

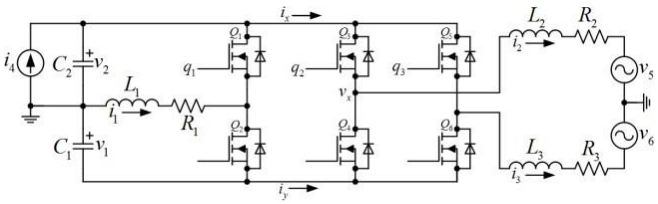


Fig.6.
Bi-directional two half-bridge buck-boost converter.

Figure (6) shows a bi-directional buck-boost converter with two half bridges, in which adverse PV array terminals are attached to the ground potential through the inverter's neutral line to eliminate the solar array's leakage currents. This circuit utilizes power decoupling setup through DC-DC converter's bi-directional power flow, allowing tight voltage regulation to track Maximum Power Point Tracking (MPPT). However, with the increased switching frequency, high power loss occurs in semiconductor devices. Also reduced switching frequency will increase the peak flux density, which in turn increases the inductor losses. Hence this converter is operating at optimal switching frequency about 40 kHz.

The topology of the impedance source inverter (ZSI) is capable of eliminating various stages of energy conversion in dc – ac and achieving high voltage boost in a single stage.

The ZSI topology is intended to increase the dc input voltage and match the inverter ac output voltage demands with two inductors and two condensers. For the application of a string inverter setup, a 1-phase modified impedance source inverter (MZSI) is described in [31]. Figure (7) shows the MZSI schematic.

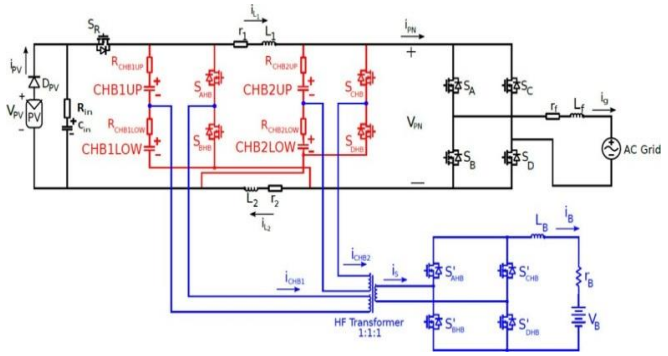


Fig.7. Modified Z-Source inverter topology

MZSI based topology has two purposes of its operation.

a) It can directly connect the AC grid without any isolation transformer, since the ZSI itself provides the galvanic isolation whenever required.

b) It also provides energy through a 3-winding isolation transformer and a full bridge inverter to charge the EVs. This is parallel connection configuration along with the direct AC grid connection to charge the EVs or for energy storage system (ESS).

MZSI boosts the input voltage for requirements of AC grid and also provides energy to charge EVs efficiently by a single converter topology.

A transformer less PV inverter with cascaded H-bridge for leakage current reduction in solar array is presented in [32]. The conventional three-phase cascaded H4 grid inverter is evaluated using the common mode current model. The connection between voltage of common mode, voltage of differential mode and leakage current is evaluated. The H4 cascaded bridge has good reliability, but it has a drawback that, it cannot reduce the leakage current; reasons for H4 inverter failure in reducing the leakage current are discussed. To fix this issue, a traditional three-phase cascaded H5 setup is introduced for grid-connected PV inverters and their switching modulation systems, which can considerably mitigate the leakage current. Below figure (8) represents the modular cascaded H5 inverter configuration for grid connected PV systems.

Common-mode current in transformer less PV inverters creates severe electromagnetic interference and insecurity, further decreasing the efficiency of PV inverters. A H5 inverter topology is presented [33] in which, by common grounding of the PV array and AC grid, an extra switch is added between the input and the inverter bridge arms as shown in figure (9). But the junction capacitors of additional switch in H5 inverter topology will cause serious problem of CM current with its asymmetrical structure in practice. During turn on and off of switches in H5 topology, the junction capacitors charging and discharging process causes the mid-point voltages of bridge leg. Because of this, CM voltage frequently swings, which also produces large CM current [33]. An EMI filter is needed to decrease the CM current, which will further increase the inverter's price, volume and weight.

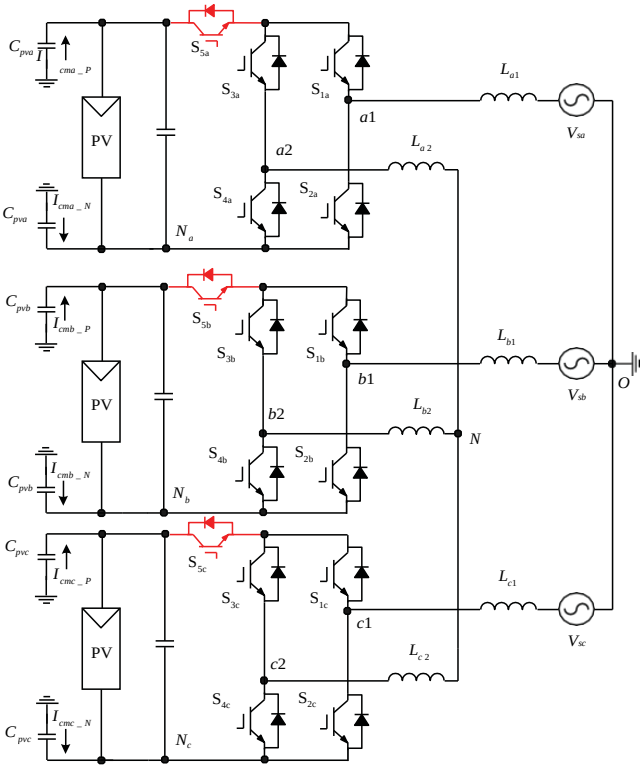


Fig.8. Three phase cascaded H5 inverter topology

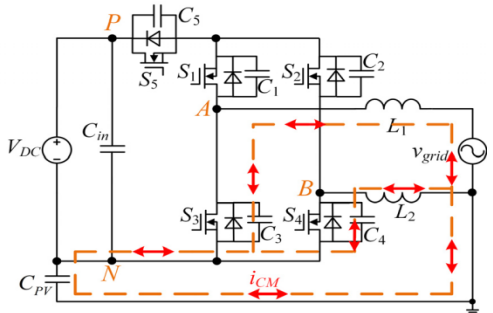


Fig.9. Single phase common mode H5 inverter topology

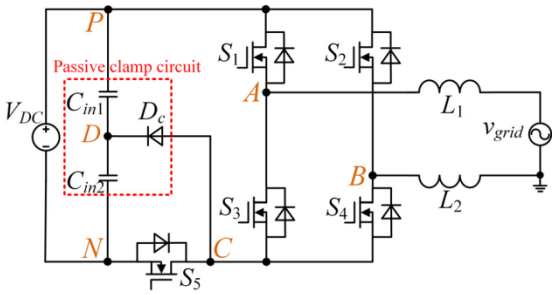


Fig.10. Common mode single phase H5 inverter topology

An enhanced H5-D topology is described in [34], thus reducing the CM current by adding a clamping diode to the topology of H5 to make the common-mode voltage constant. The H5-D topology is shown in figure (10), using the same electrical parameters and switches of H5 topology, the CM current is brought to one-third of CM current in H5-D topology. Due to its easy installation and practical operation, H5-D topology anticipates the best choice for transformers less single phase PV inverters.

A two-half-bridge H4 topology is presented in [35], one half-bridge consists of two IGBT switches S1, S2 and C1 and the other half-bridge consists of switches S3, S4 and C2. By introducing ground connection between adverse PV array terminal and neutral grid point, the stray capacitance of the PV array is bypassed. A transformer-less multilevel grid connected inverter is proposed [35] in which 3-level (fig.11) and 5-level (fig.12) topologies are developed and compared for eliminating the leakage current.

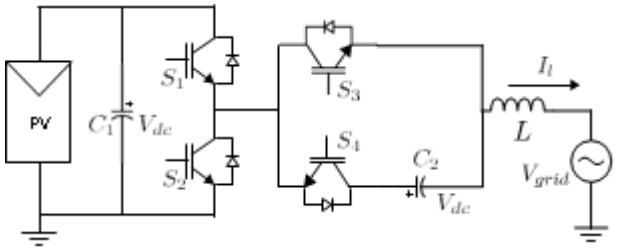


Fig.11. 3-level H4 transformer less inverter topology

The important characteristics of H4 & H6 transformer less inverter are outlined as follows:

- To bypass the stray capacitance of the PV array, completely eliminate the CM leakage current by ground connection.
- This inverter's modular topology can be readily expanded to n-level by adding the appropriate number of half-bridge modules.
- The topology of the 3-level H4 inverter is first of its kind which eliminates the current of CM leakage with limited switches (four).
- The topology of the 5-level H6 inverter (multilevel) is first of its kind, eliminating the current of CM leakage with fewer (six) switches.
- For the identical DC link voltage, at least 27 percent and maximum 100 percent more output voltage is achieved with the half bridge topologies. This topology is therefore cheap to replace the topologies of the NPC.
- It gives a superior dynamic response.
- Compared to standard full bridge transformer less inverters like H5, Heric and FB-DCBP, the capacitance requirement of this topology is comparatively large in size.
- Multilevel topology decreases current THD, leading in reduced filter requirement size, with superior efficiency in mitigating CM current; henceforth this topology is an option to standard transformer less grid-connected PV inverters.

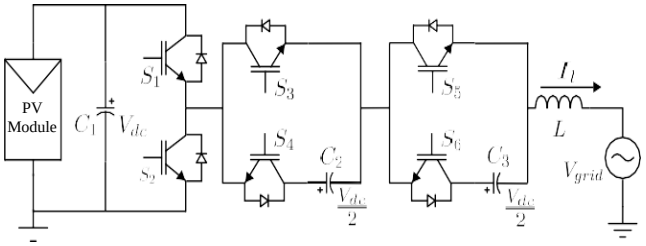
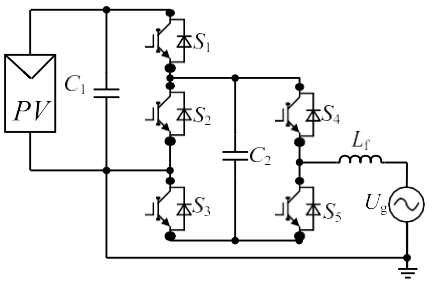
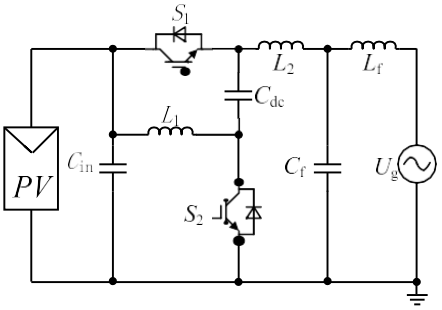


Fig.12. 5-level H6 transformer less inverter topology

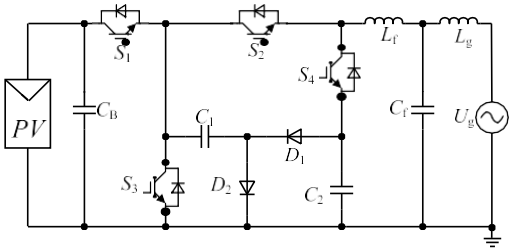
Common mode grounding topology is a category of topologies proposed recently, which can fully get rid of the leakage current. The idea is a straight link of the negative photovoltaic array terminal to the medium voltage AC grid neutral point, which allows a short circuit of the parasitic PV array capacitor. In [36], a common mode grounding topology is provided with an efficient DC bus model. Although the flying condenser does not charge in negative half-cycle, the output voltage will therefore be distorted in negative half-period. The inverter topology shown in [37] has two-level performance, consisting of more harmonic content. A popular grounding topology based on multi levels is described in [35], but its structure and operation of the control circuit is complicated. The more level, the more complex in the control circuit, the more difficult it is for scientific applications to perform. Also presented in [38] is a common mode grounding topology similar to the efficient DC bus. However, it requires a two-stage transfer of energy, which increases the loss. Few common mode grounding topologies in single phase transformer-less inverters are shown in figure (13).



(a)



(b)



(c)

Fig.13.Single-phase common mode transformer less inverter

(a) Topology in [36]
(b) Topology in [37]
(c) Topology in [38]

In perspective of the constraints in the above topologies [36], [37] & [38], a novel flying capacitor topology is proposed in [39] with charging and discharge schemes. This topology obtained a new transformer-less inverter family for PV grid integration, where the utility grid's neutral point is immediately attached to the solar PV array's negative terminal. This prevents the impact of stray PV array capacitance and totally eliminates the leakage current owing to stray capacitance. In addition, topology utilizes only 5-number of semiconductor switches, reducing circuit costs and power losses. While operating the inverter, the path of current flow takes from 2-switches, which also reduces the conduction losses. Finally, to verify the correctness and effectiveness, the suggested inverter topology for 1kVA prototype is constructed.

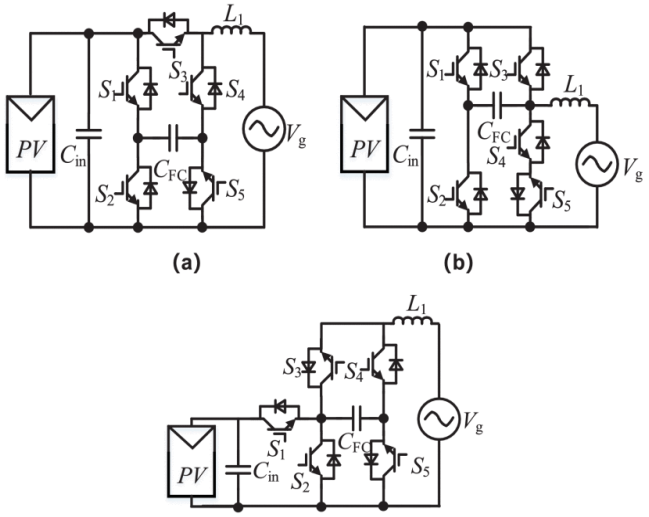


Fig.14. Novel H5 topologies proposed in [39].

Different design topologies of multi level inverters with their switching devices and components required are listed in below table and compared. The same were represented in a bar diagram for better understanding of these concepts.

Table:1 Comparison of devices & components quantity

Topology	Switches	Diodes	Capacitors	Inductors
QZSI	6	3	3	4
MCSI	8	0	2	5
Combined H-Bridge	8	8	4	2
MZSI	9	0	5	0
H4	4	0	2	0
H5	5	0	2	0
H6	6	0	3	0
Topology in [36]	5	0	2	0
Topology in [37]	2	0	3	2
Topology in [38]	4	2	4	1
Topology in [39]	5	0	2	0

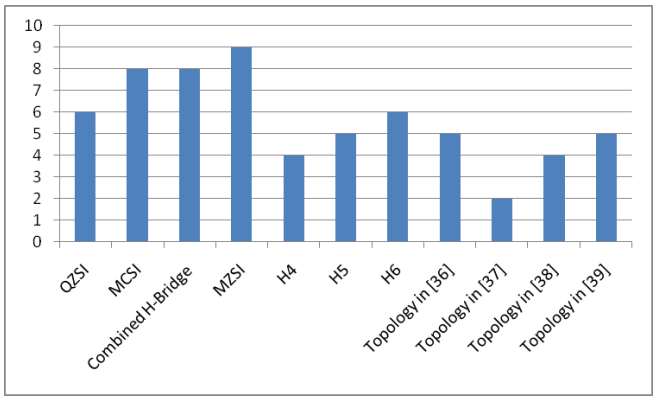


Fig:15. Comparison of number switch requirement of different converter configurations.

B. Developments in Multi Level Inverters & their Control Schemes.

To suit a near sinusoidal staircase waveform, Multilevel Inverter utilizes number of semi-conductor switches that are properly connected to different reduced dc voltage sources.

A multilevel inverter's most pleasant trademarks are provided as follows:

- Common mode voltage.
- Input current.
- Switching frequency.
- Reduced harmonic distortion.

Certain Applications of Multilevel Inverters:

- Variable frequency AC Motor drives

- Active power filters
- Electric vehicle motor drives
- DC source utilization
- Power factor correction equipment
- Consecutive frequency link systems
- Integration of non-conventional energy resources

Multi-level inverter design has got plenty of literature, among the existing investigations, some of the research investigations have been presented here.

A basic multi cell voltage-source inverter (VSI) proposed in [40]. These converters are spread from a pleasing concept to a real-life industrial alternative for the future. The main features such as harmonic mitigation and especially the equality of open-loop nominal voltage were discussed. Also, find out how to use this theory for high-power applications. In addition, developments in the field of wide bandwidth control are still anticipated, yet a big proportion of applications are already using this topology and not only the field is high power.

Multilevel diode-clamped inverters (figure.16), flying-capacitor (figure.17) to replace the two-level inverters with series-connected switches or transformer-based stepped wave inverters in high and medium voltage applications such as variable frequency drives and static VAR compensators shown in [41]. The MLDCL inverters decrease switches by about half the number of switches required. Their clamping diodes, capacitors, gate drive circuits are also reduced compared to current MLI topology counterparts. Regardless of the excessive VA rating of power switches, the new MLDCL inverters are still costless due to the simple gate drive circuits and the minimum number of switches, which further reduces the size and volume of the topology. The cost is further reduced with novel diode clamped and the flying capacitor inverters due to considerable reduction in the VA rating of the diodes and voltage rating of the capacitors.

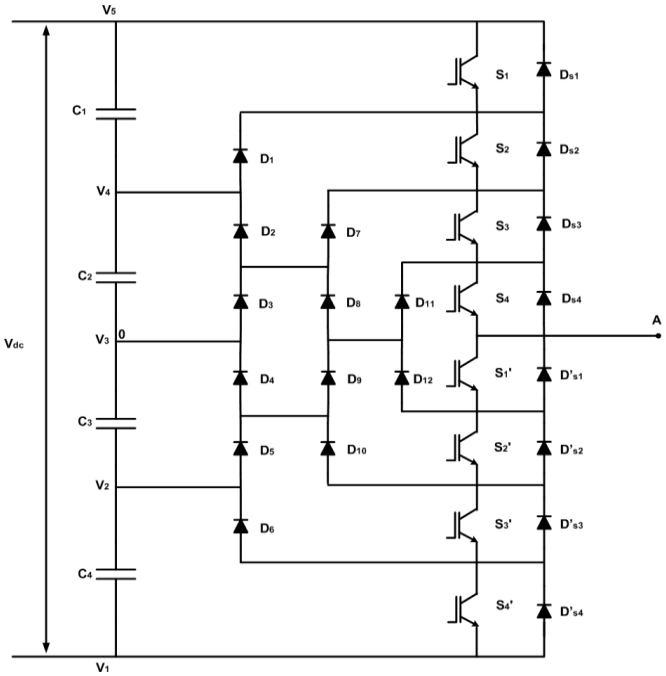


Fig.16. Diode clamped multi level inverter topology

A contemporary multi-level topology with two separate designs, specifically the H-bridge topology and an additional bipolar switch suggested in [42], significantly reducing the power circuit complexity. To optimize the topology size, a programmable gate array (FPGA) based power modulator circuit and a firing angle controller is developed. The above two ideas are used to design a five-level bridge inverter. This new setup of the converter decreases the number of components and optimizes the design compared to the current counterparts of topology. This topology with the additional bipolar switch works as expected, producing the required five-level output using only 5-number of semiconductor switches and condenser clamping supplied by two splitting condensers ; and operating at high modulating frequencies (up to 200 KHz), creating smooth output voltage profile.

The comparison between unequal symmetrical and asymmetrical configuration of Multi level inverters were discussed in [43]. This topology introduced a setup of unequal DC connection voltage. In this process, one of the voltages of the capacitors during operation is twice the level of the capacitors. Asymmetric DC coupling scheme is implemented as there is an adjacency between all output voltage levels which implies that distinct voltage levels can be obtained with only one switch. Using asymmetric arrangement, nine distinct voltage levels can be produced at phase voltage, which is two voltage levels more than conventional four-level inverters with the same number of switching devices. This will result in a decrease in output voltage with low and high harmonic content.

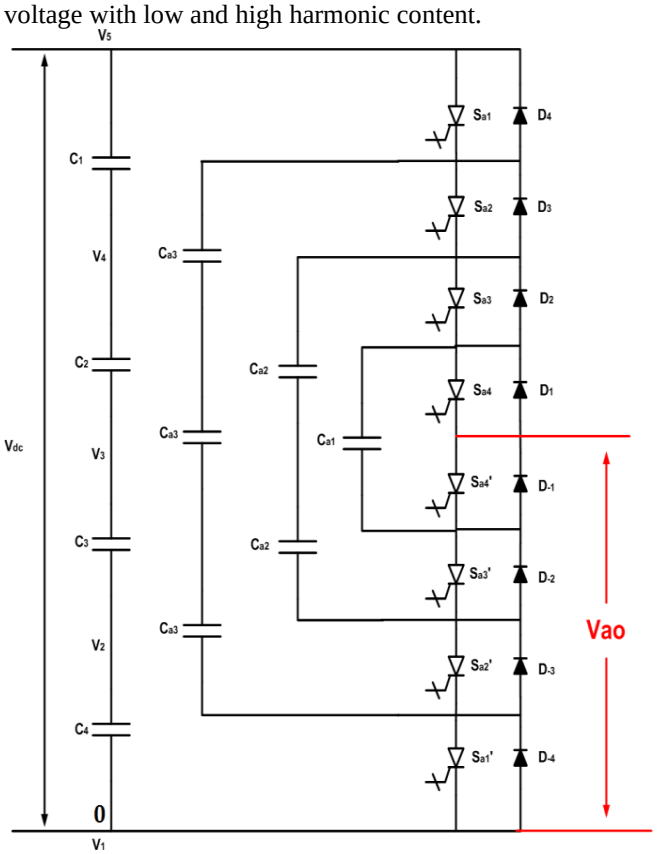


Fig.17. Flying capacitor based multi level inverter topology

A real-time algorithm for minimizing THD under staircase modulation is developed in multi-level inverters with unequal or variable voltages [44]. This has an algorithm that calculates the switching angles for multilevel inverters with unequal or variable voltage steps under the modulation of the staircase in real time. The voltage THD is minimized with the suggested algorithm, which is demonstrated by the rigorous mathematical derivation. A new expression of THD is implemented to substantially simplify the derivation. The computational complexity is evaluated to demonstrate that the computing time is low enough to be able to handle popular microprocessors or DSPs in real time. Thus, in multilevel inverters with unequal or variable voltage measures, the suggested algorithm is made appealing by minimizing the voltage THD and the calculating capacity in real time. Experimental findings check the algorithm's efficiency.

A PSO optimization algorithm for Cascaded Multi level inverter in connection with selective harmonic elimination method to minimize the harmonic content in the MLI output presented in [45]. The PSO was proposed in H-bridge cascaded multilevel inverters to fix the SHE issue with unequal dc sources. When the resulting strategy reaches the limitation of modern algebra software tools, optimum switching angles can be found in the suggested technique by simple analysis. A 11-level cascaded H-bridge inverter is supplied with simulation and experimental outcomes to validate the precision of the computational outcomes.

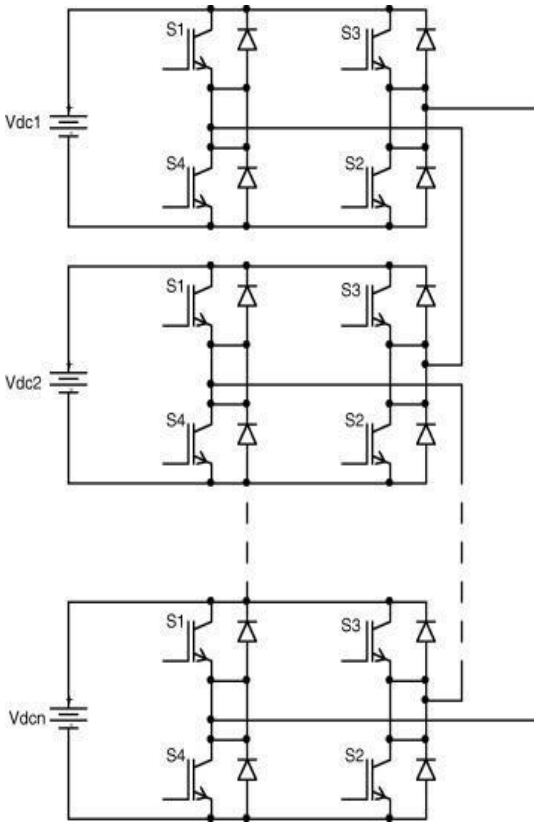


Fig.18. Cascaded H- bridge multi level inverter topology

A novel methodology is provided in [46] (Figure.18) to eliminate the chosen harmonics in the cascaded H-bridge MLI. The Bee algorithm is an optimization algorithm based on honeybees ' natural foraging behavior to discover the best solution. In running the converter, this algorithm offers optimum switching angles. Elimination of low-order harmonics is explored in this article using SHEPWM approach. To fix the equations, BA is implemented. Solutions also have a close probability of achieving global minimum runs for 1, 2, 5, and 10 times, and this probability is greater than the same runs for GA. Finally, experimental findings are provided to confirm BA alternatives that validate the precision of the technique proposed.

A modern multi-level inverter designated as Multi Level Module (MLM) with a decreased amount of power electronics components is implemented in [47]. The topology is based on balancing circuits of DC link voltage that use condensers instead of thyristor switches. The topology proposed extends the flexibility of the design and the possibilities of optimizing the converter for different objectives. It has been shown that for a given number of voltage levels, the structure consisting of MLMs with two switches has the minimum number of switches. Comparison was made of the suggested topology with other topology. The suggested topology has been shown to provide 125 output voltage levels with a maximum of 400 V, using 24 IGBTs and 604.5V blocking voltage on bidirectional switches However, the other topology generates 161 voltage levels using 28 IGBTs and 1000 V blocking voltage.

The suggested topology not only has reduced switches and components compared to the other one, but also its full bridge converters operate at reduced voltage.

By cascading the level generation part with the voltage reversal presented in [48], a new scheme is obtained depending on the setup of the level generation part shown in figure (19), it can also be operated at any required level. Therefore, additional components are only needed at the level generation portion for greater level operation. Consequently, the number of components required for the proposed MLI is lower than the conventional topologies for operation at a higher level. The suggested MLI's prominent characteristics are: 1) The suggested MLI setup consists of LGP and PGP cascades. 2) Only the switches needed at the BUs residing in the LGP are needed for greater level operation. Compared to standard topologies, this decreases the need for additional equipment. 3) Each dc voltage source is also shared by all levels in the presented MLI topology. Therefore, there is no possibility of inter-phase asymmetry.

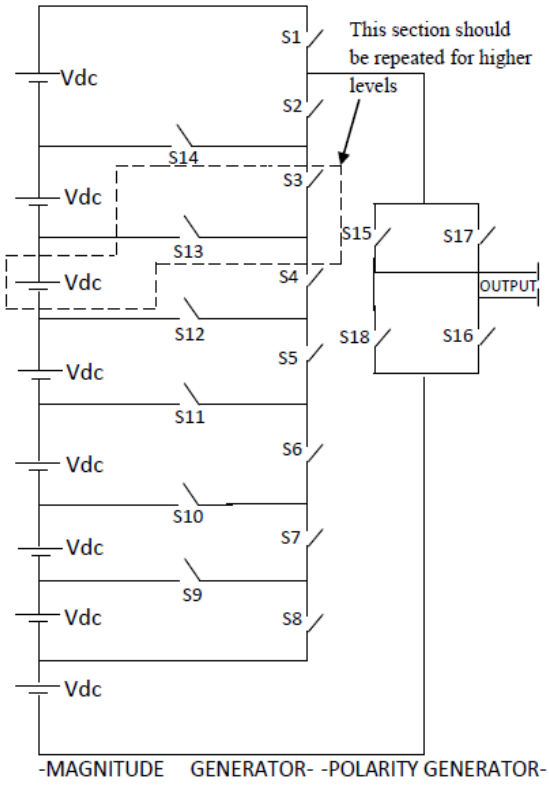


Fig.19. Two-stage Multi level inverter topology

A Hybrid Cascaded Multi Level Inverter (HCMLI) is developed in [49], which compares efficiency and design with CHBMLI. This structure utilizes a distinct level developer(sub-module) component that provides 4-level operation and is then linked to a full bridge converter to make it a hybrid model (CHBMLI) shown in figure (20). The topology with decreased switch count is extremely compact. By cascading the suggested sub-module, modularity is accomplished. In addition, the sub-module is superior to the frequently used half-bridge sub-module because it shows reduction in the number of conductive switches for all voltage levels and needs less isolation for gate drives. A novel approach to cascaded H-bridge multi-level inverter switching optimization is discussed in [50]. This topology defines one of PSO's methods called the technique of optimizing ant colony to operate CHBMLI switches. This is focused primarily on eliminating harmonics of the lower order such as harmonics of the 5th and 7th order. The suggested technique does not eliminate the higher order harmonics and can be removed by filters. Also the THD is reduced to very lower value and maintain according to the IEEE 519 standard. An ACO method is provided in [51] to eliminate the harmonics in the CHBMLI. This method focused entirely on the development and testing of the ACO algorithm. The algorithm is also applied to CHBMLI at 7-level and the output is checked for the harmonic content. The SHEPWM method is used for a seven-level inverter. By introducing ACO to the associated objective function, the optimum switching angles are found. Comparison is made in [52] of five distinct optimization techniques (GA, BEE, PSO, BSA, and DSA) to find the optimum switching angles. Furthermore, a comparative analysis was conducted simply on the basis of achieving global minimum and convergence rank. PSO is a well-known algorithm used in the SHEPWM method associated harmonic issue, so ACO is contrasted with PSO in the harmonic issue and findings demonstrate the efficacy of ACO and greater convergence rate with regard to PSO. A SHEPWM method based on a 5-level multi-level inverter called the Phase Opposition Disposition technique is described in [53]. It is intended and implemented a fresh five-level inverter topology using POD method, which is capable of generating five-level performance with less component count. No dc supply sources used in the suggested multi-level inverter are lower than standard multi-level Cascaded H-bridge inverters. Switches are switched on at low switching frequency (50Hz). Switching losses are therefore almost insignificant.

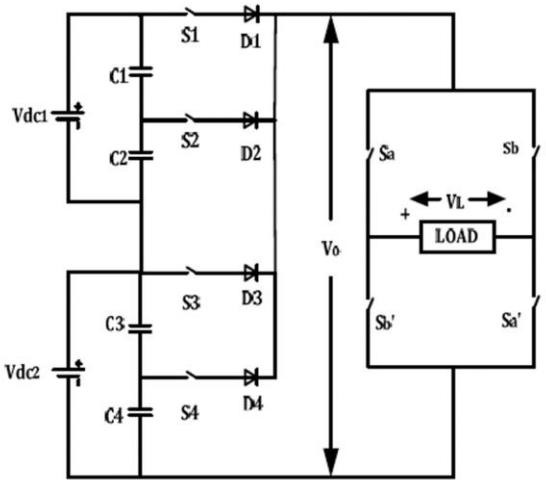


Fig.20. Modified level developer based Multi level inverter topology

A new multi-level single-phase inverter topology shown in[54]. This topology utilizes a lower switch count and can produce 13 output levels using only three DC voltage sources in the asymmetric mode of operation, which is better than some other topologies.

Fundamental frequency switching method is discussed in order to generate gate pulses. The simulation outcomes are contrasted in both operation modes.

Table: 2 Comparison of devices & components quantity for Multi Level Inverters

Inverter Configuration	Diode Clamped MLI	Flying – Capacitors MLI	Cascaded H-Bridge MLI	LD H-Bridge MLI	Modified LD H-Bridge MLI
Main switching devices	2 (m–1)	2(m–1)	2(m–1)	((m+1)/2)+4	**((m-1)/2) +4**
Main diodes	2 (m–1)	2(m–1)	2(m–1)	0	**0**
Clamping diodes	(m–1) (m–2)	**0**	**0**	0	**0**
DC bus capacitors	(m – 1)	(m – 1)	(m – 1)/2	(m-1)/2	**(m-1)/2**
Balancing Capacitors	**0**	(m–1) (m–2)/2	**0**	0	**0**

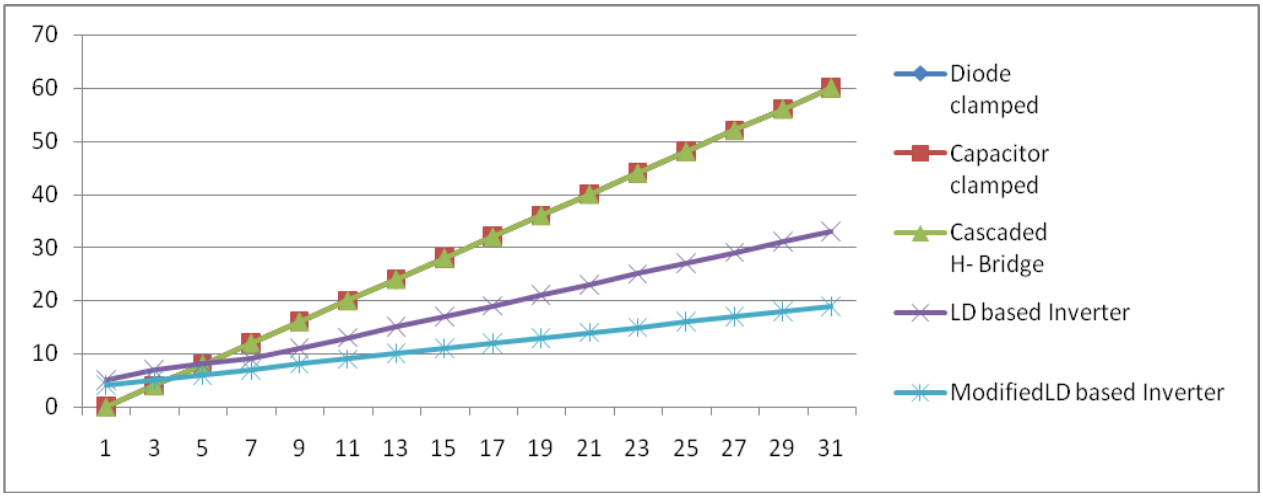


Fig: 21. Comparison of switching devices requirement for different types of multi level inverters.

IV. CONCLUSIONS

This article presents various design topologies of solar inverters. The primary focus is on designing compact and simple inverters that provide better regulation and efficiency for solar PV applications. This leads to transformer-less inverters being implemented to decrease system losses and weight. In grid interconnection applications, transformers are primarily used to provide galvanic isolation and to increase the lower voltages of PV arrays to fulfill grid voltage ratings. To boost input voltage, transformer less inverters requires boost converters, but isolation is extremely difficult with it. To prevent this problem, Z-source inverter can be used to increase input voltage and provide excellent isolation between grid and PV arrays. However, for easy operation, these topologies use 2-level and 3-level inverters. These inverters have large dv/dt, which is therefore not possible for adequate operation; the PV panel's leakage current is also a major problem owing to its stray capacitance. Multi-level inverters are implemented to minimize this issue. In their design, multi-level inverters use the large number of switches, hence the more switching losses and complex in the control circuit. Several research studies avoid further difficulties and investigate the ideal MLI design structures. While optimizing the control circuit design, research leads to the best design of MLIs with Level developer-based structure. Control schemes such as PWM, SVPWM, Phase Shifted PWMs provide significant harmonics in inverter output. Selective Harmonic Elimination PWM (SHEPWM) methods have been introduced to eliminate these harmonics, but this control technique has some constraints that it can only eliminate harmonics of lower order such as harmonics of the 5th and 7th order but not harmonics of higher order. Optimization techniques such as PSO, BEE, ACO, GA and DSA have overcome this restriction. Among these methods of optimization,

ACO has reduced THD and is best suited for controlling multi-level inverters based on the level developer. This study finally concludes that the level developer based asymmetric inverter topologies along with impedance source inverter provides good isolation and better efficiency for solar PV integrated systems. Since these topologies use very less number of switches compared to conventional topologies, therefore the switching losses and conduction losses are minimized.

A.Research Gap in the Literature

- Implementation of Z-source based Multi level transformer less inverter to provide effective galvanic isolation between AC grid and PV arrays.
- Leakage current elimination by common mode grounding practices of PV array and neutral of AC grid.
- Optimization of switching angles of Multi level inverters to reduce the constant dv/dt.
- Application soft computing techniques for reduced switch, level developer based multi level inverters to provide better voltage control.

REFERENCES

1. S. A. Azmi, G. P. Adam, K. H. Ahmed, S. J. Finney, and B. W. Williams, "Grid interfacing of multi-megawatt photovoltaic inverters," IEEE Transactions Power Electronics., Vol.28, No.6, pp. 2770–2784, June (2013).
2. Kroposki, B. B. Johnson et al., "Achieving a 100% renewable grid: operating electric power systems with extremely high levels of variable renewable energy," IEEE Power Energy Magazine, Vol. 15, No.2, pp. 61–73, April (2017).
3. H. Choi, M. Ciobotaru, M. Jang, and V. G. Agelidis, "Performance of medium-voltage dc-bus PV system architecture utilizing high-gain dc–dc converter," IEEE Transactions on Sustainable Energy, Vol. 6, No.2, pp. 464–473, April (2015).
4. T. Kerekes, E. Koutroulis, D. Séra, R. Teodorescu and M. Katsanevakis, "An optimization method for designing large PV plants," IEEE Journal of Photovoltaics, Vol.3, No. 2, pp. 814–822, April (2013).
5. B. Johnson, S. V. Dhople, A. O. Hamadeh, and P. T. Krein, "Synchronization of parallel single-phase inverters with virtual oscillator control," IEEE Transactions on Power Electronics., Vol.29, No.11, pp. 6124–6138, November (2014).
6. W.McMurray, "Fast response stepped-wave switching power converter circuit," U.S. Patent 3 581 212, May 25, (1971).
7. J. A. Dickerson and G. H. Ottaway, "Transformer less power supply with line to load isolation," U.S. Patent 3 596 369, Aug. 3, (1971).
8. R. H. Baker, "High-voltage converter circuit," U.S. Patent 4 203 151, May 13, (1980).
9. M. R. Islam, Y. G. Guo, and J. G. Zhu, "Power Converters for Medium Voltage Networks," Green Energy and Technology Series, Springer-Verlag GmbH, Heidelberg, Germany, September (2014).
10. M. R. Islam, Y. G. Guo, and J. G. Zhu, "Multilevel converters for step-up transformer-less direct grid integration of renewable generation units with medium voltage smart microgrids," in: Large Scale Renewable Power Generation: Advances in Technologies for Generation, Transmission and Storage, Springer-Verlag: Berlin Heidelberg, pp.127–149, Feb- (2014).
11. M. R. Islam, Y. G. Guo, and J. G. Zhu, "A multilevel medium-voltage inverter for step-up-transformer-less grid connection of photovoltaic power plants," IEEE J. Photovoltaics, vol. 4, no. 3, pp. 881–889, May 2014.
12. H. Wang, L. Kou, Y. F. Liu, and P. C. Sen, "A seven-switch five-level active-neutral-point-clamped converter and its optimal modulation strategy," IEEE Trans. Power Electronics., Vol.32, No.7, pp. 5146–5161, July. (2017).
13. Q. A. Le and D. C. Lee, "A novel six-level inverter topology for medium-voltage applications," IEEE Transactions on Industrial Electronics., Vol.63, No.11, pp. 7195–7203, November (2016).
14. Xiao, L. Hang, J. Mei, C. Riley, L. M. Tolbert, and B. Ozpineci, "Modular cascaded H-bridge multilevel PV inverter with distributed MPPT for grid-connected applications," IEEE Transactions Industrial Applications., Vol. 51, No. 2, pp. 1722–1731, March.–April. (2015).
15. Wang, K. Zhang, J. Xiong, Y. Xue, and W. Liu, "A coordinated compensation strategy for module-mismatch of CHB-PV systems based on improved LS-PWM and reactive power injection," IEEE Transactions Industrial Electronics., doi: 10.1109 /TIE .2018.2842789, (2018).

A. A. Stonier and B. Lehman, "An intelligent based fault tolerant system for solar fed cascaded multilevel inverters," IEEE Transactions on Energy Conversion technologies, Vol.33, No.3, pp. 1047–1057, September (2018).

16. S. Mohanty, B. Subudhi, and P. K. Ray, "A grey wolf-assisted perturb & observe MPPT algorithm for a PV system," IEEE Transactions on Energy Conversion technologies, Vol.32, No.1, pp. 340–347, March (2017).
17. Y. Mahmoud and E. F. El-Saadany, "A novel MPPT technique based on an image of PV modules," IEEE Transactions on Energy Conversion technologies, Vol.32, No.1, pp. 213–221, March (2017).
18. H. Bayat and A. Yazdani, "A power mismatch elimination strategy for an MMC-based photovoltaic system," IEEE Transactions on Energy Conversion technologies, Vol.33, No.3, pp. 1519–1528, September (2018).
19. L. Tarisciotti, P. Zanchetta, A. Watson, P. Wheeler, J. C. Clare, and S. Bifaretti, "Multiobjective modulated model predictive control for a multilevel solid-state transformer," IEEE Transactions on Industrial Applications, Vol.51, No.5, pp. 4051–4060, September–October (2015).
20. L. Wang, D. Zhang, Y. Wang, B. Wu, and H. S. Athab, "Power and voltage balance control of a novel three-phase solid-state transformer using multilevel cascaded H-bridge inverters for microgrid applications," IEEE Transactions on Power Electronics., Vol.31, No.4, pp. 3289– 3301, April (2016).
21. L. Ferreira Costa, G. De Carne, G. Buticchi, and M. Liserre,"The smart transformer: a solid-state transformer tailored to provide ancillary services to the distribution grid," IEEE transactions on Power Electronics Magazine, Vol.4, No.2, pp.56–67, June (2017).
22. S. K. Kollimalla and M. K. Mishra, "A novel adaptive P&O MPPT algorithm considering sudden changes in the irradiance," IEEE Transactions on Energy Conversion., Vol.29, No.3, pp. 602–610, Sep- (2014).
23. Z. Yang, J. Sun, X. Zha, and Y. Tang, "Power decoupling control for capacitance reduction in cascaded H-bridge converter-based regenerative motor drive systems," IEEE Transactions on Power Electronics, doi: 10.1109/ TPEL. (2018). 2818719, (2018).

A. Marzoughi, R. Burgos, D. Boroyevich, and Y. Xue, "Design and comparison of cascaded H-bridge, modular multilevel converter, and 5- L active neutral point clamped topologies for motor drive applications," IEEE Transactions on Industrial Applications., Vol. 54, No. 2, pp. 1404–1413, March –April (2018).

24. Sandeep Anand, Saikrishna Kashyap Gundlapalli, and B. G. Fernandes, "Transformer-Less Grid Feeding Current Source Inverter for Solar Photovoltaic System," IEEE transactions on industrial electronics, Vol. 61, No. 10, pp. 5334-5344, October (2014).
25. Mohammad Meraj, Syed Rahman, Atif Iqbal and Lazhar Ben-Brahim, "Common Mode Voltage Reduction in a Single-Phase Quasi Z-Source Inverter for Transformer less Grid-Connected Solar PV Applications," IEEE Journal of emerging and selected topics in power electronics, Vol.7, No.2, pp. 1352-1363, June (2019).
26. Subhendu Dutta, Dipankar Debnath and Kishore Chatterjee, "A Grid-Connected Single-Phase Transformer less Inverter Controlling Two Solar PV Arrays Operating Under Different Atmospheric Conditions," IEEE Transactions on industrial electronics, Vol.65, No.1, pp. 374-385, January (2018).
27. Sachin Jain and Vivek Agarwal, "A Single-Stage Grid Connected Inverter Topology for Solar PV Systems With Maximum Power Point Tracking," IEEE transactions on power electronics, Vol. 22, No. 5, pp. 1928-1940, September (2007).
28. Lloyd C Breazeale and Raja Ayyanar, "A Photovoltaic Array Transformer-Less Inverter with Film Capacitors and Silicon Carbide Transistors," IEEE Transactions on Power Electronics, DOI 10.1109/TPEL. (2014). 2321760,
29. Siddhartha A. Singh, Giampaolo Carli, Najath A. Azeez , and Sheldon S. Williamson, "Modeling, Design, Control, and Implementation of a Modified Z-Source Integrated PV/Grid/EV DC Charger/Inverter," IEEE transactions on industrial electronics, Vol. 65, No.6, pp. 5213-5220,June (2018).

30. Xiaoqiang Guo, Jiale Zhou, Ran He, Xiaoyu Jia, and Christian A. Rojas, " Leakage Current Attenuation of Three-Phase Cascaded Inverter for Transformer less Grid-Connected PV Systems," IEEE transactions on industrial electronics, Vol.65, Issue.1,February (2017).
31. W. Li, Y. Gu, H. Luo, W. Cui, X. He and C. Xia, "Topology review and derivation methodology of single-phase transformerless photovoltaic inverters for leakage current suppression," IEEE Transactions on Industrial Electronics., Vol. 62, No. 7, pp. 4537-4551, July (2015).
32. Hong Li, Yangbin Zeng, Bo Zhang, Trillion Q. Zheng, Ruixiang Hao, and Zhichang Yang, "An Improved H5 Topology with Low Common Mode Current for Transformer less PV Grid Connected Inverter," IEEE Transactions on Power Electronics, Vol.34, Issue.2, pp.1254 -1265 February (2019).
33. Abhijit Kadam, and Anshuman Shukla, "A Multilevel Transformer less Inverter employing Ground Connection
34. between PV Negative Terminal and Grid Neutral point", IEEE transactions on industrial electronics, Vol. 64, Issue.11, November (2017).
35. Y. Gu, W. Li, Y. Zhao, B. Yang, C. Li, and X. He, ''Transforme rless inverter with virtual DC bus concept for cost-effective grid-connected PV power systems,'' IEEE Transactions on Power Electronics., Vol. 28, No. 2, pp. 793–805, February (2013).
36. N. Vázquez, M. Rosas, C. Hernándezand, E. Vázquez, and F. J. Perez Pinal, ''A new common-mode transformer less photovoltaic inverter,'' IEEE Transactions on Industrial. Electronics., Vol.62, No. 10, pp. 6381–6391, October (2015).
37. J. F. Ardashir, M. Sabahi, S. H. Hosseini,G. B. Gharehpetian, ''A single-phase transformer less inverter with charge pump circuit concept for grid-tied PV applications,'' IEEE Transactions on Industrial Electronics, Vol.46, No. 7, pp. 5403–5415, July (2017).
38. Zhiling Liao, Chenchen Cao , Diancheng Qiu, And Changbo Xu, "Single-Phase Common-Ground-Type Transformer less PV Grid-Connected Inverters," IEEE Access, pp. 63277 – 63287, May (2019).
39. Thierry A. Meynard Henri Foch, Philippe Thomas, Jacques Courault, Roland Jakob, and Manfred Nahrstaedt, "Multicell Converters: Basic Concepts and Industry Applications", IEEE Transactions On Industrial Electronics, Vol. 49, No. 5, October (2002).
40. Gui-Jia Su, "Multilevel DC-Link Inverter", IEEE Transactions On Industry Applications, Vol. 41, No. 3, May/June (2005).
41. Gerardo Ceglia, Víctor Guzmán, Carlos Sánchez, Fernando Ibáñez, Julio Walter, and María I. Giménez, "A New Simplified Multilevel Inverter Topology for DC–AC Conversion", IEEE Transactions On Power Electronics, Vol. 21, No. 5, September (2006).
42. A.Nami, F.Zare, G.Ledwich, , A.Ghosh, F. Blaabjerg, "Comparison between Symmetrical and Asymmetrical Single Phase Multilevel Inverter with Diode-Clamped Topology", IEEE Transactions on power Electronics,Vol.13, No.2, July (2008).
43. Yu Liu, Hoon Hong, and Alex Q. Huang, "Real-Time Algorithm for Minimizing THD in Multilevel Inverters with Unequal or Varying Voltage Steps under Staircase Modulation" IEEE Transactions On Industrial Electronics, Vol. 56, No. 6, June (2009).
44. H. Taghizadeh and M. Tarafdar Hagh, "Harmonic Elimination of Cascade Multilevel Inverters with Nonequal DC Sources Using Particle Swarm Optimization", IEEE Transactions on Industrial Electronics, Vol. 57, No. 11, November (2010).
45. Ayoub Kavousi, Behrooz Vahidi, Reza Salehi, Mohammad Kazem Bakhshizadeh, Naeem Farokhnia and S. Hamid Fathi,"Application of the Bee Algorithm for elective Harmonic Elimination Strategy in Multilevel Inverters", IEEE Transactions On Power Electronics, Vol. 27, No. 4, April (2012).
46. Javad Ebrahimi, Ebrahim Babaei and Gevorg B. Gharehpetian, "A New Multilevel Converter Topology with Reduced Number of Power Electronic Components", IEEE Transactions On Industrial Electronics, Vol. 59, No. 2, February (2012).
47. Arpan Hota, Sachin Jain, and Vivek Agarwal, "An Optimized Three Phase Multilevel Inverter Topology with Separate Level and Phase Sequence Generation Part", IEEE Transactions on Power Electronics, Vol. 23, No. 6, March (2014).
48. Sze Sing Lee, Michail Sidorov, Chee Shen Lim, Nik Rumzi Nik Idris and Yeh En Heng, "Hybrid Cascaded Multilevel Inverter (HCMLI) with Improved Symmetrical 4-Level Submodule", IEEE Transactions On Power Electronics, Vol.16, No.4, Nov-(2016).
49. Sarika D Patil, Sumant G Kadwane, Snehal P Gawande,"Ant colony optimization applied to selective harmonic elimination in multilevel inverters", 2nd International Conference on Applied and Theoretical Computing and Communication Technology, (2016), Page No:148-153.
50. Mahmoud Babaei and Hassan Rastegar "Selective Harmonic Elimination PWM Using Ant Colony Optimization", 25th Iranian Conference on Electrical Engineering (lCEE2017), Page No: 347-354.
51. Sourabh Kundu , Arka Deb Burman, Santu K.Giri, Sarbani Mukherjee, Subrata Banerjee, "Comparative study between different optimization techniques for finding precise switching angle for SHE-PWM of three-phase seven-level cascaded H-bridge inverter",IET Power Electron. The Institution of Engineering and Technology (2017).
52. P.Vishnuvardhan Reddy, L.Bangar Raju "Design And Analysis Of Five Level Inverter Using Pod Pwm Technique", International Journal Of Professional Engineering Studies, Volume .8, Issue 4, May (2017).
53. Marif Daula Siddique, Asif Mustafa and Adil Sarwar, "Single Phase Symmetrical and Asymmetrical Design of Multilevel Inverter Topology with Reduced Number of Switches", IEEE Transactions Industrial Electronics, Vol. 18, No.8, (2018).

AUTHORS PROFILE

Devineni Gireesh Kumar received his B.Tech degree from JNTU, Anantapur in 2009 and M.Tech degree from SRM University in 2011. He is currently working towards his Ph.D in Electrical Engineering in the school of Electronics & Electrical Engineering at Lovely Professional University, Jalandhar, Punjab, India. His research interests include solar PV inverters, Multilevel converters, Electric Vehicle Drives

Dr. Aman Ganesh Received his Ph.D degree from NIT Kurukshetra. He is currently working as Professor in school of Electronics & Electrical Engineering at Lovely Professional University. Jalandhar, Punjab, India. His research areas of interests include Coordinated control of STATCOM and PSS, Standalone and Grid connected PV Solar System.