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Simulation and Performance Evaluation of In Ga P/In Ga As/Ga As Dual Channel HEMT

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Abstract: ***An InGaP/InGaAs/GaAs dual channel High Electron Mobility transistor (HEMT) with three δ doped layers with different doping densities is modeled and simulated in this paper by using two dimensional ATLAS simulation package from Silvaco software. Different DC performances (Drain characteristic and Transfer characteristics) at various voltage levels are analyzed and results are compared by taking the gate length of 500nm and 800nm at two different temperature levels (250k and 300k) to determine the efficiency of the device for high speed digital device applications. The paper describes the effect of parasitic access resistance on device gate length and effect of mobility by varying temperature. High drain current drivability, large carrier densities and better saturation characteristics are realized because of the inclusion of InGaAs channel instead of GaAs DC structure and schottky behavior of InGaP layer. The studied double channel HEMT with proper dimensions and accurate doping profile makes it a promising device for high performance electronics device applications***.

Keywords: Atlas, delta doped sheets, InGaP, schottky.

I. INTRODUCTION

With the fast progress in fabrication technologies, many devices made from compound semiconductor materials such as field effect transistors (FETs), hetero junction field effect transistors (HBTs) , many switching devices and HEMTs have been suggested [1]-[5]. The speed of the devices made from compound semiconductor materials extensively increases due to high mobility of carrier. Hence these devices can exhibit higher frequencies of operation. However the device performance can be increased further by increasing average velocity of electrons, which is achieved by scaling down the gate length. Unfortunately, the presence of parallel conductance in wide-band gap dopant layers, directs to abrupt peak in transconductance, which restricts the device performance and current driving capability. Therefore, to prevail the drawbacks of conventional HEMTs, dual channel HEMT has been suggested [6]-[9].

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InGaP, InGaAs and its analogous materials have excellent properties that build them as promising candidate for high speed, low noise and low power applications. InGaAs is a noble choice for channel layer because of its small band gap and low effective mass. As a result high mobility and peak velocity can be achieved [10]-[11]. This paper emphasizes on the study of InGaP/InGaAs/GaAs dual channel HEMT with three δ-doped layers by taking gate length of 500nm and 800nm at temperature 250k and 300k. This paper comprises of three sections. Section II deals with model description followed by results and description in section III. Conclusion is described in section IV.

II. MODEL DETAIL AND THEORETICAL CONSIDERATIONS

The structural representation of InGaP/InGaAs/GaAs dual channel HEMT is shown in fig 1. The model of the device is established on a 4000Å semi insulating (S.I) GaAs substrate, 450 Å un-doped $In_{0.49}Ga_{0.51}P$ buffer layer, 20 Å δ doped sheet 3 with doping density $\delta_3(n^+)$ of $1\times10^{12}\ cm^{-2}$,50 Å un-doped $In_{0.49}Ga_{0.51}P$ spacer layer, 100 Å un-doped $In_{0.2}Ga_{0.8}As$ channel layer, 40 Å un-doped GaAs spacer layer , 20 Å δ doped sheet 2 with doping density $\delta_2(n^+)$ of $2\times10^{12}\ cm^{-2}$, 40 Å un-doped GaAs spacer layer, 100 Å un-doped $In_{0.2}Ga_{0.8}As$ channel layer, 50 Å $In_{0.49}Ga_{0.51}P$ un-doped spacer layer, 20 Å δ doped sheet 1 with doping density $\delta_1(n^+)$ of $5\times10^{12}\ cm^{-2}$, 160 Å un-doped $In_{0.49}Ga_{0.51}P$ Schottky layer and 300 Å GaAs cap layer with doping density n^+ of $3\times10^{18}\ cm^{-3}$.

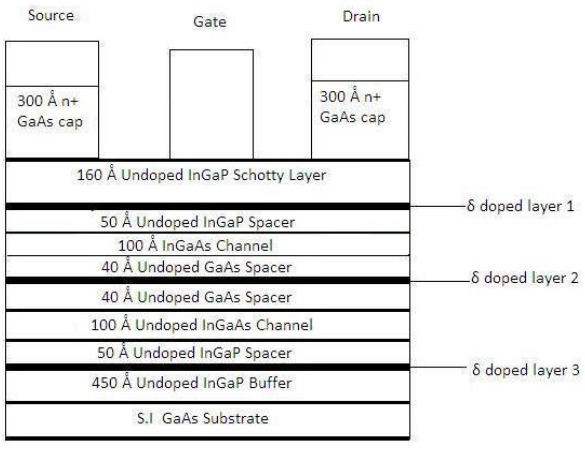

Fig 1. Schematic crossection of InGaP/InGaAs/GaAs HEMT

The three delta doping layers as carrier supplier are included into the structure to provide even distribution of carrier throughout the channel layer and hence outputs in high current densities [12].
GaAs cap layer is used to minimize the contact resistance of the drain and source contacts, so that the device can be protected from oxidation. Spacer layer is present to reduce scattering effect and hence improving the electron mobility. InGaP schottky layer is used to provide schottky contact between semiconductor material and gate metal to have low leakage current and better carrier imprisonment. Some physical parameters employed throughout the simulation process are given below in a tabular form.

Table 1. Physical parameters for simulation

Parameter	Symbol	Value	Reference
$In_{0.49}Ga_{0.51}P$ energy gap(ev)	E_g	1.92	[13]
$In_{0.2}Ga_{0.8}As$ energy gap(ev)	E_g	0.75	[13]
GaAs energy gap(ev)	E_g	1.42	[14]
Saturation velocity (cm/s) $In_{0.49}Ga_{0.51}P$	γ	1.0×10^6	[15]
Saturation velocity(cm/s) $In_{0.2}Ga_{0.8}As$	γ	7.7×10^6	[16]
Saturation velocity(cm/s) GaAs	γ	7.7×10^6	[16]
Low field mobility GaAs(cm^2/Vs)	μ	1000	[16]
Low fieldmobility InGaAs(cm^2/Vs)	μ	6000	[16]

III. RESULTS AND ANALYSIS

To observe the different device performances, different characteristics are obtained. The energy band diagram showing valence band and conduction band is shown in fig 2. The band gap energy is found to be 1.9 eV for InGaP, 1.1 eV for InGaAs and 1.4 eV for GaAs which is same as theoretical value.

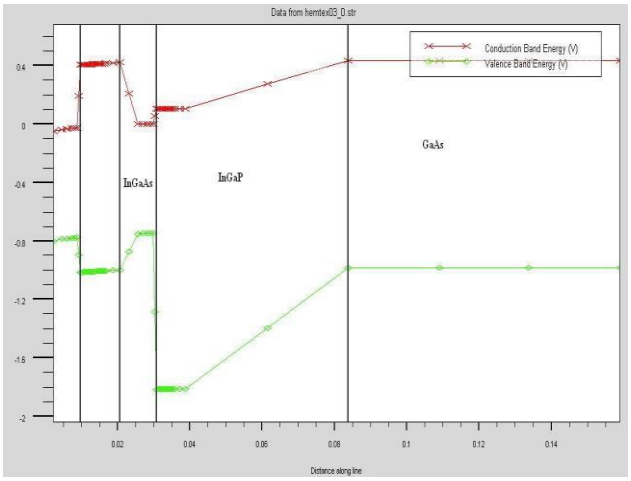

Fig 2. Energy Band diagram of dual channel HEMT

Fig 3 and fig 4 reveal drain characteristics which is drain current versus drain source voltage (I_D vs V_{DS}) at 500nm and 800nm gate length of InGaP/InGaAs/GaAs dual channel HEMT at 250k and 300k respectively. From fig 3, it is observed that, maximum drain saturation current I_D at fixed gate source voltage V_{GS} of 1v is 470 mA/mm and 390 mA/mm for gate length of 500nm and 800nm respectively at temperature of 250k. The maximum drain current I_D at constant V_{GS} of 1v is 360 mA/mm and 297 mA/mm for gate length of 500nm and 800nm respectively at temperature of 300k as shown in fig 4. It is observed that when gate length is reduced, parasitic access resistances are also reduced, as a result performance becomes better.

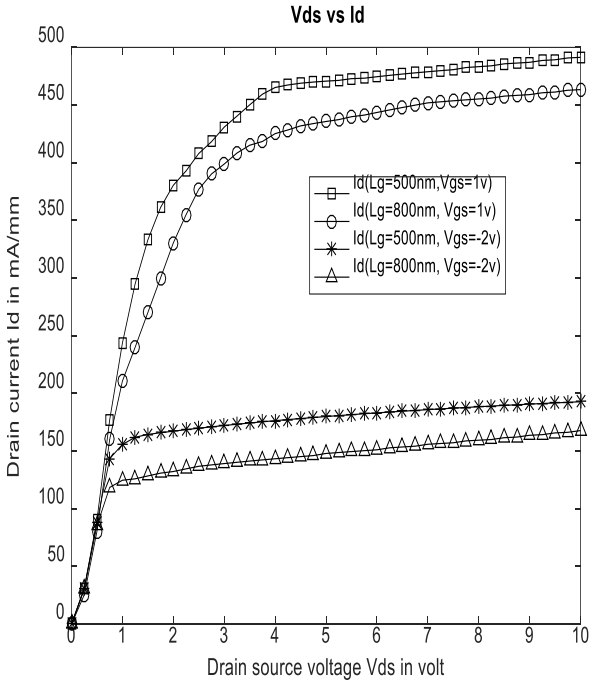

Fig 3. Drain characteristics of dual channel HEMT at 250k

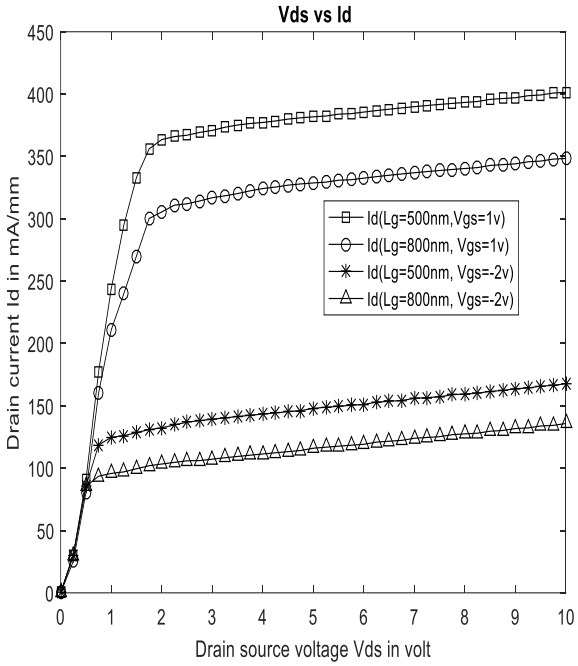

Fig 4. Drain characteristics of dual channel HEMT at 300k

Fig 5 and fig 6 shows the response between drain current and gate source voltage (I_D vs V_{GS}) for 500nm and 800nm gate length at 250k and 300k respectively. At temperature 250k, the maximum drain currents obtained are about 693 mA/mm and 597 mA/mm at V_{DS} 3v for gate length of 500nm and 800nm respectively as presented in fig 5. Fig 6 conveys, at temperature 300k, drain currents are about 627 mA/mm and 542 mA/mm at V_{DS} 3v for gate length of 500nm and 800nm respectively.

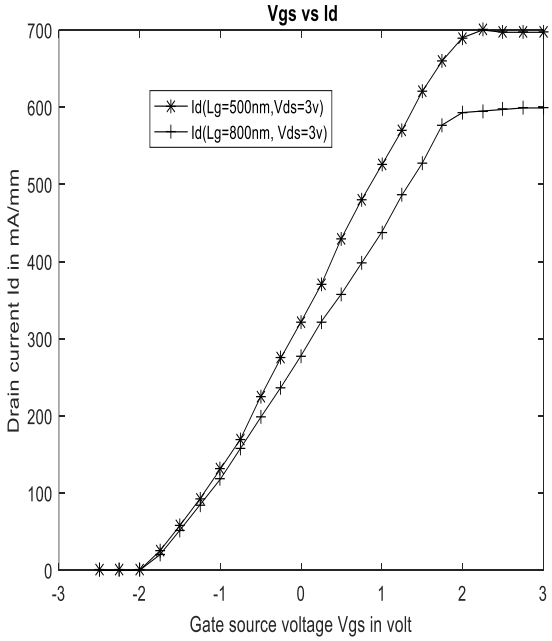

Fig 5.Transfer Characteristics of dual channel HEMT at 250k

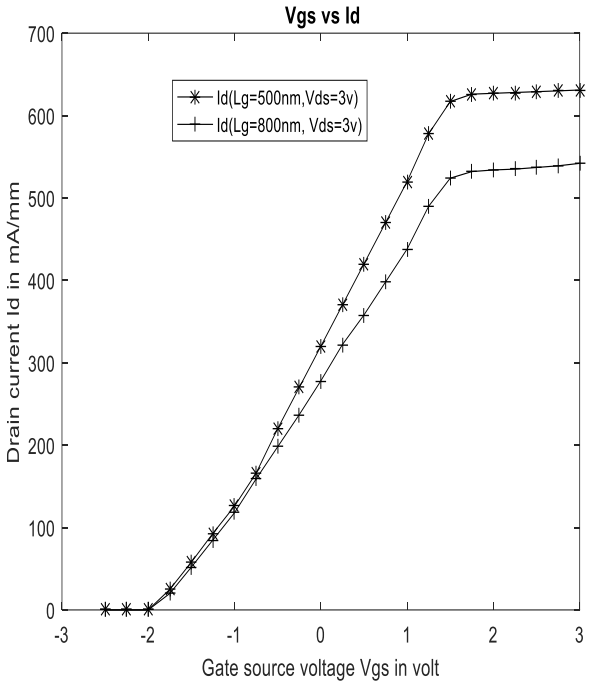

Fig 6. Transfer Characteristics of dual channel HEMT at 300k

There-fore it is observed that, due to the increase in temperature, mobility gradually degrades, which affects the device performance.

IV. CONCLUSION

The DC characteristics of InGaP/InGaAs/GaAs dual channel HEMT were investigated by taking gate length of 500nm and 800nm at two different temperature levels and results are compared. Simulations are done by using ATLAS simulator from silvaco. It is observed that, when gate length is reduced, device current is enhanced because of reduction in parasitic access resistances. It is also found that when temperature is increased, corresponding mobility of the device degrades. Thus the simulated device is a promising one for high voltage and high power applications.

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