International Journal of Engineering and Advanced Technology (IJEAT)
ISSN: 2249-8958 (Online), Volume-9 Issue-1, October, 2019

Design and Performance Analysis of Low Power High Speed 4x4 CNTFET Binary Content Addressable Memory Array

A. Gangadhar, K. Babulu

Abstract: ***In this paper, Carbon Nanotube Field Effect Transistor (CNTFET) based Binary Content Addressable Memory (BCAM) array is presented. The CAM array comprises of address decoders, encoders, data drivers and BCAM cells. Performance analysis is carried for 4X4 BCAM array. Each BCAM cell is designed based on adiabatic logic with optimum CNTFET parameter for low power and high speed applications. The performance of proposed BCAM array is analyzed for average power, peak power and search delay. The proposed CNTFET based BCAM array show improvement in the performance compared to that of complementary metal oxide semiconductor (CMOS) based BCAM array. The average power and peak power of the proposed 4x4 CNTFET BCAM array are in the range of micro watt (µW) while it is in the range of milli watt (mW) for CMOS based BCAM array. The search delay of the proposed 4X4 CNTFET BCAM array is improved by 32.3% compared to that of CMOS based BCAM array. All simulations are conducted for both CNTFET and CMOS based BCAM cells, BCAM array in HSPICE at 32 nm technology.***

Keywords: carbon nanotube field effect transistor, 4x4 content addressable memory array, optimum parameter set.

I. INTRODUCTION

Content Addressable Memories (CAM) have become more popular in applications like parallel search and fast look up tables. The main functions of CAM are to store the data and to locate the address where it has been stored in the memory in less time. The CAM has the ability to search the data in one clock cycle. The simplest form of CAM is Binary CAM (BCAM). The applications of CAMs include packet classifiers, look-up table, network routers and cache controllers. CAM cell has similar structure to that of (Static Random Access Memory) SRAM except additional circuitry for comparison of data. Usually the CAM cells are arranged in an array form for storing the data and to search the data. The stored information is structured as rows and columns in the form of CAM cells. The depth and width of the CAM array is represented by number of rows and columns respectively. The main components of CAM array are encoder, decoder, data drivers and individual BCAM cells which are arranged in row and column pattern [1]. In CAM array the search operation takes place in parallel. This would make the search operation incredibly quick. Post-processing of CAM inputs is extremely application-specific, which is either a match or a mismatch. [2- 4]. The problem of parallel search is high power consumption. Numerous efforts have been made to improve CAM's energy efficiency.

The general architecture of 4x4 BCAM array is shown in Figure 1. It can store four data words and each word is of 4-bit length. Assume the first row from top of the array contains the data word as "0110". The data word stored in second row is 1011. The data word stored in third row is 0100. The data word contained by the fourth row is 1110. Match lines (ML) are used to indicate whether the data match has been found or not. Assume the search data is 0100. After comparison with all locations, it is found in third row in the array. The corresponding match line (ML_1) is highlighted and is shown in Figure1.

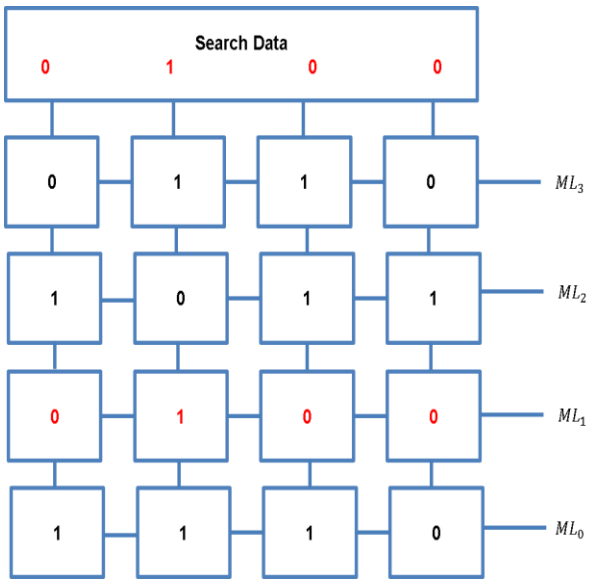

Fig.1 General 4x4 BCAM Array

The search power is the prime sources of power consumption in CAM cells/ array [5-12]. Several attempts were made to decrease consumption of power in CAM cells/ array The output is set to low value by using NAND gates when mismatch happens.

Revised Manuscript Received on October 30, 2019.
* Correspondence Author
A.Gangadhar*, Research Scholar, ECE Department, JNTUK, Kakinda, India. Email: gangadhar.ece@jntukucev.ac.in
K.Babulu, Professor, ECE department, JNTUK, Kakinda, India. Email: kapbbl@gmail.com

While this method saves energy, but increase the impedance of match line and thus slows down the operation of comparison [5]. Therefore, for workloads needing greater velocity, NOR type cells are generally preferred. A method for predicting the mismatch and preventing the line from charging to its complete swing is presented [6]. Low swing search lines [7] were suggested to save the power of the search line. Low swing search lines with higher capacitive loads on global search lines and complete swing on local search lines with reduced capacitive loads. A pipeline search scheme is presented to reduce the power consumption that originally activates fewer parts of the CAM and eventually activates only the matching parts [8]. To tackle the pre-charge power consumption, a free pre-charge free design has been proposed [9]. A model that decreases the leakage power in two novel ternary CAM (TCAM) cells suggested by CAM [10]. By decreasing the capacitance on the match line, power consumption can be reduced [11]. To reduce the power consumption, a current –race scheme is presented unlike traditional pre-charging [12]. There are several architectures available in the literature, but all accessible CAM architectures are inefficient owing to full memory access in each search procedure. [13-20].

At nanoscale CMOS faces challenges like short-channel effects, leakage current and source-to drain tunneling. Because of the high mobility of electrons movement near ballistic transport and high driving capacity and smaller area, the CNTFETs are become promising alternate for CMOS technology especially when the device scaled at nanometer range. The authors [21-26] revealed that CNTFET outperforms compared to CMOS for both circuits and transmission lines. The positive feedback logic shown superior performance in the design of BCAM cells and other circuits needed to realize the BCAM array such as priority encoder, decoder and other logic gates [27, 28].

In this paper, adiabatic logic based CNTFET BCAM cell and its 4x4 BCAM array are proposed. The optimized CNTFET is used for the design of CAM cells. The CNTFET is optimized in tube count, chirality vector, pitch value, oxide thickness and type of oxide material. The type of adiabatic logic used in the design of CAM cell is improved positive feedback adiabatic logic (IPFAL). The integration of optimized CNTFET and IPFAL has improved the performance of BCAM cell/ array. The remainder of document rest organized as follows. Section II presents the proposed CNTFET based BCAM cell and BCAM array. Section III presents the simulation results and its performance analysis. The performance of proposed BCAM and BCAM array is compared to that of CMOS based BCAM cell/ array. Section IV concludes the paper.

II. PROPOSED CNTFET –IPFAL BCAM CELL AND 4X4 BCAM ARRAY

In this section, the proposed CNTFET based BCAM cell circuitry and their operation with respect to search operation is presented. The circuit diagrams of proposed CNTET IPFAL BCAM cell is shown in Fig 2. The adiabatic logic is integrated with CNTFET to improve the performance of the BCAM cells. Here, Power Clock (PC) signal acts as a Word Line (WL). The PC is considered as a sinusoidal signal. The search operation in CNTFET based IPFAL is as follows. Input A acts search data. The stored values are considered as in B and $\bar{B}$. If the input data A matches with the values of B, then ML goes high otherwise it is at low logic level. The power and delay analysis of CNTFET with various CNTFET parameters such as tube count, chirality vector, pitch value, oxide thickness and type of oxide material is performed. The analysis yielded optimal parameter set for CNTFET to achieve low power consumption. The same parameter set is used for simulation of the CNTFET based BCAM cells and BCAM array. The optimal CNTFET parameter set is given in Table I.

Table I: CNTFET parameters for Low power applications

S.No.	CNTFET Parameter	Value
1	Tube count	3
2	Chirality Vector	(10,0)
3	Pitch Value	5
4	Oxide Thickness	9
5	Oxide Material	$Si_3N_4(K_{ox} = 7)$

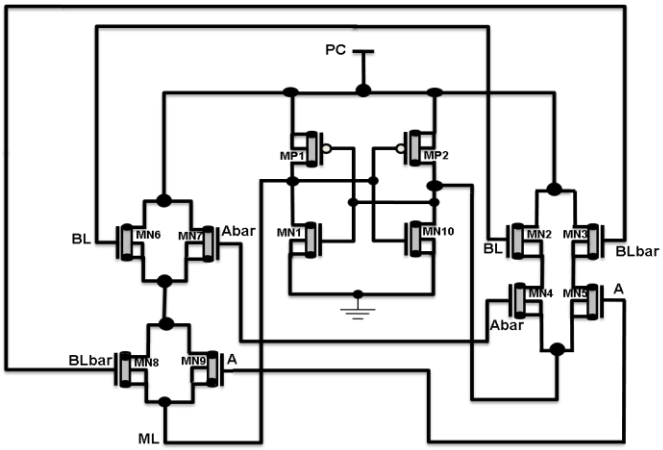

Fig.2: CNTFET based IPFAL CAM cell

A 4x4 BCAM array comprises of BCAM cells arranged in rows and columns, encoder and decoder. If the search data word is equal to stored data word, the respective ML will be highlighted. For example, if the search data word is the same as the stored data word, then the corresponding ML is low and all other ML lines remain at high logic level. The block diagram of 4x4 CNTET-IPAL-BCAM array is shown in Fig.3

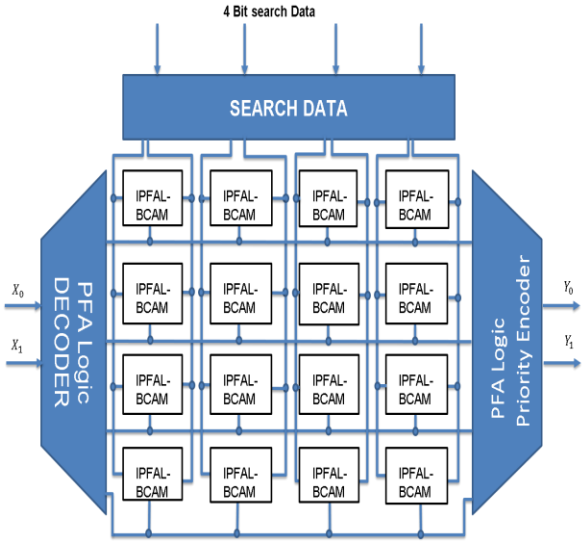

Fig. 3 Proposed 4X4 CNTFET based BCAM array

III. RESULT ANALYSIS

This section presents the output waveforms and performance of the proposed CNTFET based 4x4 BCAM array is presented. The performance of BCAM array in terms of average power, peak power and search delay is presented. The simulations are performed using HSPICE. The power clock signal is a sinusoidal signal of amplitude 0.7 V and frequency 125 MHz. The logic 1 is considered as 0.7 V and logic 0 is considered as 0V. The technology used CMOS and CNTFET is 32nm Technology. The proposed CNTFET based BCAM array performance is compared to that of CMOS technology based BCAM. The proposed CNTFET-IPFAL BCAM show better performance compared to that of CMOS-IPFAL BCAM cell. The values of average power and search delay is listed in Table II. The values of average power, peak power and search delay of 4x4 BCAM array are listed in Table III. The output waveforms of PFAL logic gates and encoder are shown through Fig.7 to Fig.10.

Table II: The power and delay analysis of proposed BCAM Cell

S.No.	Type of the Binary CAM cell	Power and Delay values of the proposed binary CAM Cell	
		Average Power	Search Delay
1	CNTFET	0.17nW	0.69nS
2	CMOS	1.86 µW	1.57 nS

Table III: The power and delay analysis of proposed BCAM array

S.No.	Type of the Binary	Power and Delay values of the proposed binary CAM Array		
		CAM cell Array	Average Power	Peak Power	Search Delay
1	CNTFET	1.5 µW	8.1 µW	1.8 nS
2	CMOS	0.14 mW	1.6 mW	2.66 nS

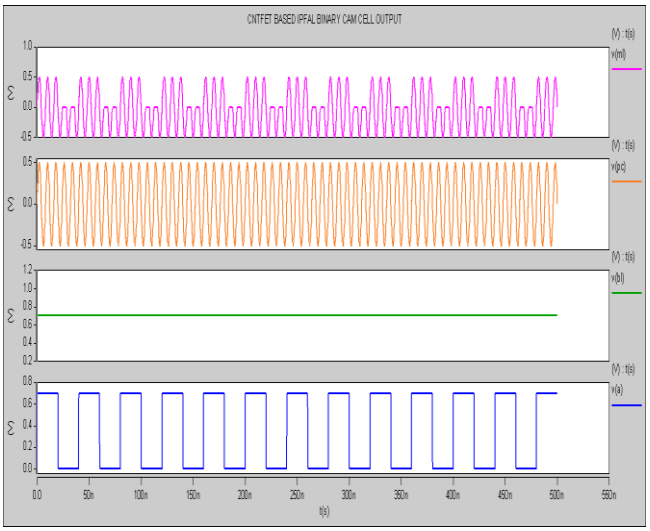

Fig.4 CNTFET based IFPAL - BCAM Cell output

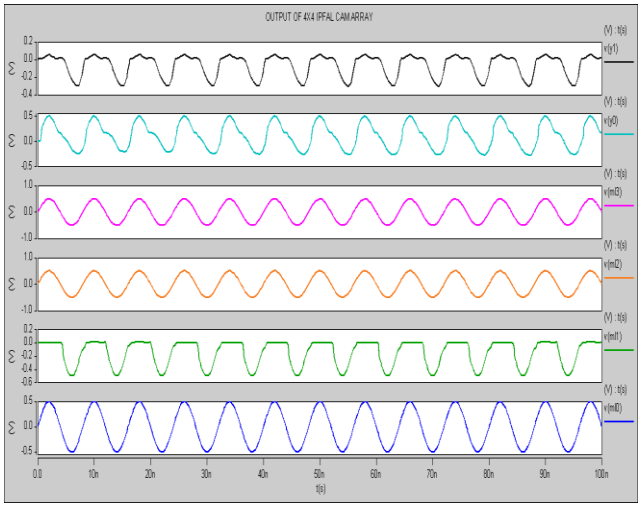

Fig.5 CNTFET based IFPAL - BCAM array output

In the proposed BCAM cell, if search data matches with stored data then the ML line follows power clock otherwise the ML line is at low and is shown in Fig. 4. It assumed that the stored data is 1010 and it is available in third row of BCAM array. When we give 1010 as search data only ML_1 line is at low remaining all ML lines follow power clock and this shown in Fig.5.

IV. CONCLUSIONS

In this paper, 4x4 CNTFET based IPFAL-BCAM array is presented. The proposed BCAM array is based on the positive feedback adiabatic logic array.

The simulation results show an improvement in average power, peak power and search delay of proposed BCAM cells compared to that of CMOS-based BCAM array. The average power and peak power of the proposed 4x4 CNTFET BCAM array are in the range of μW while the range of values for CMOS based BCAM array are mW. The search delay of the proposed 4x4 CNTFET BCAM array is improved by 32.3% compared to that of CMOS based BCAM array. All simulations are performed in HSPICE at 32 nm technology for both CMOS and CNTFET.

REFERENCES

1. K. Pagiamtzis and A. Sheikholeslami, "A low-power content addressable memory (CAM) using pipelined hierarchical search scheme", IEEE Journal of Solid-State Circuits, vol. 39, no. 9, pp. 1512-1519, 2004.
2. Kostas Pagiamtzis and Kostas Pagiamtzis, "Content-Addressable Memory (CAM) Circuits and Architectures: A Tutorial and Survey", IEEE Journal of Solid-State Circuits, Vol. 41, No. 3, pp. 712-727, March 2006.
3. Kittur, H.M.; Zackriya, V.M. Precharge-Free, "Low-Power Content-Addressable Memory", IEEE Transactions on Very Large Scale Integration Systems, Vol.24, pp.2614–2621, 2016.
4. Chen, T.S, Lee, D.Y, Liu, T.T., Wu, A.Y. "Dynamic Reconfigurable Ternary Content Addressable Memory for Open Flow-Compliant Low-Power Packet Processing", IEEE Transactions on Circuits Systems. Vol.63, pp.1661–1672, 2016.
5. Zukowski, C. and Wang, S.-Y. "Use of selective precharge for low-power content-addressable memories", In Proceedings of the 1997 IEEE International Symposium on Circuits and Systems. Circuits and Systems in the Information Age ISCAS'97, pp. 1788–1791, Hong Kong, China, 12 June 1997.
6. Zackriya M. and Kittur, H.M. "Content Addressable Memory—Early predict and terminate precharge of Match-Line Content Addressable Memory", IEEE Transactions on Very Large Scale Integration Systems, Vol.25, pp.385–387, 2016.
7. Yang, B.D.; Lee, Y.K.; Sung, S.W.; Min, J.J.; Oh, J.M.; Kang, H.J. "A low power content addressable memory using low swing search lines", IEEE Transactions on Circuits Systems, Vol.58, pp.2849–2858, 2011.
8. Pagiamtzis, K. and Sheikholeslami, A. "A low-power content-addressable memory (CAM) using pipelined hierarchical search scheme", IEEE Journal of Solid-State Circuits Vol.39,pp.1512–1519, 2004.
9. Mahendra, T.V.; Mishra, S.; Dandapat, A. "Self-Controlled High-Performance Precharge-Free Content-Addressable Memory", IEEE Transactions on Very Large Scale Integration Systems, vol.25, pp.2388–2392, 2017.
10. Mohan, N. and Sachdev, M. "Low-Leakage Storage Cells for Ternary Content", IEEE Transactions on Very Large Scale Integration Systems, Vol.17, no.5, pp.604-612, 2009.
11. Mohan, N.; Sachdev, M. Low-capacitance and charge-shared match lines for low-energy high-performance TCAMs. IEEE J. Solid-State Circuits 2007, 42, 2054–2060.
12. Arsovski, I.; Chandler, T.; Sheikholeslami, A. A ternary content-addressable memory (TCAM) based on 4T static storage and including a current-race sensing scheme. IEEE J. Solid-State Circuits 2003, 38, 155–158.
13. Irfan, M.; Ullah and Z. G-AETCAM, "Gate-Based Area-Efficient Ternary Content-Addressable Memory on FPGA", IEEE Access, Vol.5, pp.20785–20790, 2017.
14. Ullah, Z. "LH-CAM: Logic-Based Higher Performance Binary CAM Architecture on FPGA", IEEE Embedded Systems Letters, Vol.9, no.2, pp.29–32, 2017.
15. Ullah, Z.; Jaiswal, M.K.; Cheung, R.C. Z-TCAM: An SRAM-based architecture for TCAM. IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 2015, 23, 402–406.
16. Ullah, I.; Ullah, Z.; Lee, J.A. EE-TCAM: An Energy-Efficient SRAM-Based TCAM on FPGA. Electronics 2018, 7, 186.
17. Ullah, Z.; Jaiswal, M.K.; Cheung, R.C. E-TCAM: An efficient SRAM-based architecture for TCAM. Circuits Syst. Signal Process. 2014, 33, 3123–3144.
18. Ullah, I.; Ullah, Z.; Lee, J.A. Efficient TCAM design based on multi pumping-enabled multi ported SRAM on FPGA. IEEE Access 2018, 6, 19940–19947.
19. Ullah, I.; Ullah, Z.; Afzaal, U.; Lee, J.-A. DURE: An Energy-and Resource-Efficient TCAM Architecture for FPGAs with Dynamic Updates. IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 2019.
20. Yu,Y.; Belazzougui,D.; Qian,C.; Zhang, Q. Memory-Efficient and Ultra-Fast Network Lookup and Forwarding Using Othello Hashing. IEEE/ACM Transactions Networks. 2018, 26, 1151–1164.
21. C.Venkataiah et.al. "Analytical Study of Bundled MWCNT and Edged-MLGNR Interconnects: Impact on Propagation Delay and Area", IEEE Transactions on Nanotechnology, 2019. DOI 10.1109/TNANO.2019.2920679.
22. C.Venkataiah, K. Satyaprasad, T. Jayachandra Prasad, "FDTD algorithm to achieve absolute stability in performance analysis of SWCNT interconnects", Journal of computational electronics, 2018. DOI: 10.1007/s10825-017-1125-1.
23. C.Venkataiah, K. Satyaprasad, T. Jayachandra Prasad, "Insertion of optimal number of repeaters in pipelined nano interconnects for transient delay minimization", Circuit systems and signal processing, 2019. DOI: 10.1007/s00034-018-0876-7.
24. C.Venkataiah, K. Satyaprasad, T. Jayachandra Prasad, "Signal integrity analysis for coupled SWCNT interconnects using stable recursive algorithm", Microelectronics Journal, volume. 74, pp. 13-23, 2018.
25. C.Venkataiah, K. Satyaprasad, T. Jayachandra Prasad, "Crosstalk induced performance analysis of single walled carbon nanotube interconnects using stable finite difference time domain model", Journal of nanoelectronics and optoelectronics, Vol. 12, pp. 1-10, 2017.
26. C.V.S. Reddy, C.Venkataiah, V.R.Kumar, S.Maheswaram, N. Jains, S.D. Gupta and S.K. Manhas "Design and simulation of CNT based nano-transistor for greenhouse gas detection", Journal of nanoelectronics and optoelectronics, Vol. 12, pp. 1-9, 2017.
27. D. Jothi and R.Siva Kumar, "D. Jothi , R.Siva Kumar, "Design and Analysis of Power Efficient Binary Content Addressable Memory (PEBCAM) Core Cells", Circuits, Systems and signal processing"Vol.37, No. 4, pp 1422–1451, April 2018.
28. Thockchom Birjit Singha ; Shruti Konwar ; Soumik Roy ; Reginald H. Vanlalchaka, "Power efficient priority encoder and decoder" International Conference on Computer Communication and Informatics, Coimbatore, India 3-5 Jan. 2014.

AUTHORS PROFILE

A.Gangadhar completed his B.Tech and M.Tech in 2005 and 2010 respectively. Presently, he is working as an Assistant Professor in ECE in UCEV, JNTUK Vizianagaram, India. He is a research scholar at JNTU Kakinada. His research interests include VLSI Design and Embedded System Design.

Dr.K.Babulu has received Ph.D in VLSI from JNTUA, India. Presently, he is working as Professor in the department of ECE, UCEK, JNTU College of Engineering, Kakinada. His research interests include VLSI Design, Embedded System Design, ASIC Design and PLD design.