Low Noise Amplifier Design of CMOS Inductorless with Noise Cancellation Technique

Mahesh Mudavath, K Hari Kishore, Sanjay Madupu, Prashanth Chittireddy, Srinivas Bhukya

Abstract- This article presents the Low Noise Amplifier (LNA) design of CMOS Inductorless Noise cancellation (NC) technique for portable wireless receivers. An Inductorless CMOS LNA for multi-standard wireless applications with less area, single-chip is presented. This NC technique is used to cancel out the noise involvement in LNAs at the output of matching device. The proposed Inductorless CMOS LNA designed in a CMOS 45nm GPDK technology process. The simulated results within the frequency range of 1.04GHz-1.8GHz are considered here. The maximum gain has achieved 20dB @ 1.04GHz, 23dB @ 1.8GHz and a low NF of 1.2dB @ 1.04GHz, 0.6dB @ 1.8GHz. The input and output reflection coefficients are obtained as less than -10dB it is desirable value to fit in this LNA.

Keywords: An Inductorless; Noise Cancellation Technique; Low Noise Amplifier; Noise Figure.

I. INTRODUCTION

The rising demand for high data rates and high speed in wireless communication systems is increasing the necessities on the transceiver front-ends, as they are pushed to exploit more and more extensive bands at higher frequencies, faster data transfer rates and wider bandwidths [1]. The work in this proposed article is focused on design and analysis of CMOS RF receiver front-ends composed of LNAs for wireless applications operating at microwave frequencies [2]. The particular case of Wireless standards the 1GHz-1.8GHz industrial, scientific and medical (ISM) band normally leads to RFICs utilizing LNA’s circuit design with numerous inductors [3]. Because of that reason those bulky spiral inductors effect of costly RFIC. So to avoiding them is enormously a cost effective approach. On the contrary, low power inductor less CMOS LNAs may not offer the less NF of those inductor components based counterparts. But an inductorless CMOS LNAs with NC technique should offer a high gain, low noise figure, as well as significantly reduced silicon chip area [4] [5]. An Inductorless LNAs typically suffer from meager noise performance, mostly due to the high noise involvement of the matching device. This NC technique is used to cancel out the noise involvement in LNAs [6]. These techniques are frequently explained with the help of the block diagram shown in Fig. 1 [7]. Here the input signal coming from a source of antenna terminal with internal impedance $Rs$ is concurrently fed to a matching of CS amplifier and CG amplifier.

Fig. 1 A block diagram of NC technique

II. PRINCIPLE OF NC TECHNIQUE

The proposed LNA includes a CS & CG amplifier stages [4] [Fig. 2 & Fig.3 follows], The NC technique is adopted to decrease the noise involvement of the CG amplifier [8]. Compared with CS, in the interim, the power gain & the total NF performances are also improved further. It has been experiential that the proposed LNA’s linearity has little effect on the CG path [4]. Consequently, the bias voltage of the circuit and power consumption is optimized to reduce in the CG path. The different noise cancellation of paths for CMOS LNAs goes during bring in a phase mismatch among the 2 parallel paths. This phase mismatch harmfully impacts the system noise cancellation & gain [9]. For that reason, its cause on performance of NF and gain is furthermore quantitatively with analyzed in this paper.

Fig.2 Generalized LNA topology (a) CS and CG amplifier (b) signal and noise flow from CS and CG (c) small signal model analysis of CS and CG.
Low Noise Amplifier Design of CMOS Inductorless with Noise Cancellation Technique

For the small-signal model analysis [7] shown in Fig. 2(c), a MOSFET transistor in saturation can be modeled as a transconductance \( g_{m} \) juncture with a signal voltage summer at the input and a current summer at the output.

Although the circuit diagram in Fig. 2(b) is a helpful generality of NC LNAs, the structure of new NC LNAs requires some extra knowledge [7] [10]. The solution to the NC principle is the recognition of the two nodes in a circuit where the signal appears with the same polarity but the instantaneous noise appears with opposite polarity [7]. If such nodes exist in a circuit, additional circuit can forever be added of (signal + noise) voltages at these nodes suitably and combine them in such a way that the noise is nullified at the output shown in Fig. 3.

![Fig.3 Simplified circuit of noise cancellation](image)

III. DESIGN OF LNA WITH NC TECHNIQUE

A. CS AMPLIFIER

The path of CS is realized by a 2 stage amplifier as shown in Fig. 6. The 1st stage consist a transistor \( M_1 \) & resistor \( R_i \). The 2nd stage, consisting of transistors \( M_2 \) and \( M_3 \), resp., to drive 50Ω load of measurement, then the component size of \( M_1 \) has so optimized as to attain nearly 20mS \( g_{m3} \) [10]. The equivalent small ac signal model is exposed in Fig. 5. Neglecting the components of parasitic capacitors i.e., \( c_{gs}, c_{gd} \) of the MOSFET and presumptuous the input matched impedance \( (Z_{in}) \) with \( R_i \), then the voltage gain of CS amplifier is expressed by [4].

\[
A_{v}^c \approx \frac{1}{2} g_{m1} R_1 \frac{g_{m2}}{g_{m3}}
\]  

(1)

B. CG AMPLIFIER

The CG amplifier which consists of transistor \( M_4 \), resistor \( R_2 \), and a current (dc source) \( I_1 \) is adopted to schematic circuit design. With CG amplifier path in favor of achieving the perfect matching input impedance as depicted in Fig. 4. The input matching impedance of the LNA design is conquered generally by the transconductance \([9] [11]\) of transistor \( M_4 \) \( (g_{m4}) \). Thus, to match with \( R_2 \) the \( g_{m4} \) of \( M_4 \) roughly elected has 20mS. According to the equivalent small-signal analysis in Fig. 4, shows the gain of the selected CG among the adder is described as:

\[
A_{v}^C \approx \frac{1}{2} g_{m4} R_2
\]  

(2)

Where \( \beta \), is the small signal transfer function of \( M_3 \) which is specified by

\[
\beta = \frac{g_{m3}(r_{o3})}{1 + g_{m3}(r_{o3})} R_2
\]  

(3)

Where \( r_{o3} \) refers the output impedance at drain of \( M_3 \). In fact \( g_{m3}(r_{o3}) \leq 1 \) for the advanced CMOS technology [8] and \( \beta \) value is approx taken as 1.

![Fig.5 The small-signal analysis of the CMOS LNA.](image)

Unlike the input impedance matching N/W’s associated with inductors or/and transmission lines, and the component of active components generate plenty of noise power. Consequently, a scheme of noise cancellation technique [12] [13] is implemented to diminish the noise of \( M_4 \) \((\Delta v_{SA})\) which is the primary noise generator within the path of CG. As illustrated in Fig. 4, \((\Delta v_{SA})\) causes two immediate voltage responses, one each at node A & B, by opposite signs, exposed as shown beneath [4]:

\[
v_{A,M4} = i_{M4}(Z_{in} || R_2) \approx i_{M4} \frac{1}{2g_{m4}}
\]  

(4)

\[
v_{B,M4} = -i_{M4}(1 - g_{m4} R_s/2)R_2
\]  

(5)

At node A the noise voltage \( v_{A,M4} \) is amplified by CS. By the side of the output node ‘C’, having noise voltage \( (v) \) transferred by \( v_{A,M4} \) is given by

\[
v_{C,M4} = 2\Delta v_{SA} v_{A,M4} = i_{M4} A_{v}^C/g_{m4}
\]  

(6)

In view of the phase mismatch \((\Delta \theta)\), among the CG & CS paths, the output of the noise voltage \( (v) \) transferred by \( v_{B,M4} \) is revised thus:

\[
v_{C,M4} = \beta v_{B,M4} e^{i\Delta \theta} = -i_{M4}(1 - g_{m4} R_s/2)R_2 e^{i\Delta \theta}
\]  

(7)

By the side of output node ‘C’, the total noise voltage accumulated by \( M_4 \) is calculated thus:

\[
v_{C,M4} = v_{A,M4} + v_{B,M4}
\]
\[ i_{m4} \left[ \frac{A_{VS}^C}{g_{m4}} - \left( 1 - \frac{g_m R_S}{2} \right) \beta R_2 e^{j\Delta \theta} \right] \]  
(8)

To reduce the noise contribution of \( M_4 \), the circuit needs to be satisfied thus:

\[ \left( 1 - \frac{g_m R_S}{2} \right) \beta R_2 \cos(\Delta \theta) = \frac{1}{g_{m4}} A_{V}^C \]  
(9)

For, \( g_{m4} = 1/R_s \). Substituting (9) for (2), the relationship between \( A_{V}^C \) and \( A_{V}^G \) for the best noise cancelation is obtained by

\[ |A_{V}^C| = \frac{1}{\cos(\Delta \theta)} |A_{V}^S| \]  
(10)

Taking into consideration the phase mismatch among CS & CG paths have been aggregated in adder. Then on the whole voltage gain is revised as:

\[ A_{V}^T = A_{V}^C + A_{V}^G (\Delta \theta) = \frac{1}{2} \left( g_{m1} R_1 + g_{m2} R_2 e^{j\Delta \theta} \right) \]  
(11)

To attain optimally revoke the noise power of \( M_4 \), the ratio of \( A_{V}^C \) and \( A_{V}^S \) can be calculated thus:

\[ \phi = \frac{A_{V}^C}{A_{V}^S} = 1 + j\tan(\Delta \theta) \]  
(12)

IV. SIMULATION RESULTS

In the design of proposed inductorless LNA, the generated simulations were carried out using SpectreRF from Cadence design suite. These selected LNA structure working at the frequency of 1.04-1.8GHz and design was using CMOS 45nm GPDK technology process. Fig. 7-13 shows simulated results and S-parameters result of CMOS LNA. The LNA achieved to acquire a voltage gain (S_{21}) of 20-23dB @ 1.04-1.8GHz shown in Fig.8. The plot of NF is shown in Fig. 9 as 1.2-0.6dB@ 1.04-1.8 GHz. The input return loss, S_{11} is -12.5 dB & output return loss S_{22} is -11.3dB are shown in Fig. 10 & Fig. 11. The plot of Fig. 12 gives the reverse isolation (S_{12}) are -55dB that is provided by the circuit. The attained value of NF is supposed to be good as it exceeds the constraint which is normally less than 2 dB without having to tradeoff the power gain which also satisfies the prerequisite and, also obtained Simulated 1dB compression point (IP_{1dB})=-22.9dBm shown in Fig.13.

Fig.6 The Schematic of the Inductorless CMOS LNA

Fig.7 Input (red signal) and amplified output (green signal)
Fig. 8 Simulated voltage gain $S_{21}=20\,$dB @ 1.04GHz and 22.9 dB @ 1.8GHz center frequency

Fig. 9 Simulated Noise Figure (NF) = 1.2 dB @ 1.04GHz and 0.6 dB @ 1.8 GHz center frequency

Fig. 10 Simulated input return loss $S_{11} = -12.5\,$dB @ 1.04GHz and -11.12 dB @ 1.8 GHz center frequency

Fig. 11 Simulated output return loss $S_{12} = -11.3\,$dB @ 1.04GHz and -12.8 dB @ 1.8GHz center frequency

Fig. 12 Simulated $S_{12} = -55.01\,$dB @ 1.04GHz and -
The simulated results are summarized and compared to other related works in the area of LNA design and also with some designs employing the inductorless CMOS LNA strategy. The results are tabulated in Table 1.

### Table 1: Performance summary and comparison of CMOS LNAs

<table>
<thead>
<tr>
<th>Parameter</th>
<th>My work</th>
<th>[5]</th>
<th>[4]</th>
<th>[2]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology (nm)</td>
<td>45nm</td>
<td>65n</td>
<td>18</td>
<td>130</td>
</tr>
<tr>
<td>Center Frequency (GHz)</td>
<td>1.04GHz</td>
<td>0.05</td>
<td>0.1</td>
<td>0.1</td>
</tr>
<tr>
<td></td>
<td>1.8GHz</td>
<td>3</td>
<td>1.8</td>
<td>2.1</td>
</tr>
<tr>
<td>Voltage Gain (dB)</td>
<td>20-23 dB</td>
<td>8</td>
<td>14.5</td>
<td>21</td>
</tr>
<tr>
<td>Noise Figure (dB)</td>
<td>1.2-0.6dB</td>
<td>6*</td>
<td>3.8</td>
<td>2.0</td>
</tr>
<tr>
<td>Input return loss $S_{11}$ (dB)</td>
<td>-11.2 dB</td>
<td>--</td>
<td>-7.8</td>
<td>--</td>
</tr>
<tr>
<td>Reverse isolation $S_{12}$ (dB)</td>
<td>-55dB</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>Output return loss $S_{22}$ (dB)</td>
<td>-12.8</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
</tbody>
</table>

### V. CONCLUSION

An Inductorless CMOS LNA for multi-standard wireless applications with less-area, single-chip is presented. This NC technique is used to cancel out the noise involvement in LNAs at the output of matching device. The proposed Inductorless CMOS LNA designed in a CMOS 45nm GPDK technology process. The simulated results within the frequency range of 1.04GHz-1.8GHz are considered here. The maximum gain has achieved 20dB @ 1.04GHz, 23dB @ 1.8GHz and a low NF of 1.2dB @ 1.04GHz, 0.6dB @ 1.8GHz. The input and output reflection coefficients are obtained as less than -10dB it is desirable value to fit in this LNA. The obtained 1dB compression point (IP$_{1dB}$) is -22.4dBm and also LNA consumes only 6.5mA with 1.2V power supply.

### REFERENCES


### AUTHOR PROFILE

Mahesh Mudavath was born in Warangal, Telangana state, India. He received the B.Tech degree in Electronics and Communication Engineering from JNTU Hyderabad, India. He received M.Tech degree in VLSI Design from C-DAC Mohali, Chandigarh, India. Presently he is pursuing the Ph.D. degree in the area of VLSI Design from Koneru Lakshmaiah Education Foundation, Vaddeswaram, Guntur, A.P, India-522502. His research interests include CMOS analog circuit, RF wireless transceiver design, and Low Noise Amplifier Design. He has published 15 International Journals. He is a life member of ISTE.

Dr. Hari Kishore Kakarla was born in Vijayawada, Andhra Pradesh, India. He received B.Tech in Electronics & Communication Engineering from JNTU Andhra Pradesh, India, and M.Tech from SKD University, Andhra Pradesh, India. He completed the Ph.D in the area of VLSI from Koneru Lakshmaiah Education Foundation, Vaddeswaram, Guntur, A.P, India-522502. Presently he is working as a Professor in ECE, K L University, Guntur, Andhra Pradesh, India, where he has been engaged in teaching, research and development of Digital Testing, Low-Power VLSI, High-speed CMOS VLSI.

Retrieval Number: A1305109119/2019©BEIESP
DOI: 10.35940/ijeat.A1305.109119
Low Noise Amplifier Design of CMOS Inductorless with Noise Cancellation Technique

Sanjay Madupu was born in Warangal, Telangana state, India. He received the B.Tech degree in Electronics and Communication Engineering from JNTU Hyderabad, India. He received M.Tech degree in VLSI and Embedded System from (KITS) KU Warangal, India. Presently he is working as Asst. Professor in Vaagdevi Engineering College, Warangal, Telangana, India. His research interests include CMOS analog and digital circuits, RF wireless transceiver design, and Low Noise Amplifier Design.

Prashanth Chittireddy was born in Warangal, Telangana state, India. He received the B.Tech degree in Electronics and Communication Engineering from JNTU Hyderabad, India. He received M.Tech degree from JNTU Hyderabad, India. Presently he is working as Asst.Professor in Vaagdevi Engineering College, Telangana, India. His research interests include CMOS analog circuits, RF wireless transceiver design, and Low Noise Amplifier Design. He is a life member of ISTE.

Srinivas Bhukya was born in Warangal, Telangana state, India. He received the B.Tech degree in Electronics and Communication Engineering from JNTU Hyderabad, India. He received M.E degree in Communication Engineering from Osmania University (OU), Hyderabad. Presently he is working as Asst. Professor in Sri Indu College of Engineering and Technology, Ibrahimpatnam, Hyderabad, Telangana, India.