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# Design and Analysis of 32-bit Reverse Converter based on low power Parallel Prefix Adder

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***Abstract:*** ***The Residue Number System (RNS) based reverse converter can play as main role in Parallel arithmetic operations of Digital Signal Processing (DSP) applications and VLSI technologies. Normally, by the use of carry adders, the reverse conversion design gives high delay and high power consumption. Due to resolve of above problem, the design of reverse converter is proposed by the use of familiar high speed (less propagation delay) Parallel Prefix - Kogge Stone Adder (PP- KSA). This paper describes the design of 32-bit Reverse converter with regular PP-KSA and proposed MUX (Multiplex) logic of PP-KSA with Hybrid Modular Parallel Prefix structure (HMPE) separately. In addition to that, the performance of that designs are analysed based on area, delay and power independently. The Performance results of proposed MUX logic of PP-KSA Reverse converter design yields low power than the other design which uses the regular PP-KSA. The simulation and synthesis effects can be done in Xilinx ISE 14.2i tool.***

***Keywords: Brent Kung Adder, Carry Generation Stage, Hybrid Modular Parallel Prefix Adder, Kogge Stone Adder. Ladner Fischer Adder, Multiplex logic.***

## I. INTRODUCTION

Generally, to achieve efficient fundamental arithmetic operations in DSP applications, the Parallel Algorithm based design provides better performance. In existing, the above process carried out by the use of carry binary adders like Carry Select Adder (CSLA), Carry Look Ahead Adder (CLA), and Ripple Carry Adder (RCA) etc [17]. By using of above adders, the design provides low speed and high power consumption [1]. To resolve the above problem, the DSP design techniques can be carried out using regular Parallel Prefix Adder [15]. The PPA which gives high speed DSP design technologies with low power and high speed operations [22]. The various designs of 32 bit regular Parallel Prefix Adders (Brent Kung Adder – BKA, Kogge Stone Adder - KSA, Ladner Fischer Adder – LFA) are designed and the performance of those adders can be analysed based on area, delay and power in existing paper [2]. The performance of that result clearly shows that the Kogge Stone Parallel Prefix Adder provides low power and less delay than BKA and LFA and the area to be increased in KSA.

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The PPA can be used in RNS based Reverse converter design with the use of high speed and low power VLSI applications in DSP technologies [3]. This paper is arranged as follows, in section 2; explains the design of reverse converter with regular Parallel Prefix Algorithm, in section 3; it explains the design of reverse converter with proposed MUX logic, in section 4; it describes the results of both logic used in reverse converter design and performance results are compared. The final section is concluded with the analysis performance and discussion.

## II. REVERSE CONVERTER DESIGN WITH REGULAR PARALLEL PREFIX ALGORITHM

PPA is mainly used in DSP technologies due to high speed arithmetic operations. Here the carry is initially calculated for both 0 and 1 inputs in parallel manner so that the timing constraints is less [20] and need not to wait for the carry for next sum calculation [4]. There are many types of PPA used in Arithmetic processing such as KSA, BKA, LFA, Han Carlson Adder (HCA) etc [18].

The Parallel Prefix Algorithm includes three basic steps: The first step is Pre computation; here propagation (P) and generation (G) values are calculated based on the given inputs, [5] The second step is Carry generation stage; here the carry generation and carry propagation values are calculated by using pre computation results [21], The third step is Post computation: here the final results of sum and carry out values are calculated [6]. As already discussed, from 32 bit Parallel Prefix Adder's performance compared results, the Kogge stone adder gives better performance in less delay operation [7].

The 32 bit reverse converter design used the regular eight stage 4-bit KSA adder to achieve the better performance [16]. This regular Parallel Prefix algorithm design [8] which gives sum output of 32 bit KSA that is calculated separately by using XOR logic function. [19] The example of sum [0] and sum [1] output calculation is given in the equation (1) and (2).

Sum [0] = P [0] XOR Cin; -------- (1)

Sum [1] =P [1] XOR C [0]; -------- (2)

This type of regular PP-KSA is directly applied to reverse converter design which includes Hybrid Modular Parallel Prefix Excess one (HMPE) structure [9]. The Basic HMPE structure is shown in "Fig. 1".

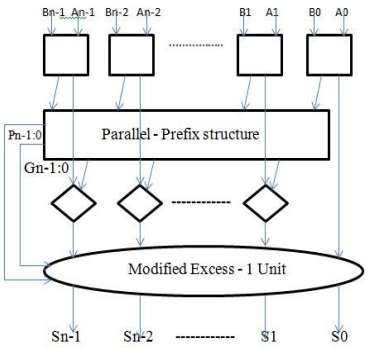


**Fig.1. Basic HMPE Structure of Reverse converter design**

The HMPE structure is used in Reverse Converter design which consists of one Parallel- Prefix Structure and one Excess -1 Unit [10]. The first type of Reverse Converter design is used the PP-KSA with regular Parallel Prefix Algorithm and Excess-1 unit which provides the sum and carry out results [11].

## III. REVERSE CONVERTER DESIGN WITH PROPOSED MUX LOGIC OF PPA ALGORITHM

As already known, Due to less delay operation, a 32-bit PP- KSA provides better performance than other PPA adders [12]. Here also the 32 bit reverse converter design used the regular eight stage 4-bit KSA adder to achieve the better performance [13]. This 32 bit reverse converter design is used the PP-KSA with Proposed MUX (Multiplex) logic function.

The proposed MUX logic function directly applied in the output sum results instead of XOR function of regular PP-KSA algorithm. All other processing is same as the regular Parallel prefix algorithm design. The example of sum output calculation is given by following: Usually, the MUX output depends on the select signal only, here the carry signal as select signal; if Cin as 0 then sum [0] output is directly as P [0] result, else if Cin as 1 then sum [0] output as invert of P [0] result. This process is applicable till sum [31] output.

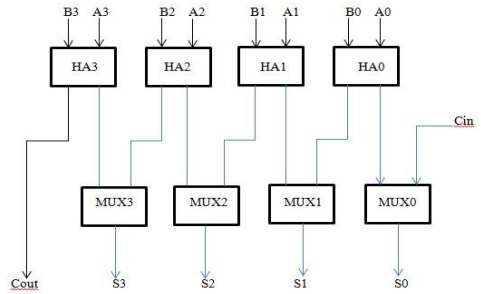


**Fig.2. Proposed PP-KSA design using MUX logic**

The Proposed MUX logic PP-KSA is then directly applied to reverse converter design which includes HMPE structure. The modified 4 bit PP-KSA with proposed MUX logic design is shown in "Fig.2". The HMPE structure is used in Reverse Converter design which consists of one Parallel- Prefix Structure and one Excess -1 Unit [14]. The second type of Reverse Converter design is used the PP-KSA with MUX logic and Excess-1 unit which provides the sum and carry out results for low power operations.

## IV. PERFORMANCE COMPARISON ANALYSIS OF REVERSE CONVERTER DESIGNS

This section explains the comparison results of reverse converter design with regular PP-KSA design and PP-KSA with MUX logic. The comparison takes place corresponding to area, delay, and power. The simulation and synthesis effects carried out in Xilinx 14.2i tool.

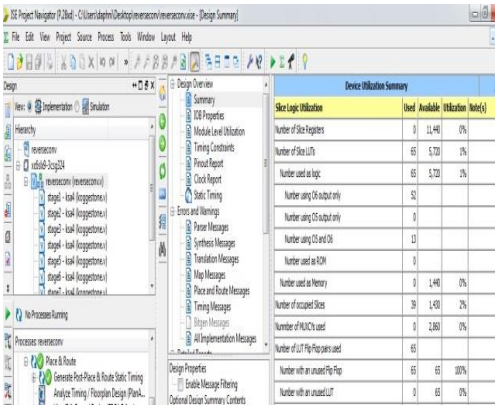

**Fig.3. Area consumption of Reverse Converter with regular PP-KSA**

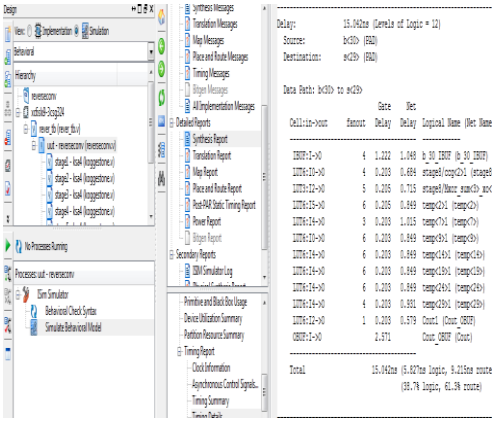

**Fig.4. Delay report of Reverse Converter with regular PP-KSA**

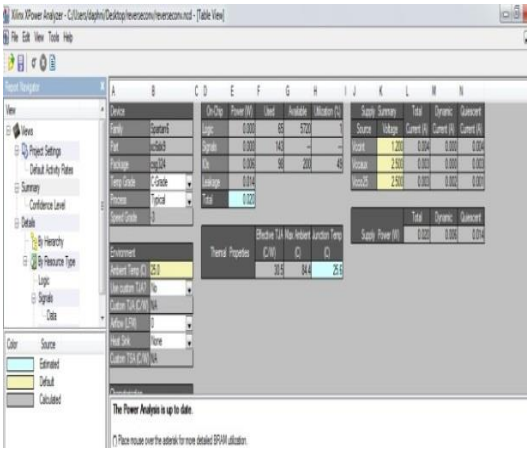

**Fig.5. Power analyser result of Reverse converter with regular PP-KSA**

The initial method which used in Reverse converter design is regular PP-KSA algorithm. Area consumption of regular PP-KSA method of reverse converter design is shown in "Fig.3" and the delay report of regular PP-KSA method of reverse converter design is shown in "Fig.4".

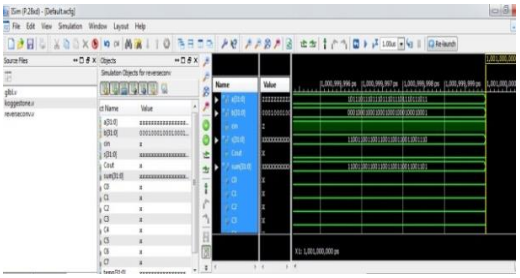

**Fig.6. Waveform results of Reverse Converter design with regular PP-KSA**

Here the number of Slices used as 39 and the delay utilization is 15.042 ns. The Power analyser report of reverse converter with regular PP-KSA design is shown in "Fig.5" and waveform results of reverse converter with regular PP-KSA design is shown in "Fig.6". Here the Power utilization as 0.020W.

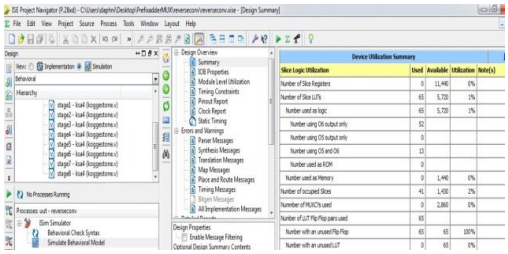

**Fig.7. Area consumption of Reverse Converter with MUX logic of KSA**

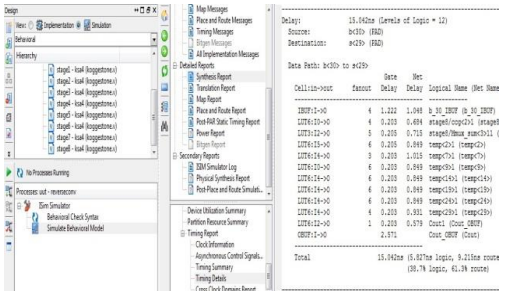

**Fig.8. Delay report of Reverse Converter with MUX logic of KSA**

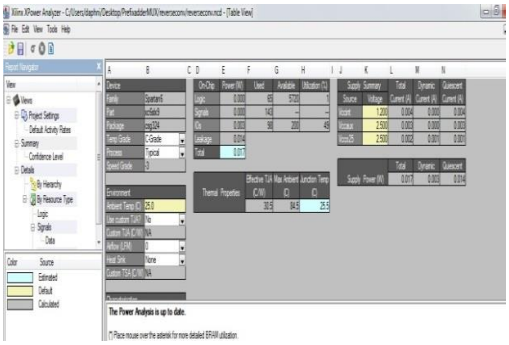

**Fig.9. Power analyzer result of Reverse converter with MUX logic of KSA**

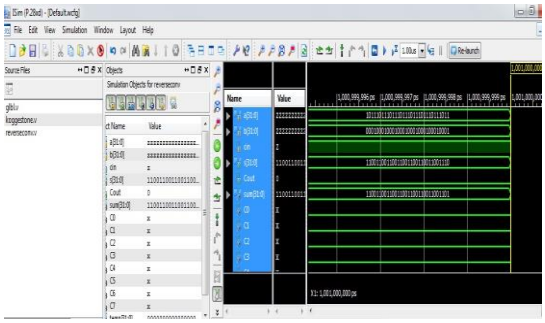

**Fig.10. Waveform results of Reverse Converter design with MUX logic of KSA**

The Proposed method which used in Reverse converter design is MUX logic of PP-KSA algorithm. Area consumption of reverse converter with MUX logic KSA design is shown in "Fig.7" and delay report of reverse converter with MUX logic KSA design is shown in "Fig.8". Here the number of Slices used as 41 and the delay utilization is same as first method as 15.042 ns. The Power analyzer report of reverse converter with MUX logic design is shown in "Fig.9" and waveform results of reverse converter with MUX logic design is shown in "Fig.10". Here the Power utilization as 0.017W.

**Table- I: Performance comparison of Reverse Converter Designs**

| Reverse Converter Design Methods | Area (Number of Slices Used) | Delay (ns) | Power (W) |
|---|---|---|---|
| Regular PP-KSA | 39 | 15.042 | 0.020 |
| Proposed MUX logic of PP-KSA | 41 | 15.042 | 0.017 |

The Performance analysis can be carried out to both the types of reverse converter design based on area, delay and power that clearly shows in "Table-I". Depends upon the area, the first method used in Reverse Converter with regular PP-KSA method is better. Because the number of slices used as 39 and the other hand the number of slices used as 41. Compared to delay, both the type of reverse converter design have same timing value that is 15.042ns. Depends upon power, the Proposed MUX logic of KSA reverse converter design is better one since the power utilization as 0.017W and the regular PP-KSA method of reverse converter have 0.020W.

## V. CONCLUSION

An effective Reverse Converter design is done with 32 bit Proposed MUX logic KSA algorithm. This Proposed logic of Reverse converter design is best suitable in low power VLSI and DSP applications. Here two methods of reverse converter are designed and Performance analyses are compared based on area, delay and power.

From the analysis, the Proposed MUX logic of KSA reverse converter design is better than the regular PP-KSA logic of Reverse converter design. To achieve further more action which is required in performance of proposed logic as reduce area utilization which will be the future exertion of this paper.

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