International Journal of Engineering and Advanced Technology (IJEAT)
ISSN: 2249-8958 (Online), Volume-9 Issue-1, October, 2019

High Efficiency RF Energy Harvesting CNTFET Rectifier for Bio-implants Applications

Munna Khan, Mohd Tauheed Khan, Mohd Hasan

Abstract: ***Carbon nanotube field effect transistor (CNTFET) based full wave rectifier given in the paper, works efficiently in the range of radio frequency. The CNTFET offers extremely less power loss and high through-put because of its high conducting properties. The Complementary Metal Oxide Semiconductor (CMOS) based studies are available but CNTFET based studies are rarely available. Therefore, CNTFET based rectifier has been used for the replacement of CMOS based rectifier architecture. The full wave rectifier circuit was analyzed using 32nm CNTFET Stanford model. An additional circuit of clampers is also used for introducing a negative DC level. Introduced negative DC signal further negated RF input signal and combined signal used for biasing the p type device during its conduction cycle. The CNTFET based rectifier with clamper circuit decreases the effective threshold voltage of switching p CNTFETs. The circuit resulted better RF input sensitivity of the transistor. Results show that 77.7% power conversion efficiency is suitable for powering up the bio-implantable devices.***

Keywords: ***Carbon Nanotube Field Effect Transistor (CNTFET), Complementary Metal Oxide Semiconductor (CMOS); Clamper, Radio Frequency (RF), Full Wave Rectifier.***

I. INTRODUCTION

Industry and academia have attracted towards the field where wirelessly power transfer techniques are widely mainly used in the biomedical implantable devices, radio frequency identification (RFID) tags and wireless sensors [1-3]. Appropriate energy is required to support the operation of these devices. Size is also a stringent constraint for these devices. Efficient power conversion mechanisms are very much needed to provide sufficient energy and powering up these devices. Battery size, less energy density, reliability, inadequate life time of device and safety to human beings are some of the constraints contained by the embedded battery and the harvesting systems. Therefore, wireless powering up of the implantable device becomes more important. Generally, there are two types of wirelessly power transfer mechanism. The one mechanism is based on radiation power transfer techniques for the far field applications [4, 5]. The other mechanism is non-radiated power transfer techniques which are being used for near field power transfer (NFPT) [6]. The power is transferred over long range in far field and implemented with the help of electromagnetic waves radiations while in case of near field, an inductive and capacitive couplings are used to transfer the power comparably over short distance. The NFPT systems are generally safe and have high efficiency. Therefore, these NFPT systems are very popular in the applications such as wireless toothbrush charger, radio frequency identifications (RFIDs), wireless auto charging, pacemakers, hearings aids and blood stream monitors. These NFPT systems are being used in the daily life of human being. Efficient rectifier architecture is required to convert the RF energy signal to the DC signal before powering up the implantable device. However, such RF energy transfer suffers with transmission loss. Low power transmission found due to improper electromagnetic coupling: inductive RF links. Therefore, it becomes utmost important to have efficient rectifier for getting required output power to the load. A number of other scientists proposed various rectifier architectures based on CMOS technology. In the environment of low power, designing an efficient rectifier is very challenging with elevated effectiveness (PCE). Power conversion, from an input AC signal to unregulated DC signal is achieved with the help of wideband rectifiers which have diode and transistors. Conventionally wideband diode based power rectifiers were generally used in power conversion chain. But it faced high threshold voltage drop. Later diode-tied MOS transistor replaced diode in the rectifier, which is easier to implement in CMOS process. Still, overall power conversion efficiency of the rectifiers degrades significantly due to the voltage drop across the switching transistors. Output voltage is also getting reduced because of the voltage drop across the transistor switch. Many earlier rectifier topologies were given and discussed with their own pros and cons. Power dissipation because of threshold voltage is high in CMOS technology [7-14]. Previous research works of authors also described rectifier architectures based on carbon nanotube FET (CNTFET) technology for low power applications [20, 23].
In an energy harvesting systems, rectifier's power conversion efficiency (PCE) is a central parameter of rectifier used for RF-to-DC converter [8]. Carbon nanotubes (CNTs) are the promising transistor's channel material in the field of low power and high speed electronics applications because of its near ballistic transport property and energy band structure. The CNTs are being made by rotating graphene sheets. Direction of rotations (chirality) of the sheets and carbon atoms arrangement make these produced CNTs behaves as a metal or as a semiconductor.

Revised Manuscript Received on October 30, 2019.
* Correspondence Author
Munna Khan*, Department of Electrical Engineering, Jamia Millia Islamia, New Delhi, India , Email:. Email: mkhan4@jmi.ac.in
Mohd Tauheed Khan*, Department of Electrical Engineering, Jamia Millia Islamia, New Delhi, India, Email: mohd127229@st.jmi.ac.in
Mohd. Hasan, Department of Electonics Engineering, Aligarh Muslim University, Aligarh,Uttar Pradesh, India, Email: mohd.hasan@amu.ac.in

The semiconductor type carbon nanotubes are used in the channel to form a CNTFE. The properties of the CNTFET are better transconductance, carrier mobility, channel control and current drive [15-19].

The current research paper focus on architecture of CNTFET based rectifier and analyses the performance. The performances of CNTFET based rectifier will be compared with CMOS based rectifier for better suitability. Therefore, in coming future, the CNTFET based rectifier may replace CMOS based rectifier architecture possible.

II. MATERIAL AND METHODS

A. Energy Harvesting System

An energy harvesting system is having a receiving antenna, rectifiers and power handling circuits. The design of an energy harvesting systems aims to optimize the design of antenna, rectifier and energy management circuits, typically I shown in Fig.1.

Rectifier is one of the important blocks of a RF energy harvesting system. The rectifier block alters the received RF energy to corresponding DC energy. Therefore, the effectiveness of antenna and rectifier will decide the overall performance of an energy harvesting system. A crucial parameter, power conversion efficiency (RF to DC conversion) decides that how efficiently an RF energy signal is changed to the corresponding DC energy by the rectifier.

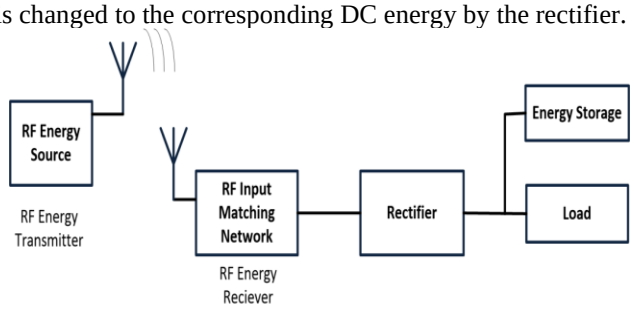


Fig. 1. Block Diagram of Energy Harvesting System

Carbon Nanotube Field Effect Transistor

Carbon nanotubes (CNTs) are used in between drain and source as a physical channel in CNTFET while a virtual channel is induced in case of CMOS transistor [15]. CNTs are made up by grapheme sheets. The single layered thin graphene sheets rolled to form tubes. The direction of the rolling decides that the formed single layered/walled CNTs (SWCNTs) are of metallic or semiconducting in nature. Chirality is the the direction of rotation which is represented as the resultant of two vectors (n1, n2) in two different directions as given in Eq (1). Here n1 and n2 are the integer and define the SWCNT chirality [15-19]. If n1- n2 is three multiple of an integer then the produced SWCNT will be a metallic otherwise in all other cases it will be semiconducting [15]. Metallic SWCNTs are widely used as interconnect while semiconductor nanotubes show incredible consideration for high performance transistors which are required in nano-electronics applications. Chirality magnitude of the SWCNT is calculated with the Eq (2) and its value is decided by the CNTs diameter. Therefore, the diameter of CNTs used in CNTFETs can be providing the good controlled of the electrical characteristics of the CNTFETs.

$$Ch = a\left(n_1^{\,2} + n_1 n_2 + n_2^{\,2}\right)^{1/2} \quad (1)$$

$$Dcn = \frac{Ch}{\pi} \cong \frac{a}{\pi}\left(n_1^{\,2} + n_1 n_2 + n_2^{\,2}\right)^{1/2}$$

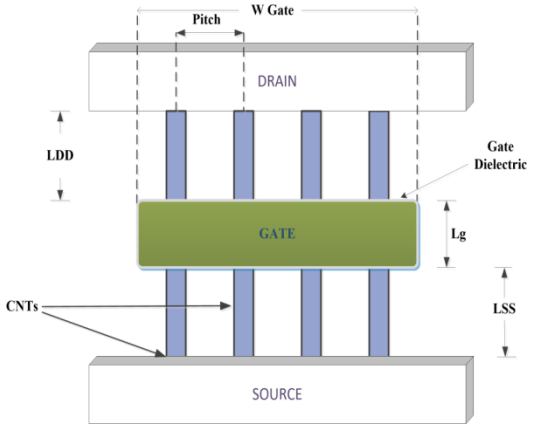
Here distance between the nuclei of two carbon atoms and it is equal to 2.49 Å.

A typical construction of a CNT field effect transistor (CNTFET) is given in Fig. 2 . This construction shows that drain,source regions are heavely doped except the undoped CNT channel region. CNTFET needs threshold voltage to make the transistor on similar to the MOSFET transistor. CNTFET threshold voltage adaptibility is achieve by changing the diameter of the CNTs as shown in Eq (3).

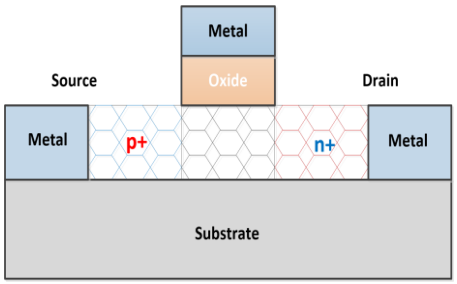
$$V_{th} = \frac{E_g}{2e} = 0.557a\frac{V_\pi}{Dcn} = \frac{0.43}{Dcn} \quad (3)$$

Here “e” charge on electron; Vπ is π bond energy with value 3.033 electron-volt.

CNTFET is also a three terminal device like MOSFET. Its working can be control by the voltage applied at one of the three terminal i.e. gate. The gate voltage is across the channel and by varying the gate voltage, the flow of charge carrier between drain and source can be easily controlled. The current intensity flow between the source and drain is determined by the number of carbon nanutubes introduced in the region of the transistor's channel. The carriers flow through these narrow CNTs between the source and drain terminal. This carrier flow shows ballistic transport properties because of the availability of longer mean free path compared to the device dimensions. Therefore, the mobility of the carrier becomes higher because of non collision of charge carrier and reduction in resistance.



(a) Top View



(b) Side View

Fig. 2. CNTFET Structure

CNTFETs also show larger drive current, higher transconductance, lower on resistance and ignorable off-current compared with the conventional silicon based technologies. Threshold voltage (Vth) of CNTFETs based device can also be controlled by varying the diameter (chirality) of carbon nanotubes. Hence the voltage drop across the diode switch can be reduced with reduction in Vth of the device. Therefore, CNTFET based device offer better analog and digital circuits [19-25] performance because of the lower threshold voltage and excellent electrical properties.

B. Carbon Nanotube Field Effect Transistor Model

The Stanford CNTFET model is used for the analysis of the rectifier. Single-walled carbon nanotubes (SWCNTs) are used as a channel in a enhancement mode, unipolar Metal Oxides Semiconductor Field Effect transistors (MOSFETs), SPICE compatible CNTFET model given by the Stanford University. In a CNTFET may have one or more CNTs with user defined CNTs diameter (chirality). The capacitors network is well described in the model which is based on quasi-ballistic transport. Many non idealities are also taken into consideration in the CNTFET model. The CNFET SPICE compatible model can be directly used in SPICE deck for the circuit performance analysis. CNT based circuits functions can be easily and accurately explored and verify with this CNTFET model. Table 1 shows some of the design parameters of CNTFET used for the analysis of the rectifier circuit.

Table 1. CNTFET Technological Parameters

Parameter	Value	Parameter Description
(n1,n2)	(19,0)	Chiral Numbers
Dch	1.5nm	Diameter of CNT
Lch	32nm	Physical Channel -Length
Lgeff	200nm	Mean free path in Intrinsic Semiconductor
Tox	4nm	Thickness of top gate Dielectric Material
Efo	0.06 eV	doped Drain/Source Tube's Fermi level

III. THE CNTFET BASED RECTIFIER ARCHITECTURE

The aim of this rectifier topology is to get better PCE with reducing efficient threshold voltage of switching transistors and power dissipation across the rectifier circuit. These are being achieved by using

i. An external clamper circuits to bias the gate of pCNT switching transistor in the architecture.
ii. And exploiting very good electrical properties of the CNTFET

The proposed architecture with high PCE is suitable for the applications in low power requirements like biomedical implantable devices, RFIDs and biosensors. In this architecture the external auxiliary circuit biased with RF input signal produced a shifted DC voltage level which is negative in nature and used for the biasing of the main switching transistor. This shifted negative voltage is used to bias the gate of main pCNTFET switch. The effective power-on voltages of rectifying transistors (pCNTFET) are diminished with this clamper mechanism. Therefore, power dissipation of rectifying transistor reduces during their conducting state and results in improved PCE and voltage conversion at low input voltage.

This CNTFET based rectifier architecture used the threshold reduction technique by using bootstrapping clamper circuit along with better electrical properties of CNTs. The clamper circuit biases the gates of p type rectifying transistor to alleviate the turning on of the transistor. The auxiliary clamper circuit as shown in Fig. 3 with a capacitor and a diode connected pCNTFET provides negative voltage to the switching transistor for the duration of on condition while a positive gate-voltage during non conducting state. Therefore, the switching transistors in the rectifier become on comparatively lesser input voltage and the efficiency and sensitivity of the rectifier is improved.

The p type transistors offers greater resistant during conduction as compared with the n type transistor. Therefore, p type transistors are being used in the clamper circuit as it is supposed to draw minimum current from input RF source during the on state of switching transistor.

This architecture consists of off-chip parallel capacitor (2pF) and resistor (10kΩ) load. Coupling capacitors Cc1 and Cc2 of 21pF are also used off-chip while Cp1 and Cp2 of 2pf are used in the circuit.

The parameters of CNTFET rectifier architecture are given in Table 2.

Table 2. Parameters of Rectifier Architecture

Transistor	Number of CNT	Inter CNT Pitch	Diameter of CNT
N_1	30	4	1.5
N_2	30	4	1.5
P_1	80	4	1.5
P_2	80	4	1.5
P_3	5	2	1.5
P_4	5	2	1.5

The rectifier architecture working for the one time period input signal is discussed as below.

During negative half cycle of input signal, coupling capacitor Cc1 will charge upto VCc1 as given in Eq (4).

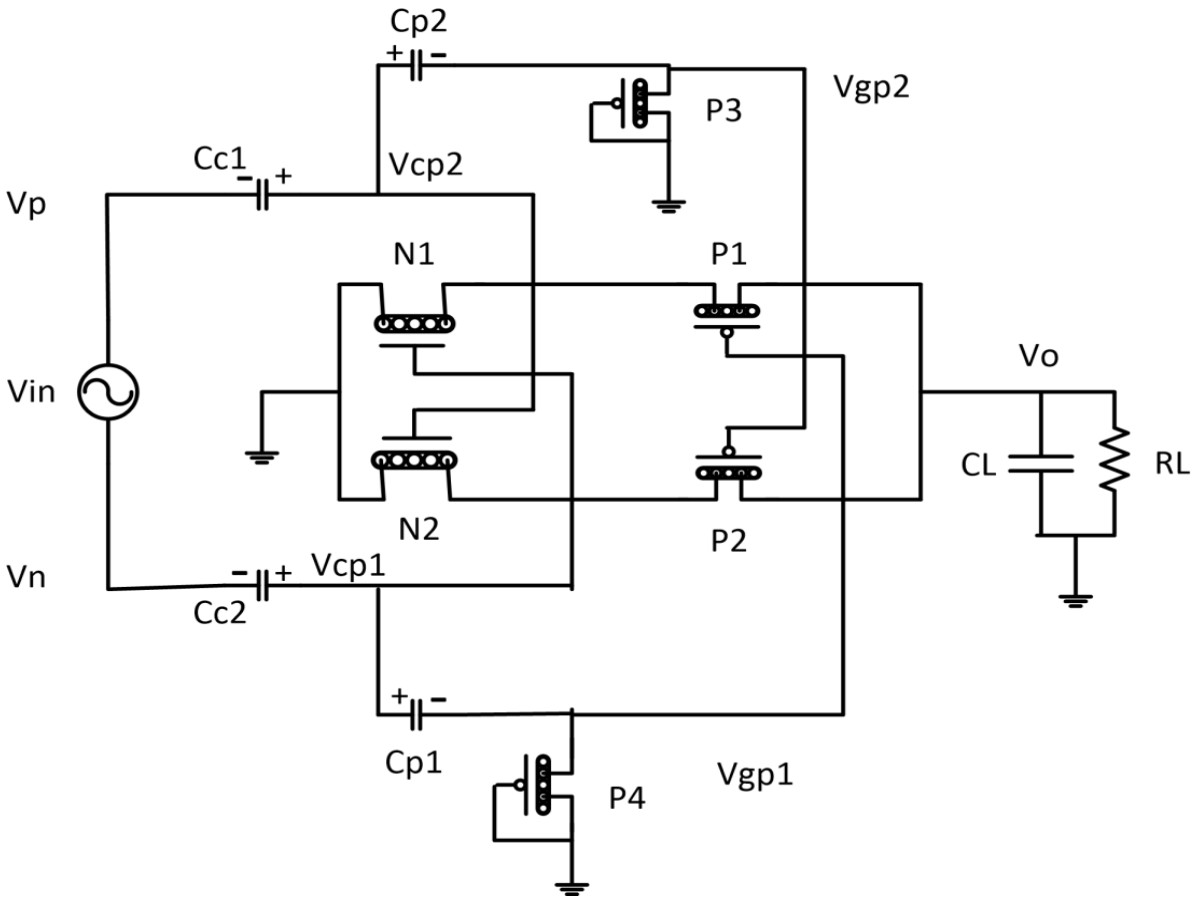
$$V_{Cc1} = Vp - Vds\ (N1) \quad (4)$$

For the duration of the positive half cycle, the capacitor Cp2 will charge upto VCp2 as shown by Eq (5) during the on condition of diode connected transistor P3.

$$V_{Cp2} = 2Vp - Vds\ (N1) - Vsd(P3) \quad (5)$$

Where, Vds(N1) is the voltage across drain-source of the N1 switching transistor while Vsd(P3) is the voltage across source-drain of P3 transistor. Vp is input differential signal voltage. The voltages on gates of P2 transistor and N1 transistor with CMOS architecture [9] and our proposed CNTFET based architecture are analysis and compared over the period of one time cycle of input RF signal. P2 transistors biasing voltage on gate i.e. Vgp2 and N2 transistor gate bias voltage Vgn2 are equal. These equal gate voltages are given in Eq (6) for positive half cycle and in Eq (7) for negative half cycle of the input RF signal.

(a)



(b)

Fig. 3. (a) Symbol of n ype and p type CNTFET (b) CNTFET based Rectifier Architecture

For, Vp > 0, N2 on, P2 off:-

$$V_{gp2} = V_{gn2} = 2Vp - Vds\ (N1) \quad (6)$$

For, Vp < 0, N2 off, P2 on:-

$$V_{gp2} = V_{gn2} = -Vds\ (N1) \quad (7)$$

In the positive half cycle, Eq (8) and (9) gives the voltages on gate terminal of N2 and P2 transistors of our proposed circuit. From these two Eqs we conclude that the transistor N2 conducts as the available gate voltage is higher than the transistor N2 threshold voltage while the positive P2 gate voltage makes it in off state during the same time.

for, Vp > 0, P2 is off, and N2 is on:

$$V_{gp2} = Vp + V_{Cc1} - V_{Cp2} = Vsd(P) \quad (8)$$

$$V_{gn2} = Vp + V_{Cc1} = 2Vp - Vds(N) \quad (9)$$

During negative half cycle, Eqs (10) and (11) provide the biasing gate voltages of N2 and P2 transistors respectively.

For, Vp < 0, P2 is on, and N2 is off:

$$V_{gp2} = -Vp + V_{Cc1} - V_{Cp2} = -2Vp + Vsd(P3) \quad (10)$$

$$V_{gn2} = -Vp + V_{Cc1} = -Vds(N1) \quad (11)$$

It is also clear from the Eqs as well as from the Fig. 4 that transistor P2 (Vgp2) has more negative gate voltage than the conventional [9] and therefore, conducts more negative voltage. Therefore, the proposed rectifier will provide greater PCE with low input RF signal. The Eq. (12) gives the expression for the DC voltage at output terminal of our given architecture.

$$Vout = Vp + Vcc_1 - Vsd(P1) = 2Vp - Vds(N1) - Vsd(P1) \quad (12)$$

The operation of other half circuit (made up by Cc2, Cp1, N1, P1 and P4) will be same as discussed above.

The output voltage by other half circuit will also be the same as given in the Eq (12).

IV. RESULTS AND DISCUSSIONS

The rectifier architecture is analyzed with 32nm CNTFET technology. The CNTFET rectifier architecture used Stanford CNTFET model for the simulations. Power conversion efficiency (PCE) and voltage conversion efficiency (VCE) as given in Eq (13) and (14) describes the rectifier circuit's performance.

$$PCE = \frac{Pout}{Pin} X\ 100 \quad (13)$$

$$VCE = \frac{Vout}{Vm} X\ 100 \quad (14)$$

An RF input signal with 953MHz frequency is given to the rectifier architecture with 10 kΩ load resistor. We are excluding the transmission and reflection losses in the analysis.

The gate voltages of transistors N2 and P2 are shown in Fig 4. These voltages are varying in time taken from the simulated results of the rectifier being used to bias the transistor N2 and P2.

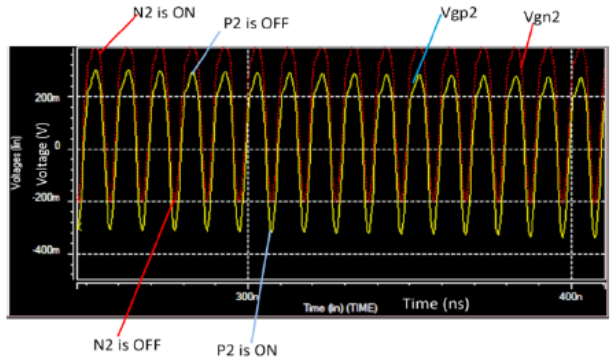


Fig.4. Gate Voltages of transistors N2 and P2

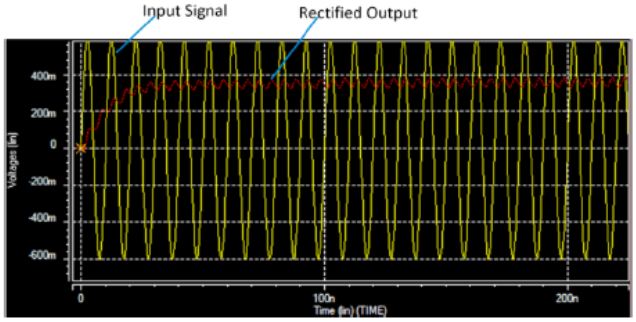


Fig.5. Rectifier output signal

The rectifier output is given in the Fig 5.

The PCE of the rectifier is decreasing with lower input power given the Fig 6.

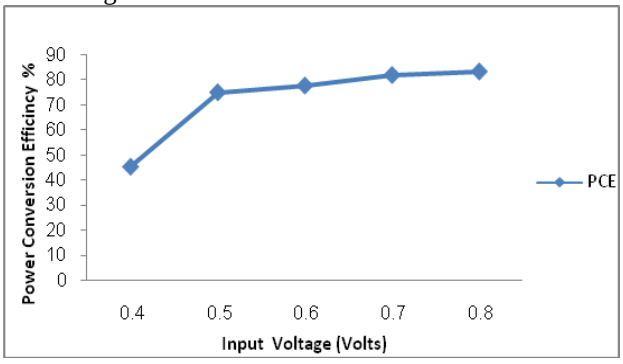


Fig..6. Power Conversion Variation with Input Signal

Table 3. Performance Comparison of Referenced Architecture

Reference	[10]	[11]	[12]	[13]	[14]	[20]	*This Work*
Technological Process	CMOS					CNTFET	
	40 nm	0.18 µm	0.18 µm	0.18 µm	0.18 µm	32 nm	32nm
Frequency (MHz)	900	10	13.56	953	953	13.56	953
(N) Stage	8	1	1	1	1	1	1
PCE (%)	42	69	53	67.5	70	75.34	77.8
Vin (V)	0.5	0.8	0.7	-	-	0.6	0.6
Vout (V)	1.2	0.5	0.39	0.6	0.38	0.27	0.4
R_L (kΩ)	250	2	2	10	10	2	10
CL (pF)	-	200	200	1.13	2	200	2

The performances comparisons of referenced architectures are given in Table 3. It can be seen that the given CNTFET architecture provides 77.8% PCE with a low input strength (0.6V) and high input frequency (953MHz).

Earlier, we used diode based full wave rectifier. After that diode-tied MOS transistors replaced diode based transistor because implementation of diede-tied MOS transistors are easy in standard CMOS process. The switching transistors stills have significant threshold voltages which causes voltage drop across it. The overall power conversion efficiency reduced and hence the output voltage because of this voltage drop. The PCE is a prime performance metric of a rectifier used in RF to DC converter circuits. The rectifiers are non linear circuits. Its PCE is depending upon the input signal strength and input signal frequency. The PCE is decreasing with the decrease in input signal strength. Therefore at low input signal strength, the input impedance increased and reduces the power conversion. But this circuit works satisfactory and provides very good PCE (77.7%) at low input signal (0.6V) strength. Parasitic resistance also becomes more prominent at high input frequency because of skin effects and introduced more power loss. Therefore, with the increase in input frequency the PCE is getting reduced. But the working of this rectifier circuit is also validated at high input frequency (953MHz). This rectifier provides very good power conversion efficiency at high input frequency. The characteristics of the state of the art rectifier have different feature sizes and processes. Therefore it is difficult to compare all reported characteristics, however among the referenced CMOS architecture the power conversion efficiency is comparably better for CNTFET based rectifier. In a wireless energy harvesting network, antenna characteristics can be a significant factor to limit the power conversion and voltage conversion of the rectifier. Therefore, the antenna characteristics may also be taken for the analysis in further research.

V. CONCLUSION

Threshold voltage compensation introduced auxiliary circuit and the reductions in leakage because of CNTFET are the two aspects on which this architecture is based.

P-type transistors in biasing circuit improve the reduction in dynamic threshold which results in the improvement in PCE of the given rectifier architecture at low input signal. The proposed CNTFET architecture use Stanford model for simulation and the simulated result is showing that that the PCE obtained with this rectifier architecture is very good at high input frequency range.

REFERENCES

1. Q. Li, J. Wang, and Y. Inoue, "A high efficiency CMOS rectifier with ON-OFF response compensation for wireless power transfer in biomedical applications," IEEE Int. Symp. Integr. Circuits, pp. 91– 94, Dec.2014.
2. Khan M, Singh AK, Iqbal SS, " SPICE Simulation of Implantable Solar Power Supply for Sustainable Operation of Cardiac Biosensors" International Journal of Biomedical Engineering and Technology 2015; 18(2): 168-185
3. Khan. M, Zaheeruddin, Singh AK,"Solar cell based DC-DC boost converter for implantable cardiac pacemaker: a computer simulation"International Journal of Biomedical Engineering and Technology 2013; 12 (3): 215-227.
4. M. Xia and S. Aïssa, "On the Efficiency of Far-Field Wireless Power Transfer," IEEE Transactions on Signal Processing, vol. 63, no. 11, pp. 2835–2847, 2015.
5. P. S. Yedavalli, T. Riihonen, X. Wang, and J. M. Rabaey, "Far-Field RF Wireless Power Transfer with Blind Adaptive Beamforming for Internet of Things Devices," IEEE Access, vol. 5, pp. 1743–1752, 2017.
6. O. J. Stavros V. Georgakopoulos, "Wireless Power Transfer in Concrete Via Strongly Coupled Magnetic Resonance," Journal of Chemical Information and Modeling, vol. 53, no. 9, pp. 1689–1699, 2013.
7. Z. Hameed and K. Moez, "A 3.2 V −15 dBm adaptive threshold-voltage compensated RF energy harvester in 130 nm CMOS,"IEEE Trans. on Circuits and Syst. I Regular Papers, vol. 62, no. 4, pp. 948–956, Apr. 2015.
8. S. S. Chouhan and K. Halonen, "Threshold voltage compensation scheme for RF-to-DC converter used in RFID applications," Electron. Lett., vol. 51, no. 12, pp. 892–894, May 2015
9. Y. Chang, S. S. Chouhan, and K. Halonen, "A scheme to improve PCE of differential-drive CMOS rectifier for low RF input power," Analog Integrated Circuits and Signal Processing, vol. 90, no. 1, pp. 113–124, Jan. 2017.
10. L. Zöscher, P. Herkess, J. Grosinger, U. Muehlmann, D. Amschl, H. Watzinger, and W. Bösch, "Threshold voltage compensated RF-DC power converters in a 40 nm CMOS technology," in Proc. of Austrochip Workshop on Microelectronics, pp. 30-34, Oct. 2016.
11. S. S. Hashemi, M. Sawan, and Y. Savaria, "A high-efficiency low-voltage CMOS rectifier for harvesting energy in implantable devices," IEEE Trans. on Biomed. Circuits and Syst., vol. 6, no. 4, pp. 326–335, Aug. 2012.
12. S. R. Khan and G. Choi, "High efficiency CMOS rectifier with minimized leakage and threshold cancellation features for low power bio-implants," Journal of Microelectronics, vol. 66, pp. 67–75, Aug. 2017.
13. K. Kotani, A. Sasaki, and T. Ito, "High-efficiency differential-drive CMOS rectifier for UHF RFIDs," IEEE J. of Solid-State Circuits, vol. 44, no. 11, pp. 3011–3018, Nov. 2009
14. M. M. Mohamed et al., "High-Efficiency CMOS RF-to-DC Rectifier Based on Dynamic Threshold Reduction Technique for Wireless Charging Applications," in IEEE Access, vol. 6, pp. 46826-46832, 2018.
15. J. Deng and H.-S. P. Wong, "A circuit-compatible SPICE model for enhancement mode carbon nanotube field effect transistors," in Proceedings of International Conference Simulation of Semiconductor Processes and Devices, pp. 166–169,Monterey, CA, USA, September 2006.
16. J. Deng and H. S. P. Wong, "A compact SPICE model for carbon nanotube field effect transistors including nonidealities and its application—Part II: full device model and circuit performance benchmarking," IEEE Transactions Electron Devices, vol. 54, no. 12, pp. 3195–3205, 2007.
17. P. L. McEuen, M. S. Fuhrer, and H. Park, "Single-walled carbon nanotube electronic," IEEE Transactions on Nanotechnology,vol. 1, no. 1, pp. 78–85, 2002.
18. B. Q. Wei, R. Vajtai, and P. M. Ajayan, "Reliability and current carrying capability of carbon nanotube," Applied Physics Letters, vol. 79, no. 8, pp. 1172–1174, 2001.
19. P. Dwivedi, K. Kumar, and A. Islam, "Comparative study of subthreshold leakage in CNFET and MOSFET @ 32-nm technology node," in Proceedings of International Conference on Microelectronics, Computing and Communications (MicroCom), Durgapur, India, January 2016.
20. M. Tauheed Khan, Munna Khan, Mohd Hasan "A Low Voltage High Efficiency CNTFET Based Rectifier for Wirelessly Power Up of Biomedical Implantable Devices" International Journal of Scientific Research and Review, Volume 7, Issue 11, 2018, ISSN NO: 2279-543X/page No. 93-103
21. F. Rahman, "Performance evaluation of a 32-nm CNTOPAMP:design, characteristic optimization and comparison with CMOS technology," in Proceedings of 14th International Conference on Computer and Information Technology (ICCIT, 2011), Dhaka, Bangladesh, December 2011.
22. M. A. Kafeel, M. Hasan, M. Shah Alam, A. Kumar, S. Prasad, and A. Islam, "Performance evaluation of CNFET based operational amplifier at technology node beyond 45-nm," in Proceedings of Annual IEEE India Conference, INDICON, Mumbai, India, December 2013.
23. M. Tauheed Khan, Munna Khan, Mohd Hasan," Low Voltage CNFET Rectifier for Wirelessly Power Up Of Implantable Devices" International Journal of Research and Analytical Reviews, Volume 5, April 2018, E-ISSN 2348 –1269, Print ISSN 2349-5138/Page No.-126-132
24. V. Bendre, A. K. Kureshi, and S. Waykole, "A low power, high swing and robust folded cascode amplifier at deep submicron technology," in Proceedings of 3rd International Conference on Information and Communication Technology for Competitive Strategies, Udaipur, India, December 2017.
25. M. T. Khan, M. Khan and M. Hasan, "High frequency low voltage 32nm node CMOS rectifier for energy harvesting in implantable devices," 2015 Annual IEEE India Conference (INDICON), New Delhi, 2015, pp. 1-4

AUTHORS PROFILE

Munna Khan is a Professor at Jamia Millia Islamia, India and worked as visiting Professor at USA. Prof Khan is recipient many awards and published more than 167 research papers in International/National journals and conferences. Dr. Khan supervised 10 Ph.D. students and worked on 3 projects.

Dr. Khan is a Fellow of AsMA, USA and ISAM India. Dr. Khan was research consultant of US Air Force and a reviewer for International/National journals. He has completed three R & D projects from Govt. of India. Dr. Khan is an active member of IEEE EMB, USA and life member of BME and ISTE India.

Mohd Tauheed Khan is a PhD student at the department of Electrical Engineering in Jamia Millia Islamia University, New Delhi, India. He finished his Master study in Electronic Circuits and Systems Design from Aligarh Muslim University, Aligarh India and obtained his Bachelor's degree in Electronics and Communication Engineering. He has published 11 research papers in national/international journals and conferences. His research interests are in VLSI design, Nanoelectronics and biomedical electronics.

Prof. Mohd Hasan profile Prof. Hasan has been working as a full Professor since March, 2005. He served as Chairman (HoD) of the Department from 12 Oct., 2015 to 11 Oct., 2018. He completed his PhD from the University of Edinburgh, UK on a Commonwealth Scholarship in the area of "Low Power Architectures for Signal Processing and Communications". He also worked as a Visiting Researcher on his own Royal Academy of Engineering, UK funded project on "Low Power FPGA' in the same University. He has published 161 papers in refereed journals and conferences with 1327 citations, h-index=19 and i10 index=44. This also includes fifteen IEEE Transactions/Journals and 47 Scopus indexed journal publications. He received "Paper of the Year Award" by the Editors of the famous International ETRI Journal for his paper entitled "High Performance Low power FFT cores" along with a best International conference paper award.

He has supervised six PhDs and currently supervising four more along with many M.Tech. Dissertations. He has delivered several keynote addresses and invited talks in Conferences and Workshops. He has filed three patents on the design of magnetic RAM (MRAM) and one patent on robust SRAM. His research interests are in VLSI Design, Nanoelectronics, Ultra low power design, Spintronics, Battery-less electronics, Variability aware design. He is also a Senior member of IEEE.