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Design And Implementation of Low-Power, High-Performance 2-4- and 4-16-Line Decoders using Adiabatic Logic Circuits

B. Srikanth, M. Sri Hari, D. Praveen Kumar, G. Shravan Kumar

Abstract*: In the present emerging field for the research, the reduction of power has become a major design problem in VLSI technology. As the size of the system shrinking gradually it has become the one the prime concerns in the design of decoders. The main purpose of this paper is to minimize the power and delay capabilities comparison with ordinary CMOS design. To avoid power reduction by introducing a different technique. In this paper we are approaching the adiabatic circuit has been introduced. The power dissipation in the adiabatic circuits can be minimized when compared to conventional CMOS logic. The designing of decoders with the adiabatic logic can reduce the power average power by 10.80% and delay by 21%, 23% and 24% at different voltage levels compared to the conventional CMOS. Finally, Spice simulation results show the comparison results between the existing CMOS decoders and the proposed adiabatic logic-based decoders at 32nm technology in all cases.

Keywords: CMOS Logic, Line Decoders, Adiabatic Logic, Low-Power, Performance, and Simulations.

I. INTRODUCTION

The CMOS logic has an emerging field in the current generation. The major purpose of this paper is to understand various types of combinational circuits with low power consumption by using CMOS circuits [1]. The majority of logic gates are designed by CMOS Circuits. These CMOS circuits contain the pullup and pulldown network.

These CMOS circuits are used because of better performance and resistance to noise in the circuits. Therefore, CMOS logics are identified by quality, transistor sizing and voltage shrinking, thus the design will offer a yield at lower voltages and the reduction of transistor length offers design complexity and increasing the performance [2]. Basically, CMOS circuits are better to noise immune and they have less static power. After that, a new designed Pass-transistor logic has been developed since 1990 [3-6], in order to give a variable different from CMOS logic and better speed, power, and area. Pass transistor logic is used alternative to CMOS logic. When coming to an adiabatic logic technique for normal decoders, integrate various types of logic gates with similar designs, with an attempt to acquire better robustness and minimize the power dissipation contrasted with exclusive existed design. The existing decoders are essential devices, often utilized by the interfacing circuits of storage elements such as multiplexed designs, execution of combination logic functions and various usages. The rest of the remaining paper as follows in order: Section-II provides a Literature survey on Line Decoders. Section-III provides an overview of existing work, Section-IV contains a problem statement. Section-V contains Proposed Design Methodology, Section-VI contain Results and Discussions, Section-VII contains Future Scope. Section-VIII provides a summary of the final conclusion followed by References.

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II. LITERATURE SURVEY

As far as in the current generation especially in VLSI technology, the biggest problem was power reduction. To achieve low power is the major concern in the digital systems. A new type of design was introduced for the 2-4 decoders point on minimizing gate count and achieve low power. A newly proposed method by utilizing mixed logic line decoders. A variation of relative spice simulations at 32nm technology displays the advanced circuits by D.Balabas and N.Konofaos [3].

The designing of Decoder circuits has been going on in the research for the past few years. Various designs have been implemented to design the decoders. One of the best methods to design the decoders are reversible logic gates. The concept is explained using reverse decoder by making use of Fredkin gates and Feynman gates with a minimum quantum cost. In recent days the reverse logic is used in its applications like Quantum computing, optical computing, Nanotechnology, Low power VLSI. The main feature of it is the property of low power consumption by Gopi Chand Naguboina, K. Anusudha[4]. The novelty in the current paper presents a new design logic structure decoder for base decoders, joining to get a new logic design like TLG, PTG, and DVL. In this, a new technique is introduced which is a GDI technique. GDI gate diffusion technique to design low power combinational circuits where we can overcome disadvantages of CMOS.

GDI methodology useful for power reduction, delay and maintains the low complexity of designs by A. Morgenshtein, A. Fish, I. A. Wagner, [5].

In the past few decades, the designers are facing a major issued with the power dissipation in the latest technology. As the demand is very high for the low power devices and integrated circuits require less power to achieve better performance throughput. As the size of the system shrinks gradually it has become one of the prime concerns for the designers. When compared to ordinary CMOS circuits the reduction of power in adiabatic circuits can be more than 90%. In the adiabatic circuit, the charge stored in the load capacitor is recovered while in conventional CMOS it is transferred to ground which caused wastage of energy by A. G. Dickinson and J. S. Denker [6].

III. EXISTING WORK

In digital systems, the information is represented in the form of binary bits. The digital data can be represented in terms of 2^n defined components of given binary information. Actually, these decoders are also called as address generators. If n-bit coded details had unutilized combinations. The circuit analyzed in this work is n-to 2^n decoders. The motive behind the decoder is to generate minterms of n data lines.

A. 2-4 Line Decoder

The design of 2-4 decoder produces the 4 minterms $D_0 - D_3$ of 2 data lines A and B. Its logical function was confidence in Truth Table I. Controlled upon the data lines information, in the given circuit based upon the selected inputs at a time anyone output is selected and generates as output 1 and the rest of the output terms are 0. A 2-to-4 inverting decoder creates the inverting output terms $I_0 - I_3$ in a way, depending upon the input variables the outputs are being set to zero and the rest of the terms are one in the given truth table II.

INPUTS		OUTPUTS			
A	B	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Table I. Truth Table of 2-4 Decoder

INPUTS		OUTPUTS			
A	B	I_0	I_1	I_2	I_3
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

Table II. Truth Table of 2-4 Inverting Decoder

As a matter of fact, in the ordinary CMOS design, the universal gates which are NAND and NOR gates are better than AND and OR gates, whereas they can be executed with the smaller number of transistors. In this manner the usage of the combinational circuit with better outperformance. The design of 2-4 decoder can also be constructed with a minimum of 6 gates which are inverters and NOR gates in Fig. 1(a). The relating type of decoders likewise are executed with 6 gates utilizing 2 inverters and 4 NAND gates, were appeared in Fig. 1(b). The structuring of decoders with NAND gates gives high effectiveness and less power consumption with NOR gates.

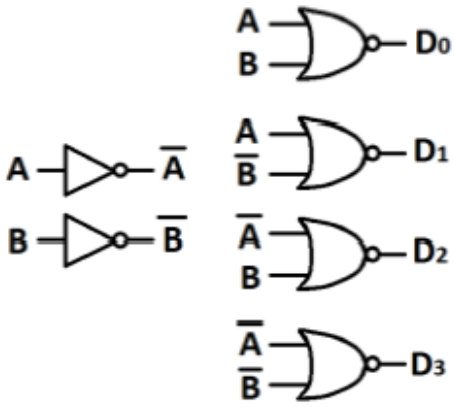


Fig. 1(a). Non-Inverting NOR Decoder

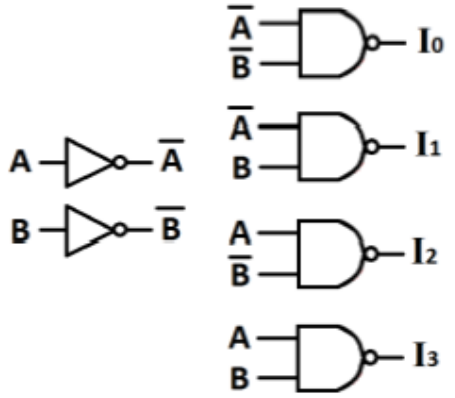


Fig. 1(b). Inverting NAND Decoder

B. 4-16 Line-Decoder with 2-4 Predecoders

Up to now, we have seen the 2-4-line decoder which is having the 2 inputs and 4 output combinations respectively. Presently, n-to- 2^n which contain the 4 inputs and 16 output lines from $D_0 - D_{15}$ of 4 input factors. Whereas another type of decoder which also contain the 4 inputs and 16 output lines with the inverting outputs $I_0 - I_{15}$. A straight forward execution of the design would require 4 input NOR and NAND gates. but, the progressively effective structure can become by utilizing a pre-decoding strategy [1]. The execution of 4 input and 16 output decoders can be designed by 2 inverting decoders and 16 2 input NOR gates as shown in Fig. 2(a) and another upsetting decoder will be executed with 2 2-4 decoders and 16 2input NAND gates as shown in Fig. 2(b).

C. Mixed Logic Designs

In digital logic circuits, the TGL gates have generally utilized in XOR-based circuits. In any case, we consider their utilization in the usage of AND/OR logic, and they can be used in the design of decoder circuits [9]. The two-terminal input Transmission Gate Logic combinational AND/OR circuits is shown in 3(a) and 3(b) accordingly. With respect to [7], new fundamental design methods that utilize only Pass transistors circuits like CPL and those that utilize both nMOS

and pMOS Pass transistors, as Double Pass Logic [8] and Dual Value Logic [9] individually.

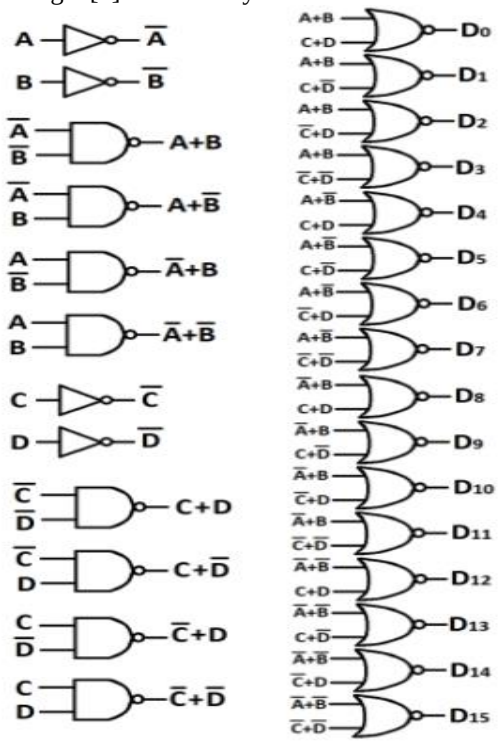


Fig. 2(a). Implementation of Non-inverting Decoder with 2-4 predecoders and a NOR-based post decoder

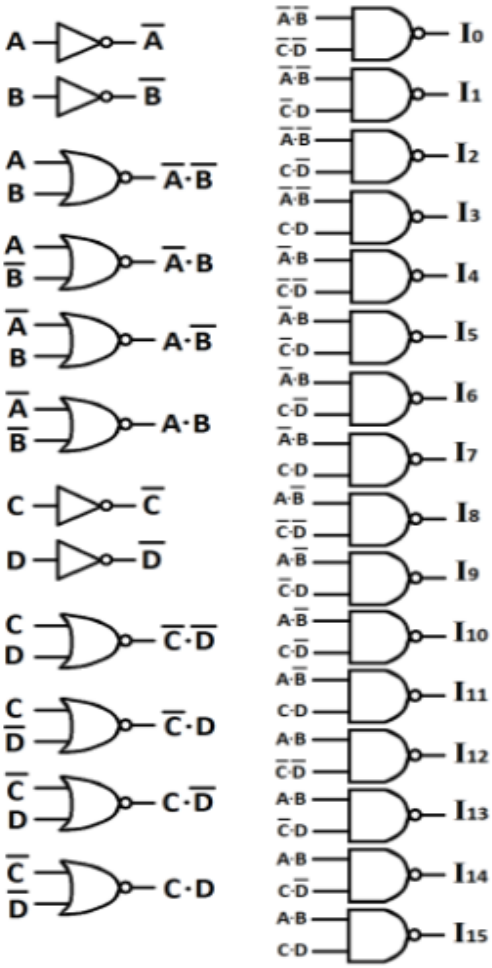


Fig. 2(b). Implementation of NAND based postdecoder with 2-4 inverting predecoders and inverting decoder

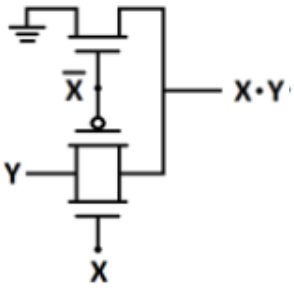


Fig. 3(a). TGL AND gate

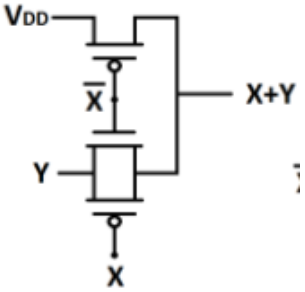


Fig. 3(b). TGL OR Gate

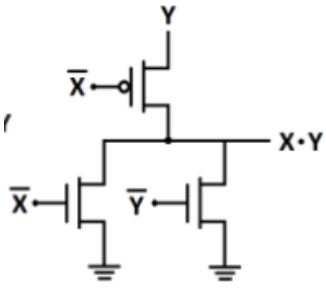


Fig. 3(c). DVL AND Gate

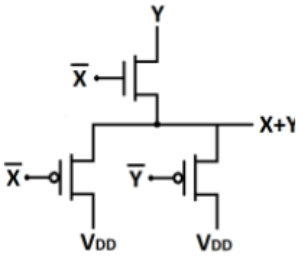


Fig. 3(d). DVL OR Gate

Expecting to the corresponding input sources which are contained in the Transmission Logic gates and Dual Value Logic gates need just three transistors instead of 4 need in the conventional CMOS circuits. Decoder circuits are very high fanout circuits where fewer inverters can be utilized by different gates, in this way utilization of the TGL.DVL gates will result in reducing the transistor count.

A significant normal for these combinational circuits is their uneven behavior. The circuits which contain in Fig. 3 are unbalanced terminal nodes. As we know that there are two input terminals for each gate which are X and Y. Actually, the operation of the Transmission Logic Gates are the input terminals X and Y. The X terminal operates each of the gate inputs of the three transistors in the circuit. Whereas another input terminal Y spreads to the yield moving to the TGL gate.

Another type of logic gate is Dual Value Logic which also contains the input terminals which are available at the TGL gate. Now one of the gate terminals operates two transistors in the circuit. Whereas another terminal operates one gate input and passes from the PTL to yield. These input terminals contribute as the operating signals and they spread signals of the terminals, separately. The uneven nature gives an engineer the variability to carry out the signal position of action where the gate input terminal utilized as an operating signal and propagate in every terminal. Considering an integral contribution, they propagate through the given terminals.

Accordingly, while finishing the confinement or proposition outputs in additional proficient in selecting the complementary variables as an operating signal. While understanding the and operation and or operation which results in (AB) and (A+B).

IV. PROBLEM STATEMENT

The design of Logical circuits has been undergoing investigation for the past few years. Various design methodology is designed for the digital logic circuits like encoders and decoders etc., are designed by CMOS circuits. The main disadvantage with the CMOS circuits is leakage power is very high and it consumes more power than the adiabatic circuits. To overcome the disadvantages in the CMOS circuits we are going for the adiabatic circuits which are having less leakage and lesser delay. From the existing work, we came to know that adiabatic circuits are superior to the CMOS circuits. The Adiabatic circuits are well known as power reduction circuits and give the high yield. The leakage power also very less in the circuits.

V. PROPOSED DESIGN METHODOLOGY

The design of low power circuits is one of the significant worries in VLSI structure. At first, it was anything but a small issue in any case, as the system size is reducing from the most recent couple of years it has become significant for designers. The developing interest for versatile electronic gadgets like mobiles, PCs require energy-efficient productive power sources with little size. Despite the fact that CMOS gadgets are very Power inviting however minimization of dynamic power dissipation is a major challenge. During charging transfer of charge occurs between V_{dd} and the load capacitance C_L i.e. an Energy $E = C_L Vdd^2$ of is transferred from V_{dd} to C_L. The adiabatic technique is better well known for energy-efficient technologies for low power VLSI designs. Adiabatic logic works on the charge recovery principle by which energy is recycled instead of dissipation.

Operation of Adiabatic Logic:

The term adiabatic is started from a word that is used to analyze the thermodynamic procedure in which no trade of energy happens between the system and the outside environment. However, in reasonable processing, such perfect conditions cannot be accomplished because of the nearness of dissipative components like resistances. Anyhow one can achieve less power reduction by increasing the speed of operation and just turning on the gates under given conditions. The adiabatic logic is otherwise called energy recovery CMOS [10]. In writing, the new type of adiabatic circuits has been implemented in this paper which are full swing adiabatic and semi swing adiabatic circuits. In generally two types of power dissipation occurs in the adiabatic circuit. There are two losses are occurring in the design which is adiabatic loss and non-adiabatic loss in the given paper. Adiabatic losses occur due to the switching resistance of transistors while current pass from the transistors whereas in non-adiabatic losses happen due to V_t.

In this paper, we are discussing new types of adiabatic circuits. They are Positive Feedback Adiabatic Logic (PFAL). The PFAL is designed with inverters in back to back connection. We will discuss the PFAL briefly later. Another type of Adiabatic circuit is the Efficient Charge Recovery Logic (ECRL) [11]. Both these designs are controlled in the quad-phase power supply.

The adiabatic logic loads the output state when the input signal decreases gradually. In ECRL design cascaded back to back PMOS pair is used which is based on the Cathode Voltage Switch Logic (CVSL).

Adiabatic logic families:

A. Positive Feedback Adiabatic Logic Family:

The PFAL [12] is a dual-rail build logic circuit developed by using the back to back connections of inverters in the given figure. The supply voltage is getting from the power-clock instead of static supply. This circuit is designed by using the pmos and nmos transistors which are cross-coupled each other and connected between power and output terminal [13]. Regarding the given information the inputs are given to the nmos transistors and they produce a low resistance between power-clock and output. The non-asserted way produces a high impedance. At some point, the voltage between the two given points is very high such that the activity is carryout. By using this procedure, we can increase the output performance. Hence, due to this activity the leakage power will be very less. PFAL demonstrates that better performances are available compared to CMOS logic.

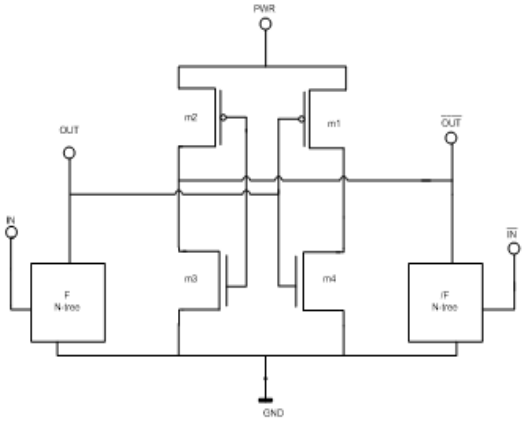


Fig. 4(a) Adiabatic Logic with Positive Feedback

B. ECRL-Efficient Charge Recovery Logic:

ECRL is another type of technique that is designed with the cross-coupled pMOS transistors. This Charge Efficient Recovery Logic was developed by back to back connection of pMOS in the circuit. The inputs are taken at the nMOS transistors. To get the supply for the output we have to replace the AC power source utilized at the gates. The clock generator generates the constant output capacitance independent of level adjustment in inputs. Full output floating is acquired as a consequence due to the feedback connection of PMOS transistors in two scenarios which are precharge and recapture stage. The design expertise in non-adiabatic misfortune in precharge and recapture due to the V_t of the PMOS. However, due to the threshold voltage, the ECRL consistently force charge on the output of a full swing.

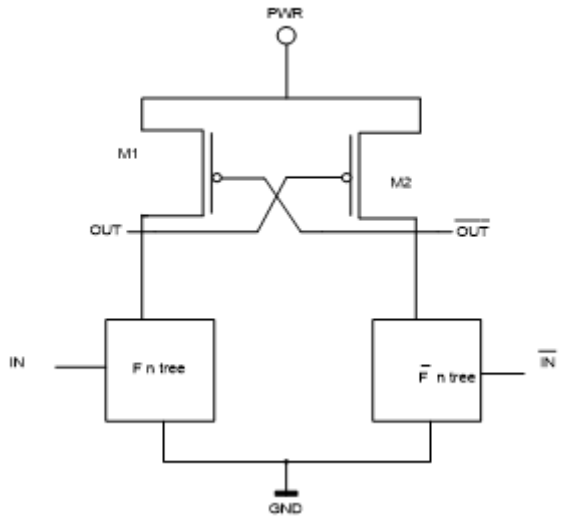


Fig. 4(b). Efficient Charge Recovery Logic

During the exchanging procedure, the logic circuit minimizes the leakage power and utilize a few some portion of the energy by reusing it from the load capacitance.

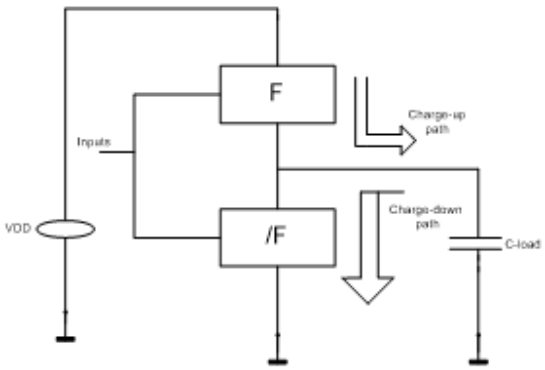


Fig. 4(c). Charging and Discharging in Conventional System

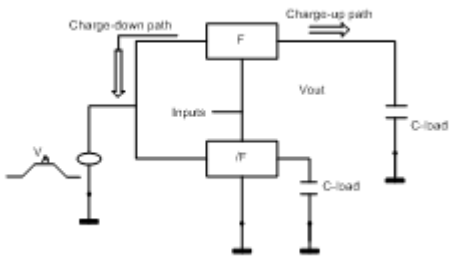


Fig. 4(d). Charging and Discharging in Adiabatic System

Adiabatic logic was essentially made for low power applications. These circuits are efficient in recovering the energy back to the input, with the goal the same energy could be utilized for the upcoming activity. The changing and reordering of charge in ordinary CMOS and Adiabatic logic. [14] [15].

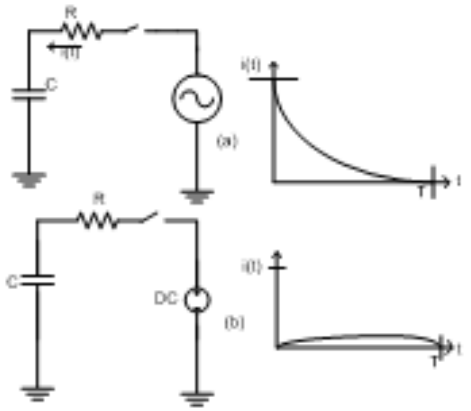


Fig. 4(e). Switching of CMOS Logic and Adiabatic Logic

VI. RESULTS AND DISCUSSIONS

The simulation results in regards to Power, Power Delay Product and Delay are appeared in given tables in consideration of propagation delay is free to that parameter. Regarding each outcome, one of the proposed design structures will be contrasted with its ordinary CMOS parameters, taken into account. The normal outperformance estimations for every situation. As indicated by the procure outputs, 2-4 decoder presents 10.8% less power. Then again, beats CMOS in all characteristics, decreasing power, and delay by 21%, 23% 24%. Both of our inverting structures, better than CMOS in all viewpoints, too. In particular, less power dissipation, delay, and Power Delay Product, individually.

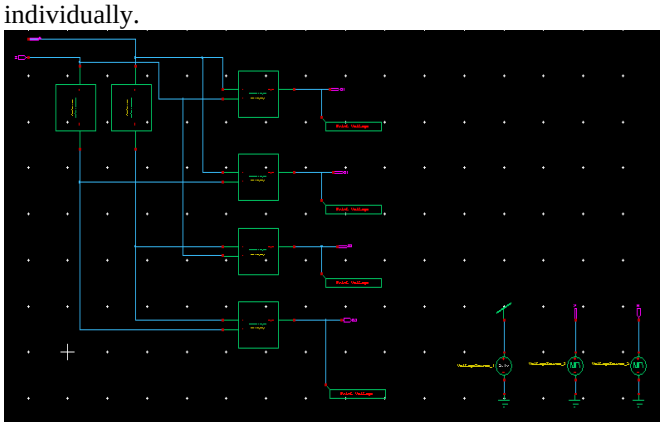


Fig. 6(a). Design of 2-4 Decoder Using Static CMOS

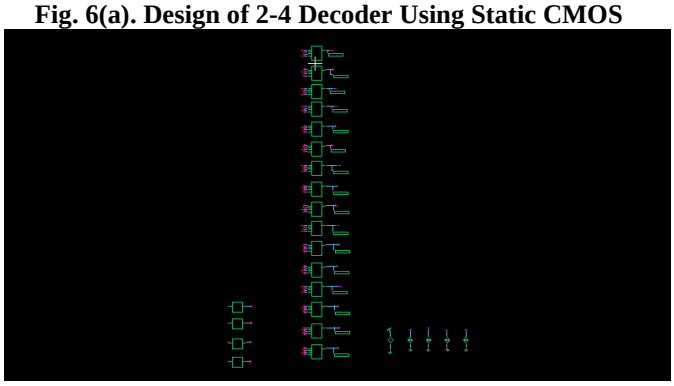


Fig. 6(b). Design of 4-16 Decoder Using Static CMOS

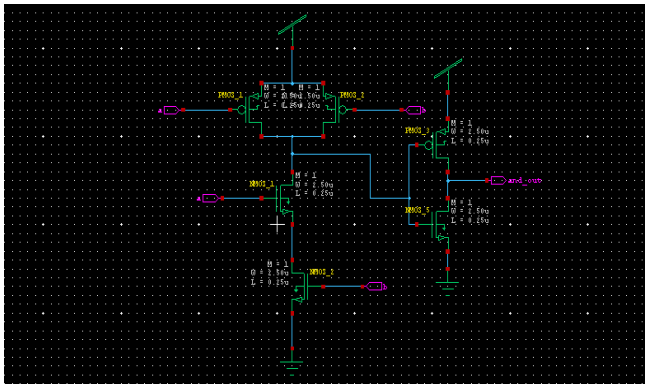


Fig 6(c). Design of Adiabatic AND Logic Circuit

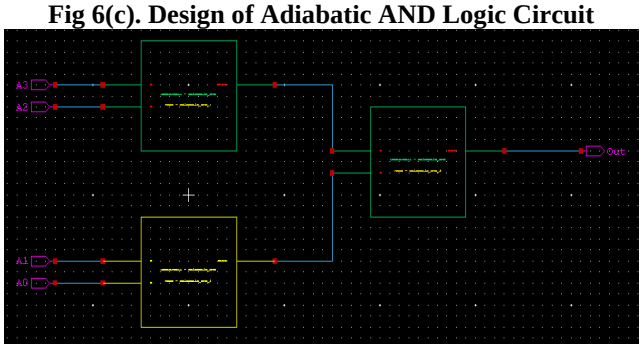


Fig. 6(d). Design of 2-4 Decoder Using Adiabatic Logic gate

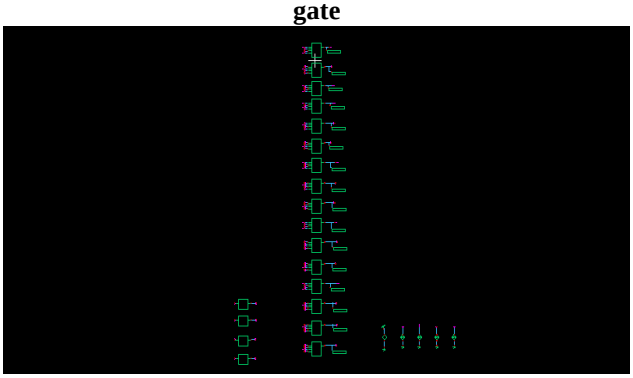


Fig. 6(e). Design of 4-16 Decoder Using Adiabatic Logic Circuit

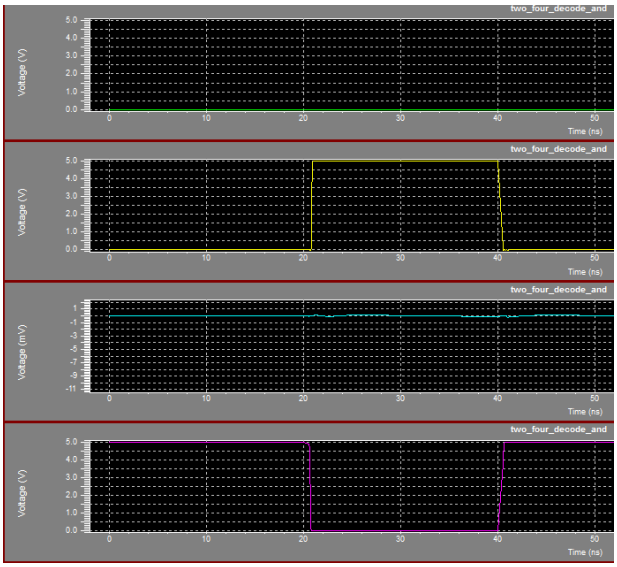


Fig. 6(f). Conventional CMOS 2-4 Decoder

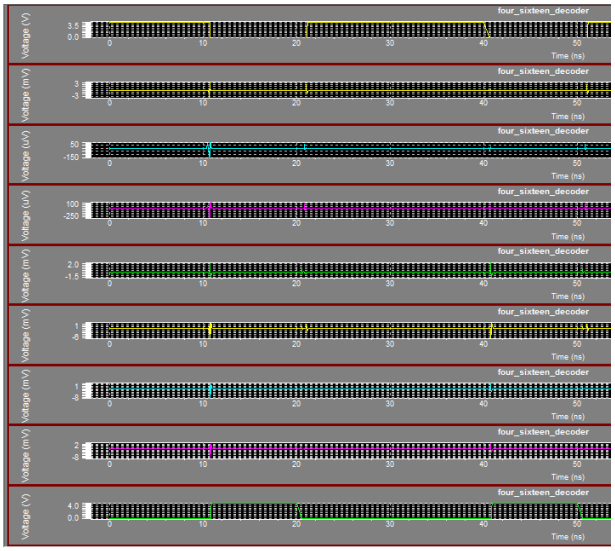


Fig. 6(g). Conventional CMOS 4-16 Decoder

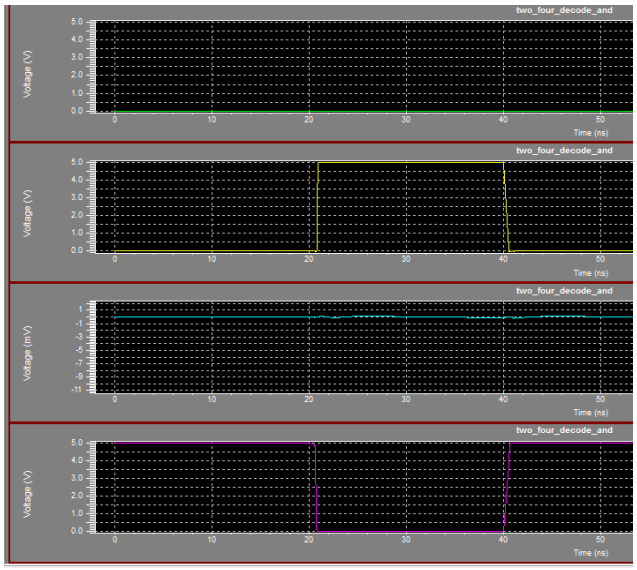


Fig. 6(h). Adiabatic 2-4 Decoder

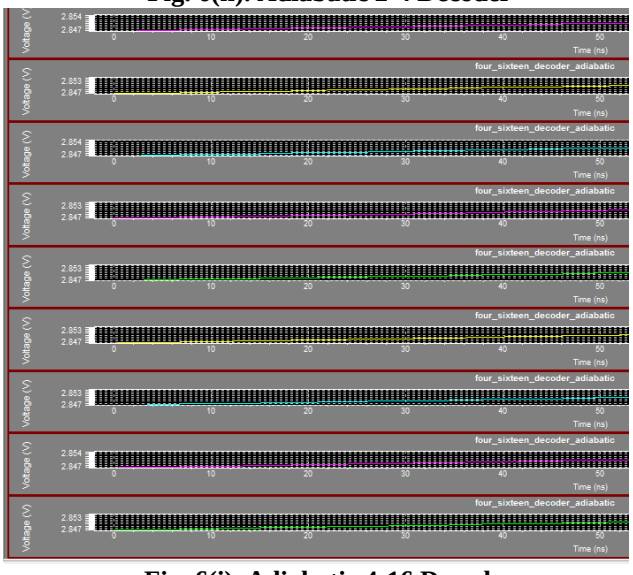


Fig. 6(i). Adiabatic 4-16 Decoder

Table-III Power Results

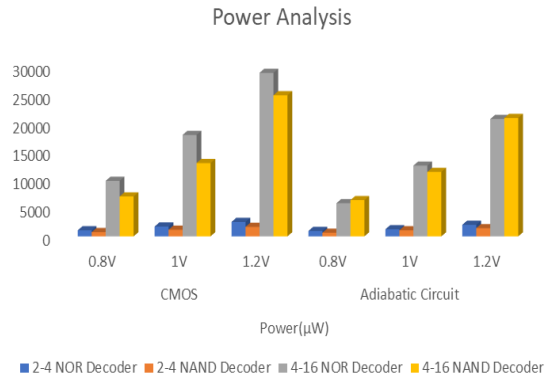
Decoders	Power(µW)					
	CMOS			Adiabatic Circuit		
	0.8V	1V	1.2V	0.8V	1V	1.2V
2-4 NOR Decoder	1074	1745	2564	958	1259	2057
2-4 NAND Decoder	750	1178	1687	643	1085	1458
4-16 NOR Decoder	9866	18034	29076	5897	12578	20879
4-16 NAND Decoder	7094	13040	25091	6450	11459	21056

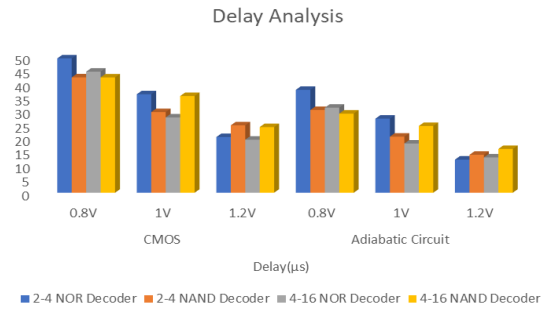
Table-IV Delay Results

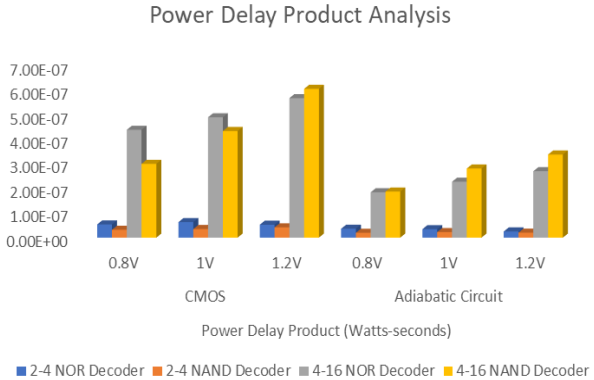
Decoders	Delay(µs)					
	CMOS			Adiabatic Circuit		
	0.8V	1V	1.2V	0.8V	1V	1.2V
2-4 NOR Decoder	49.54	36.33	20.55	37.96	27.33	12.22
2-4 NAND Decoder	42.56	29.75	24.85	30.51	20.69	13.99
4-16 NOR Decoder	44.67	27.78	19.57	31.38	18.15	13.01
4-16 NAND Decoder	42.54	35.66	24.21	29.18	24.62	16.14

Table-V Power Delay Product Result

Decoders	Power Delay Product (Watts-seconds)					
	CMOS			Adiabatic Circuit		
	0.8V	1V	1.2V	0.8V	1V	1.2V
2-4 NOR Decoder	5.36E-8	6.33E-8	5.26E-8	3.63E-8	3.44E-8	2.51E-8
2-4 NAND Decoder	3.19E-8	3.50E-8	4.19E-8	1.96E-8	2.24E-8	2.03E-8
4-16 NOR Decoder	4.40E-7	4.91E-7	5.69E-7	1.85E-7	2.28E-7	2.71E-7
4-16 NAND Decoder	3.01E-7	4.35E-7	6.07E-7	1.88E-7	2.82E-7	3.39E-7







VII. FUTURE SCOPE

The proposed design can be tested for low on-chip power density further. Though we have utilized the pulsed power source efficiently, propagation delay can further be reduced by more efficiently utilizing the pulsed power supply as VDD source. Further, the performance of the proposed schematic may be increased by checking noise margin and current at different nodes. The above circuits show a power decrease contrasted with CMOS. In the future, we will configure circuits utilizing 2N-2N2P, ECRL, PFAL, 2PASCL, CAL and so on. adiabatic logic with the goal that we can get less power dissipation. Hence, we can conclude that the proposed logic is fully adiabatic logic and it is implemented successfully in our design.

VIII. CONCLUSION

In short, from the above work, the adiabatic logic circuit is obtained to get fulfillment dependent on ordinary CMOS circuits. These circuits will work at different types of frequency and with different types of voltages. Due to switching activity in the CMOS the charge leakage will be very high, whereas in the adiabatic circuits the charge will be stored. This is one of the advantages of these circuits. Specifically, the performance of adiabatic switches the designing of decoders with the adiabatic logic can reduce the power average power by 10.80% and delay by 21%, 23% and 24% at different voltage levels compared to the conventional CMOS. At last, it is important to notice that the power dissipation in the adiabatic circuits is very lower than the conventional CMOS particularly for the low to medium circuits that are operating at desired frequencies, where CMOS performs inadequately due to static power loss.

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