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Examination and Design of Bi-Phase Encoder for Short Range Wireless Communication

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Abstract— In today's digital era, Communication systems have become ubiquitous in our everyday life. In data communication various protocols are employed to encode information bits in short range wireless communication technologies. Different types of baseband encoding schemes have been in practice for improving performance of communication which comprises of Manchester, differential Manchester and FMO codes.The transmitted signal is predicted to have zero mean for vigor issue and this is also called as dc balance. The design has been tested in Tanner EDA Tool using different logics such as CMOS logic, Pass Transistor logic and transmission gate logic.

Keywords-CMOS,EDA

I. INTRODUCTION

Short range wireless communication system plays a vital role in our daily life. Some standards like Wi-Fi, Zigbee, Bluetooth, RFID etc[2].have made miracle in many fields like security, medical care, vehicular communication and consumer applications. These technologies employ various physical layer protocols for encoding the information bits. Standard encoding mechanisms includes Manchester encoding, Differential Manchester encoding and FM0encoding[4][6]. This comes under the division of Bi-phase encoding. It operates by changing the transition of signal in the middle of the bit interval; however, the transition of signal continues to the opposite pole and it does not return to zero . It ensures that the signal never retains at logic low or logic high for an long period of time and converts the data signal into a data-plus-synchronization signal. Manchester encoding is the easiest coding mechanisms and has a less probability of error when compared to other encoding techniques. Differential Manchester[1] coding may materialize to be superficially the similar as Manchester encoding. In Differential Manchester encoding the signal transition at the middle of the bit is used for synchronization. FM0 encoding[3][5] is otherwise known as bi-phase space encoding. In this paper, we have designed and tested various encoding schemes such as Manchester, Differential Manchester and FM0 code architectures using different logic styles such as CMOS, Pass transistor and Transmission gate in circuit level. This architecture can be applied in various applications where the system has to switch among distinct encoding schemes. Having individual circuit for each encoding method would devour more resources.

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II. A REVIEW OF CODING SCHEMES

(I) MANCHESTER ENCODING

Manchester encoding [3][5] always has a mid bit transition. The direction of the mid bit transition represent the digital data. A „1" represent positive transition and 0" represent negative transition. This can be obtained by an XOR operation between the input, X and Clock.

Manchester= X (xor) Clock……..(1)

(II) DIFFERENTIAL MANCHESTER ENCODING

Differential Manchester encoding[3][5] is the variation of Manchester encoding. Each bit is obtained by comparing the with the past encoded bit and present input bit. A binary 1 is encoded if opposite state transition between the input bit and the past encoded bit. A binary 0 is encoded if the transistion states are the same.

A+=x ^ a----------(2)

B+ =~(x ^ a)----------(3)

Where $A^+$and B^+ are next state values of A and B

respectively.

Differential Manchester = (clock*A^+) + ((~clock)*B^+)

(iii) FM0 Encoding----------(5)

fm0 =(clock*A^+)+ ((~clock)*

DIFFERENT TRANSISTOR LOGIC SCHEMES (i)CMOS LOGIC

CMOS LOGIC

CMOS (COMPLEMENTARY METAL OXIDE SEMICONDUCTOR)[6] IS A TECHNOLOGY FOR MAKING LOW POWER INTEGRATED CIRCUITS. IT IS A COMPLIMENTARY MIXTURE OF N-TYPE AND P-TYPE TO CONSTRUCT A LOGIC.OUTPUTS ACTIVELY DRIVE BOTH WAYS AND HAS HIGH INPUT IMPEDANCE. CMOS IS FAST, AND CONSUMES LESS POWER

In the FM0 code[3][7], a transition is present in the middle of the bit window when the input bit is „0", whereas there is no transition in the middle of the bit for an input „1". However, there is a transition at the edge of every bit window.

A+=(~b)----------(4)

B+=(x ^ b)----------

than other technologies.

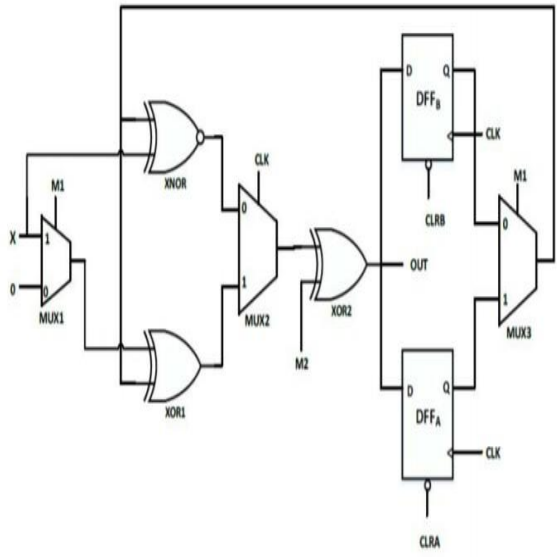
(ii) PASS TRANSISTOR LOGIC

It Reduces the transistor count by eliminating the redundant transistors. In conventional logic input is applied to gate terminals, where as in PTL it is applied to source/drain terminal. The width of the p-mos is equal to n-mos so that both transistors can pass the signal simultaneously in parallel [8-9].

(iii) TRANSMISSION GATE LOGIC

A transmission gate is a parallel connected N-FET/P-FET pair that acts as a logic control switch. Generally, the transmission gate acts as a voltage control resistor connecting the input and the output. It can be used as a logic structure, switch and latch element [10-11].

III. PROPOSED ARCHITECTURE



Manchester:M1=1;M2=1; CLRA=0;CLRB=0

Differential Manchester:M1=1; M2=0; CLRA=1;CLRB=0

FM0:M1=0; M2=1;CLRA=0;CLRB=1

Figure 1. Biphase encoding architecture

The above figure.1 shows bi phase encoding architecture which is designed in circuit level using CMOS, Pass transistor and Transmission gate. The D flip flop (DFF) stores the present state of A. The MUX selects the succeeding values of x or 0 according to the Clock. A mode signal, M and a flip flop clear signal (active low), CLR are used to chosen between Manchester and Differential Manchester encodings. In Manchester mode, CLR is activated feeds a "0" in the place of present value of x and M = 1 which makes XOR_2 act as an inverter. In Differential Manchester mode, CLR=1 and M=0. The present value of axis allowed as input to the succeeding state. XOR_2 function as a buffer. Further, to include FM0 encoding, the architecture is modified as shown in figure. It has a dual bit mode signal M1,M2 and clear signals - CLRA for flip flop DFFA and CLRB for flip flops DFFB. CLRA and CLB are active low. Based on different combinations of the signal transitions, the circuit is switched among different modes of operation. DFFA stores the present value of x and DFFB stores the present value of 0. DFFA is negative edge triggered and DFFB is positive edge triggered. MUX_3 choose the value of A or B to be as input for succeeding state based on the value of M1. FM0 needs the preceding value of x and Differential Manchester / Manchester needs the preceding value of x. However, for Manchester, the value of A becomes "0" by activating CLRA. MUX_1 choose the "0" for FM0 encoding and the value of input X otherwise. The "0"for MUX_1 can also be given by connecting it to the output of DFFA.

IV. RESULTS AND DISCUSSION

The proposed architecture has been tested in Tanner EDA Tool and the simulation waveforms for all the three modes are analyzed. This encoding scheme improves the data protection features of the system at the physical layer level. This work focuses on efficient integration of Manchester/Differential Manchester/ FM0 coding modes on a single architecture and designed in CMOS, pass transistor and transmission gate logic. FM0 and Differential Manchester coding are complex when compared to Manchester coding. Hence the operating frequency of Manchester will be narrowed by the other two modes, which will be higher otherwise.

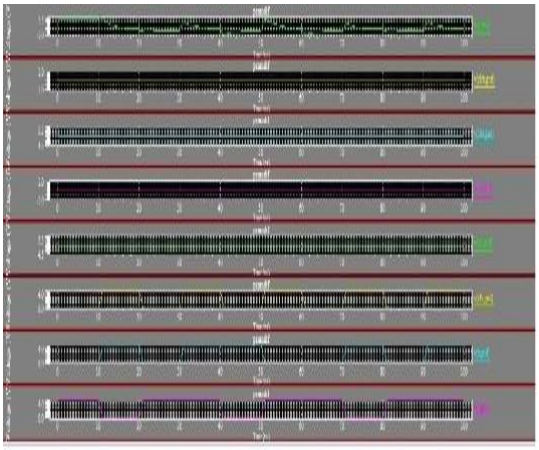


Figure 2 Output Waveform of Manchester

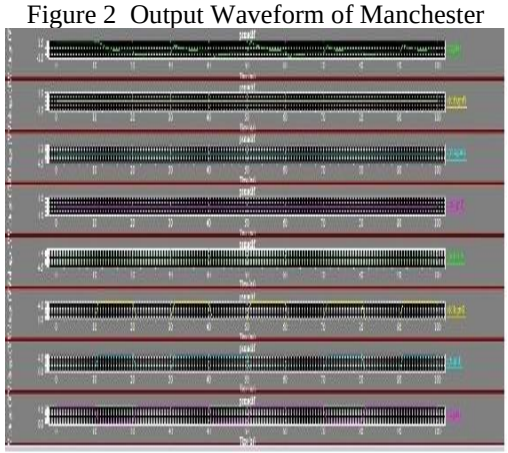


Figure.3. output waveform of Differential Manchester

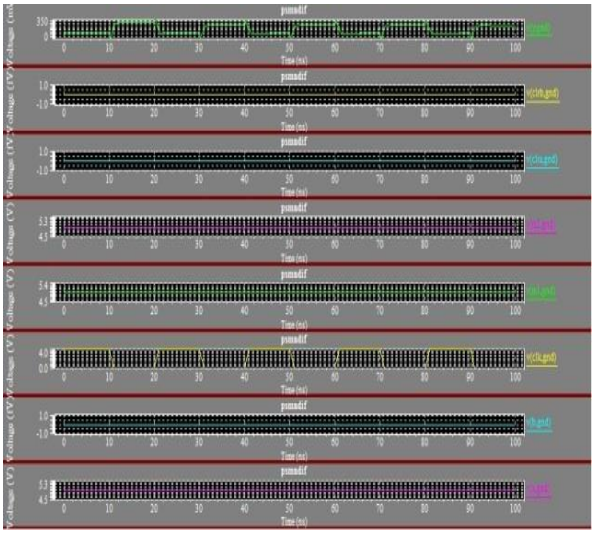


Figure.4. Output Waveform of FM0

V. COMPARISON OF PERFORMANCE

The proposed architecture has been implemented in Tanner EDA tool, the comparisons are shown in the above table. This design is compared among CMOS, Transmission gate and Pass transistor, CMOS consumes 96 transistors with 37mW power utilization and increase in area. When compared to CMOS the number of transistors has been reduced in other logics. In case of Pass transistor active devices is reduced and power consumption is decreased by 18%.

VI. CONCLUSION

A fully integrated VLSI architecture for Manchester, Differential Manchester and FM0 encoding schemes are designed and analysed using CMOS, Pass transistor and Transmission gate. In CMOS and transmission gate it requires more transistors compared to pass transistors and also it requires less power. So when compared to three different logics CMOS, pass transistor and transmission gate. Pass transistor provides better efficiency, achieve synchronization, reduced power consumption and area. This encoding schemes are used in short range wireless communication for improving signal reliability and the architecture is helpful in many applications where the system has to interface between different encoding mechanisms.

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