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Multilevel Inverter Topology with Reduced Number of Switches

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Abstract:-The commencement of multilevel inverter has enamored the researchers owing to its applications for medium and high power. Moreover there has consistently been a necessity for an approach with reduced number of switches. Bearing this in mind, this article presents an asymmetrical multilevel inverter with a switching approach employing reduced number of power electronics equipments. The increase in the level of output, number of switching equipments besides with the switching states enhances. As a consequence, higher switching losses occurs that prompts power loss. Accordingly, the efficiency of the complete conversion network diminishes. The significant characteristics of this submitted work is that the module can be accomplished as sub multiple level assembly. Progressively, with minimal rise in the switching elements, all number of levels can be elongated.

Key words: Multi-level Inverter, Symmetrical & Asymmetrical MLI, THD (Total Harmonic Distortion), Simulation.

I. INTRODUCTION

The research towards power electronics and its applications in the various filed necessitates transformation stages such as from AC to DC or vice versa. Among this, the inverters play a vital role in low and high power applications. The employment of Multi Level Inverters (MLI) with less number of switching equipment's has become the mandatory to interface the power semiconductor devices to the high voltage circuit. At first, the MLI was established in the year of 1975 [1]. Nabae et.al introduced the three level inverter topology [2].

In comparison with two level inverter, MLI have various special features such as diminished voltage stress in the power electronic switches, low level of harmonic distortion, able to function in both fundamental and high switching frequency PWM, more efficiency and less electromagnetic interference. The inputs to the MLI can be supplied either from renewable or conventional DC sources.

The most traditional approaches of MLI are enumerated below:

1. Diode clamped MLI
2. Fly back MLI
3. Cascaded H Bridge MLI

The diode clamped MLI offers multi level voltages via interlinking the phases with the cascaded bank of capacitors. The generalized equation for the number of diodes needed for individual phase is given by (m-1) (m-2), where 'm' is level inverter output. From the equation, it is clear that with the rise in the level of output, the amount of diodes essential becomes complicated. So it is infeasible to execute it practically [3]. In search of flying capacitor MLI, it is found that huge amount of capacitors are mandatory to clamp the voltage.

For a m level converter, the quantity of capacitors for each phase is given by, (m-1) (m-2)/2.

Besides, the number of dc bus capacitors needed is (m-1), Relative with the above said two MLI types, Cascaded H Bridge MLI (CMLI)[4] has been employed by many researchers as it has the capability to prepare more level of output with a predominant spectrum with less cost. In addition to that, this type does not need huge quantity of transformers and clamping diodes. It produces multistep stair case voltage waveform that corresponds to a sinusoidal waveform with the amplification in the number of levels because voltage balancing equipments are not essential.

Furthermore, the MLI with separate DC sources are classified as Symmetric MLI and Asymmetric MLI. Inverter with same amplitude of source is defined as symmetric MLI whereas amplitude of DC voltage sources employed in an asymmetric MLI is not same. In the case of symmetric MLI with independent DC sources (n), the effectual number of output phase voltages is represented by, $N_{level}= 2n +1$.

The asymmetric MLI has dissimilar voltage ratios in binary configuration [5]. It has a ratio of 1:2:4 as powers of two or three [6]. Its voltage ratio is 1: 3: 9 as powers of three [7]. It produces output voltage of 'n' th power of 3 levels.

The rise in voltage level strengthens the quality of the output power, also it necessitates huge number of power semiconductor switching devices besides with gate triggering equipments. On contrary, if the switching equipment's are less in number, simultaneously the voltage level downsides. Several research reveals that THD level for these types of cases is high that shows clearly the low quality of power output delivered to the load.

Concurrently, the complexity of the circuit arises with more levels of output and consequently efficiency level decreases. Keeping this in mind, reducing the complications in the real time implementation, it is fascinating to deplete the number of switches. These outcomes in modulatory and fewer switching loss. Therefore it is preferable disregarding the level of MLI output, if the switches exploited in the circuit arrangement is minimized, it is feasible to mean in between the switches utilized and the number of levels.

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For the sake of lowering the complexity of real time execution, it is mandatory in minimizing the number of switches that has the possibility to generate all odd and even levels at the output voltage. So, it is preferable that by not considering the level of the multilevel inverter output, if the switches employed in the circuit assembly is lowered, then it is feasible to compromise in between the number of output levels and the number of switches exhibited.

So far, various configurations have been submitted [9-13] focusing in the deterioration of reducing the equipments utilized. This reduction will not only enhance the robustness of the circuit, also driver circuits adopted for each switch and anti parallel diodes are decreased. All these benefits will bring the modular circuit configuration that is very compact and also economical one. As a supporting nature, the attentions of this work are extenuating the number of equipments exploited in the symmetrical and asymmetrical circuit. This arrangement can be anticipated as sub multiple level configuration adopting the positive output voltage only with the support of single H bridge circuit.

II. METHODOLOGY

With two dc sources as the input , the proposed work circuit diagrammatic representation is illustrated in figure 1. The multilevel output positive half cycle voltage is produced across AB. This is endorsed by traditional H bridge interpreted by the switches T1 to T4 to generate output in both positive and negative half cycles and fed to the load at last.

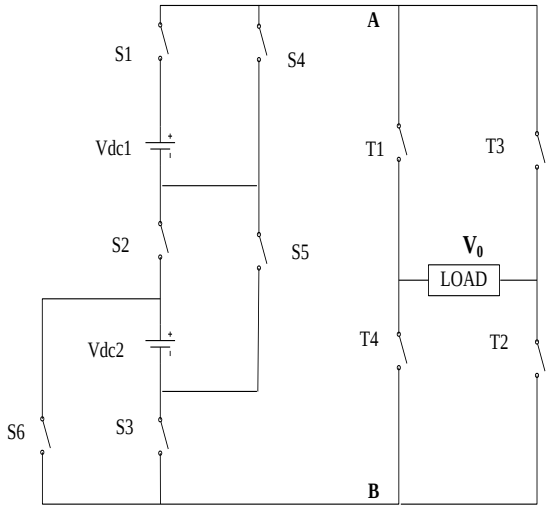

Figure 1. Recommended basic unit fed by two dc sources.

The circuit pictured in figure 1 will have the capability of generating the output at nine distinct levels i.e. four at positive state, four at negative state and one at zero state. Distant switching states and the analogous output for every switching state across AB for all feasible cases is reviewed in table 1 represent ON and 0 represent OFF state of the switching equipment. With same amplitude of dc sources, the measure of output voltage level attenuates and to enhance the voltage levels, asymmetric arrangement voltage sources are chosen. All probable measures of voltage across AB listed in the table 1 when fed H bridge generates both positive and negative outputs at V0.

Table.1. Switching State for a Proposed Unit Fed by 2 Voltage Sources

Mode	S_1	S_2	S_3	S_4	S_5	S_6	V_0
1	0	0	1	1	1	0	0
	0	1	0	1	0	1	
2	1	0	0	0	1	1	V_1-V_2
3	0	1	1	1	0	0	V_2
4	1	0	1	0	1	0	V_1
5	1	1	1	0	0	0	V_1+V_2

The different proportion of the switches are summarized for the output voltage of the recommended arrangement of the MLI in which 1 and 0 indicates ON and OFF conditions of the switching equipment's respectively. When dc voltage sources are chosen with same amplitude (symmetric configuration), the number of output voltage level minimizes and to enhance voltage levels unequal voltage sources (asymmetric configuration) are chosen. Table 1 shows feasible positive levels of voltages across AB. Voltages are fed to the H- Bridge to generate feasible output levels in positive and negative at Vo.

The similar concept can be prolonged for all circuit configurations for a specific number of dc sources for a definite number of switches.

Expected dc voltage sources for the circuit are designated in equation 1 to 3.

$$N_{source} = n \quad (1)$$

$$N_{switch} = 4n-2 \quad (2)$$

$$N_{driver} = N_{switch} = 4n-2 \quad (3)$$

With the dc voltage inputs of asymmetrical MLI having binary relationship is specified in equation 4 to 6.

$$V_{dcn} = 2^{(i-1)}V_{dc} \quad (4)$$

Where i =1, 2, 3,…n.

$$N_{step} = 2^{(n+1)}-1 \quad (5)$$

$$V_{0max} = (2^n -1)\, V_{dc} \quad (6)$$

Asymmetrical MLI with teritary relationship is given in equation 7 to 8.

$$V_{dcn} = 3^{(i-1)}\, V_{dc} \quad (7)$$

Where i=1, 2, 3,…n.

$$N_{step} = 3^n \quad (8)$$

$$V_{0max} = ((3^n -1)/2)\, V_{dc} \quad (9)$$

Through these equations, nine levels of positive output voltage are attained. The similar positive voltage can be acquired through the load enabling the switches T1 and T2 of the H bridge except the zero output voltage, 13 outputs of similar amplitude can be determined by energizing T3 and T4. Table 1 displays the measure of output voltage of the recommended configuration when works at symmetric and asymmetric techniques. Correspondingly, for n number of separate dc sources, for symmetric & asymmetric MLI under both binary and tertiary relationships, output measures can be obtained [14-15].

III. SIMULATION AND EXPERIMENTAL RESULTS

For evaluating the highlighted work, MATLAB/SIMULINK is chosen as the software platform. Switching sequence mentioned in Table 1 is followed. Figure 2 and 3 illustrates the inverter output voltage and current. Quality of output power is measured by calculating THD level of the voltage and current. FFT tool in MATLAB support for this execution. The spectrum output of THD level for both voltage and current is noted down as 9.6% and 5.8% (Figure 4 and 5). MOSFET gate pulses produced is exhibited in figure 6.

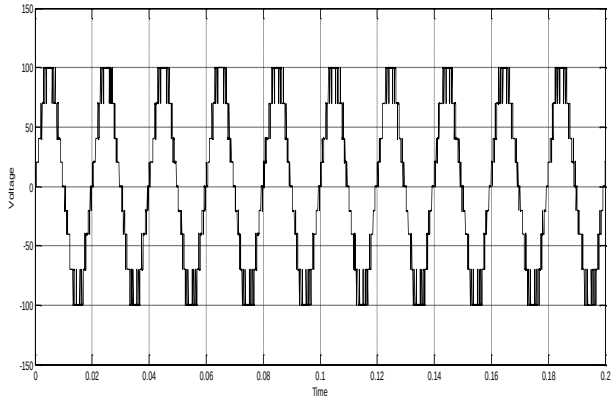

Figure 2. Multilevel inverter output voltage

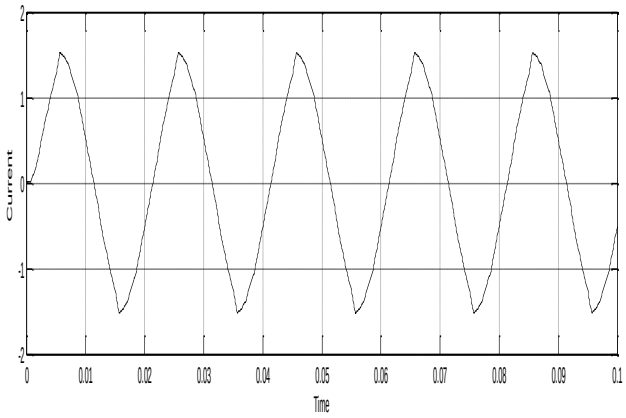

Figure 3. Multilevel inverter output current

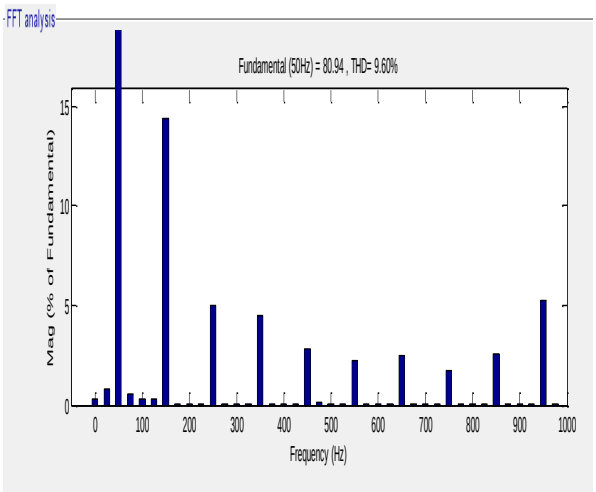

Figure 4. THD of output voltage

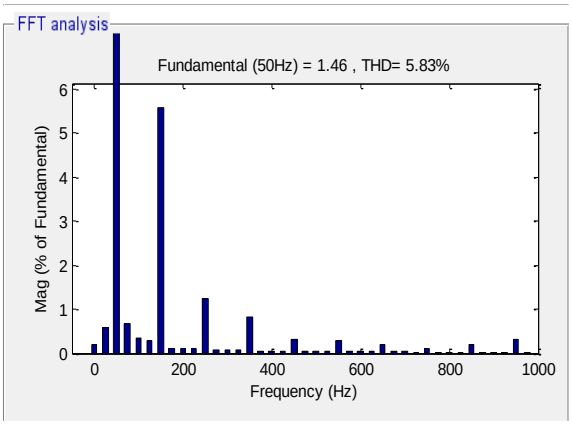

Figure 5. THD of output current

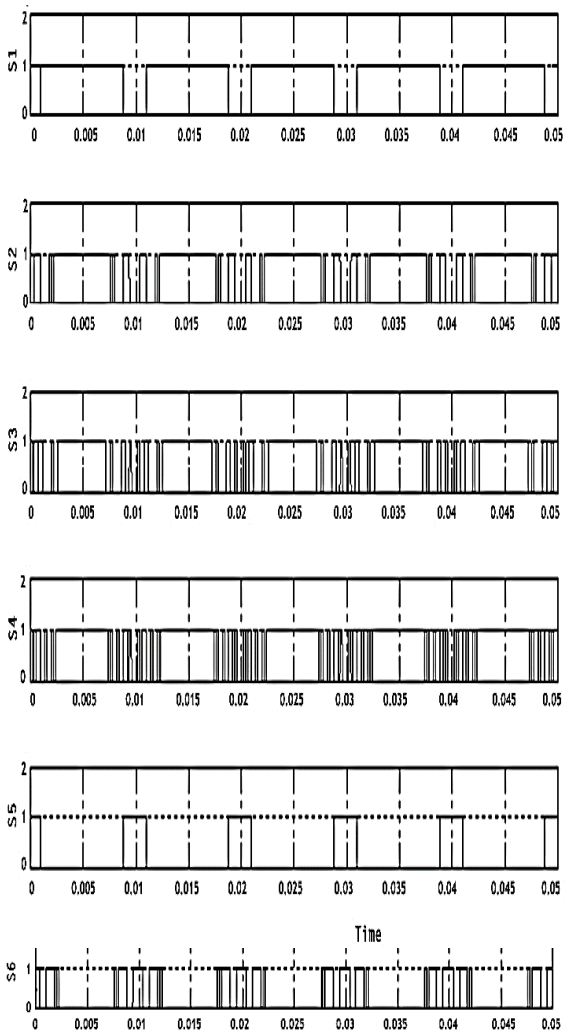

Figure 6. Simulation gate pulse

The experimental set up of the submitted work is equipped with the help of MOSFET IRF 540. ATMEL microcontroller plays a vital role in generating the needed gate pulses for the MOSFET. Two independent Regulated power supply (RPS) act as the dc source. A resistive load is connected along with the inverter. The subsequent hardware results are displayed in figure 7,8 and 9.

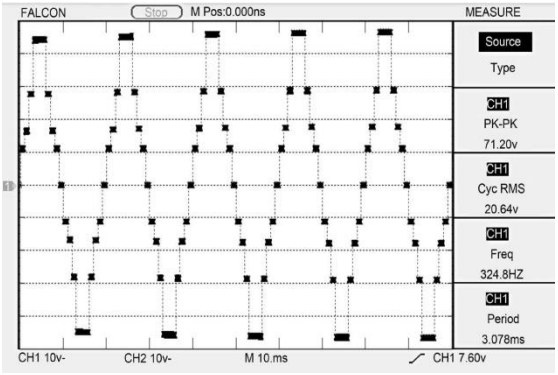

Figure 7. Hardware output voltage

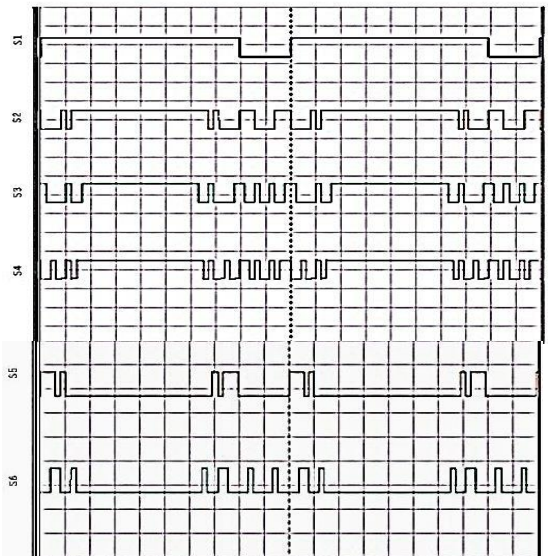

Figure 8. Gate pulse generated by the microcontroller

Figure 9. Hardware prototype

IV. CONCLUSION

In this work, an innovative approach for MLI can be prolonged to 'n' number of levels of positive output voltages is proposed. The similar arrangement can be elongated to derive positive and negative level output. In order to attain quality power in an inverter circuit with reduced switching loss and high efficiency, it is mandatory to diminish the number of switches even for a high MLI. This is focused as the main concern in this work. Symmetrical and asymmetrical categories are analyzed for both binary and tertiary relationship through the employment of H bridge inverter. The simulation and hardware outcomes ensure the quality of the output power through THD measure. It proves clearly that even with diminished number of switches for MLI, the efficiency and modularity are consistently enhanced with less cost.

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