# Design of Dadda and Wallace Tree Multiplier Using Compressor Technique

**S N Shivappriya M., Narmatha, V. Madhusri**

***Abstract- The work portrays about the design of the Dadda multiplier using 4:2 compressor techniques. The three design techniques, namely conventional design, optimized design using exclusive OR with multiplexer and a further optimized design with less number of critical paths with gates are implemented. All the three designs are implemented in Dadda multiplier and wallace tree multiplier and their performances are compared. The performance metrics measured are area, power consumption, delay and transistor count and these parameters are efficient in dadda multiplier compared to wallace tree multiplier with the above three design techniques. The designs are using behavioral modeling and the results are taken in the 180nm Cadence tool. The result shows that the Dadda multiplier performs better in terms of delay, area and transistor count for all three designs than the Wallace tree multiplier.***

***Keywords- Compressor Technique, Dadda multiplier, Wallace tree multiplier, Area, Delay, Transistor count.***

## I. INTRODUCTION

The digital logic circuits are used in various arithmetic applications so as to operate with a high degree of consistency and correctness. Most of the real time applications can indulge errors and inexactness in computational but still can produce related results. Multiplier is one of the most important blocks of hardware. The 4-2 compressor is a broad compressor structure. It can be introduced between neighboring slides with the carrying bit.

The Wallace tree's primary feature is to multiply two unsigned integers. The Wallace tree multiplier consists of AND array for calculating the products, Carry save adder is obtained in the final stage of addition to add the partial products and thus carry propagate adder. The Dadda multiplier performs quicker and the suggested methods are implemented in the Wallace tree multiplier.

## II. RELATED WORKS

[1] deals with the assessment and design of two fresh roughly 4-2 multiplier compressors. The computation produces the imprecision results because the design relays on different features of compression. [2] deal with the Modified Square Root Carry Select-Adder (MCSLA). The disadvantage is that the design computations are very complex.

[3] The sophisticated complete adder multiplexer is created to obtain low power consumption. The models are created using Verilog HDL and a Quartus II simulator is used to verify the functionalities. The disadvantage is that, with the exception of power consumption, region, delay, transistor count is higher.

## III. EXACT COMPRESSOR

The main goal of carry saves adder or parallel multiplication is to reduce the n numbers of the compressor to two numbers of compressors. In computer arithmetic, n-2 compressor is widely used. A n-2 compressor in a circuit is a slice that lowers n compressors to two compressors, meaning the n-2 compressor gets n slightly from position I and also carries one or more compressors from place to position i-1 and i-2. The theorem of inequality is to be satisfied for the proper operation of the circuit.

$n + \Psi_1 + \Psi_2 + \Psi_3 + \ldots \leq 3 + 2\Psi_1 + 4\Psi_2 + 8\Psi_3 + \ldots\ldots(1)$

Where Ψj represents the number of carry bits.

The compressor 4-2 is a commonly used compression method structure. It can be introduced between neighboring slides with the carrying bit. Cin denotes the carry bit in the place to the right. The higher-position carry bit is Cout. The 4-2 compressor outputs are provided by the following equations [4].

$Sum = x_1 \wedge x_2 \wedge x_3 \wedge x_4 \wedge C_{in}$ (2)

$C_{out} = (x_1 \wedge x_2)x_3 \wedge (x_1 \wedge x_2)' x_1$ (3)

$Carry = (x_1 \wedge x_2 \wedge x_3 \wedge x_4)C_{in} + (x_1 \wedge x_2 \wedge x_3 \wedge x_4)' x_4$ (4)

Using two complete adders, the 4-2 compressor is usually introduced.

## IV.STRUCTURE OF WALLACE TREE

The Wallace tree has been defined with three steps:

1. Multiplying each bit of one of the arguments, yielding outcomes to n2 by each bit of the other argument.
2. Reduce the number of partial products to two with full and half adder layers.
3. The cables are grouped in two digits and added with a standard adder.

## V.DESIGN APPROACHES

Three designs are suggested in this part from an approximate compressor. The precise complete adder cells can be replaced by an estimated complete adder cells [5]to design a 4-2 compressor. However, because it generates inaccurate outcomes and high error rate, it is not effective. Therefore, to decrease the mistake, two distinct designs are suggested. The other two designs make the performance better.

Three designs of an approximate compressor are suggested in this chapter. The precise complete adder cells

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can be replaced by an approximate complete adder cell [6] to design an approximate 4-2 compressor. However, because it generates erroneous outcomes and elevated error rate, it is not skilled. Therefore, to decrease the mistake, two distinct designs are suggested. The other two designs make the improvement better.

*A.Design 1:*

Compressor utilizes two adders in their entirety. There is a distinction between precise and approximate compressor outputs in this model. Due to the incorrect results, inefficiency output, the optimized design is used.

In design 1, the compressor is designed by using two full Adders. The output carry is changed to cin by changing the

Carry'= Cin(5)

Sum' = Cin' ((x1^x2)'+(x3^x4)')(6)

The Figure.2.Represents 4-2 compressor application with two complete adders. There is a distinction between precise and estimated compressor outputs in this model. The optimized design is used because of the wrong outcomes of inefficiency production.

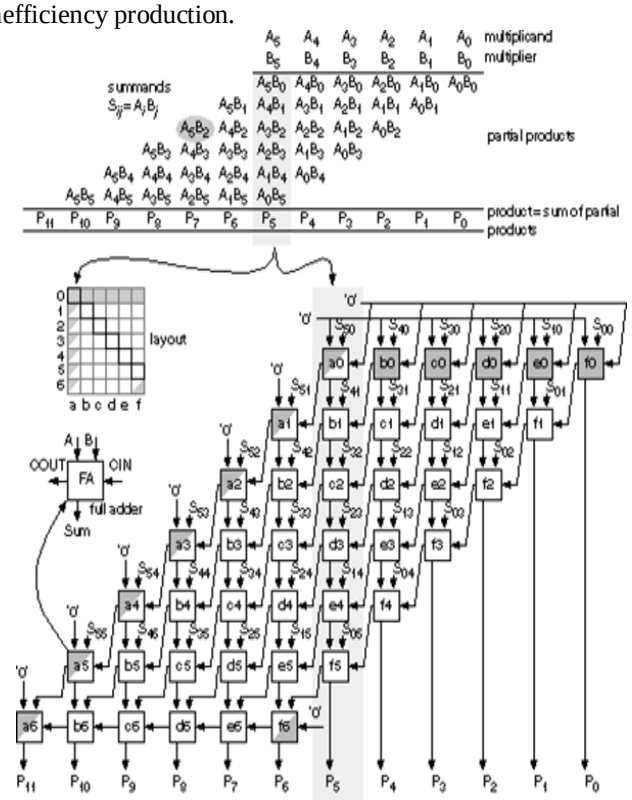


**Fig 1 Structure of Wallace Tree Multiplier**

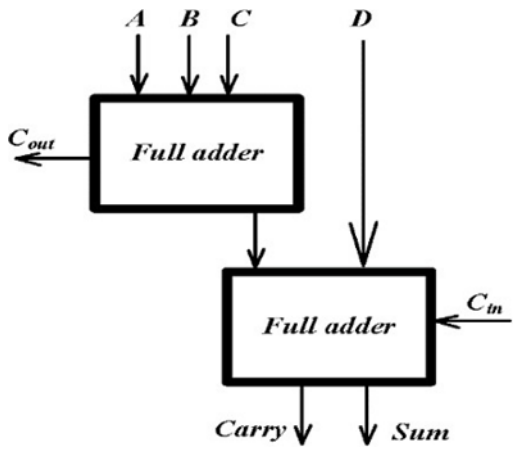


**Fig.2. Implementation of 4-2 compressor**

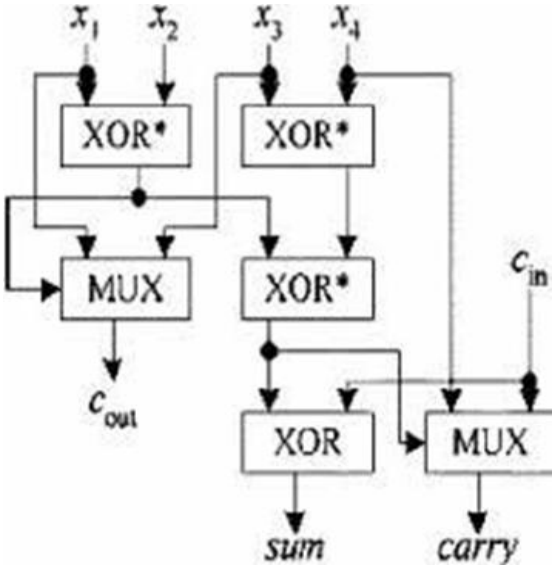


**Fig.3.Optimized 4-2 compressor**

*B. Design 2*

In Design 2, the XOR and XNOR doors are used to design the 4-2 compressor. The compressor is intended using doors to achieve the right outcomes, Efficiency output. In some countries, the output value cout may reducethe distance of the error and simplify the complicated design[8 ].

Cout = $((x_1x_2)'+(x_3x_4)')(7)$

The Figure.3.Represents the design of an exclusive OR and multiplexer 4-2 compressor. The area, the compressor's power consumption is significantly reduced compared to the compressor intended using two complete adders [7]. The compressor which is designed by using XOR and XNOR gates has more number of critical paths. So, this design also produces the incorrect output, but it is efficiency than the compressor design by using two full adders.

*B.Design 3*

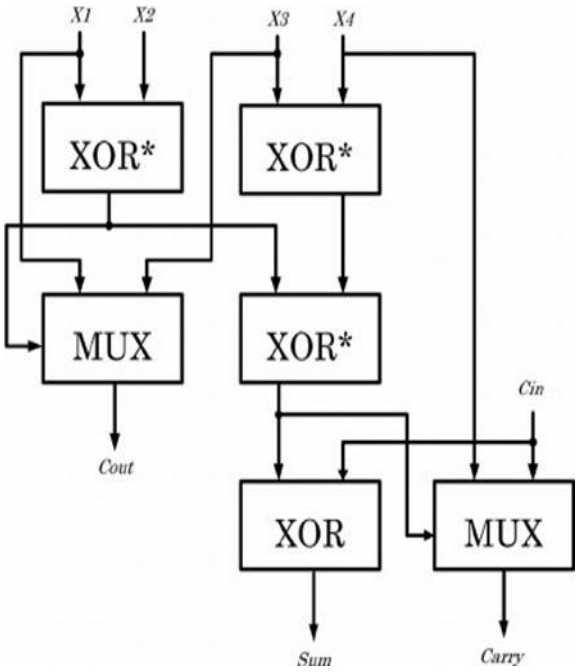


**Fig.4.Further optimized 4-2 compressor**

The design 2 is further optimized to obtain the best performance results and to reduce the number of gates and critical paths.

To decrease the error rate, this design is suggested. Compared to model 2, the carry and cout yield have the same weight.The interchanged output of the design is given by the following equations.

Sum'= $(x_1 \wedge x_2)' + (x_3 \wedge x_4)$ (8)

Carry'=$((x_1 x_2)' + (x_3 x_4)')'$ (9)

The Figure.4.shows the design of 4-2 compressor with less number of critical paths and delays. The vital path delay and the total number of gates are lower than the previous design. The further optimized design is easily implemented by using the gate level implementation.

The error rate is decreased to 2% from this layout. The scheduled design's ambiguity is lower than the other approaches to design.

## VI.MULTIPLICATION

The impact of multiplication using the compressors is examined [9]. The multiplier actually consists of three components, the first part being Partial Product Generation, the second part being Carry Save Adder (CSA) and the third part being Carry Propagation Adder (CPA).

The Carry Save Adder (CSA) is used to decrease the matrix of partial products to just two operands. In terms of delay, energy usage, region and circuit complexity, this plays an important role. Compressors ' primary use is to boost CSA velocity and decrease energy dissipation in order to obtain quick and low energy operation. In the first part :all partial products are generated using the AND gate. For the second part, is used to reduce the partial products with carry save adder.

In the first stage of partial products, two half adders, two full adders and eight compressors are used for the reduction processes. Half adder, one complete adder and ten compressors are used for the reduction phase in the final phase of partial products. Approximate compressor usage reduces power consumption, transistor number.

## VII.RESULTS

The design of the approximate compressors is designed and simulated using Xilinx software. The design is synthesized using 18nm Cadence software and the performance metrics are measured.

### *A. Transistor Count*

The amount of transistors used in the circuit must be decreased in order to decrease the complexity of the circuit. By comparing the results from table1, table 2 and table 3 the number of the transistor used is reduced in design 3 as 110. The reduction in the transistor count will reduce the complexity.

**Table.1.Results for design 1 using conventional method**

| WALLACE TREE MULTIPLIER | DADDA MULTIPLIER |
|---|---|
| Area - 4786 $m^2$ | Area - 4218 $m^2$ |
| Cells - 143 | Cells - 138 |
| Leakage Power - 336.70nW | Leakage Power - 336.10nW |
| Dynamic Power - 745621.12nW | Dynamic Power - 456281.85nW |
| Total Power - 745957.82nW | Total Power - 456617.95nW |
| Delay - 27.33ns | Delay - 24.2ns |

### *B.Power*

The power consumption of the multiplier is decreased based on the amount and type of compressors used. The low power consumption [10] is available when comparing the power consumption between design 1, design 2, and design 3 from the entire three table design 3.

| WALLACE TREE MULTIPLIER | DADDA MULTIPLIER |
|---|---|
| Area - 4574 $m^2$ | Area - 3258 $m^2$ |
| Cells - 123 | Cells - 112 |
| Leakage Power - 237.17nW | Leakage Power - 218.20nW |
| Dynamic Power - 645284.5nW | Dynamic Power - 427891.32nW |
| Total Power - 645521.67nW | Total Power - 428109.52nW |
| Delay - 24.56ns | Delay - 18.15ns |

**Table.2.Results for design 2 using optimized**

### *C.Delay*

The delay of the multiplier circuit depends on the amount of partial decrease decrease and each stage's delay. Each stage's delay in partial decrease is equivalent to each stage's delay. Reducing the multiplier delay will decrease the complex and boost the multiplier's effectiveness. Design 3 is less time-consuming compared to design 1 and design 2.

**Table.3.Results for design 3 using further optimized method**

| WALLACE TREE MULTIPLIER | DADDA MULTIPLIER |
|---|---|
| Area – 3310 $m^2$ | Area - 2022 $m^2$ |
| Cells - 118 | Cells - 110 |
| Leakage Power - 210.32nW | Leakage Power - 210 nW |
| Dynamic Power - 427459.18nW | Dynamic Power - 356419.02nW |
| Total Power - 427669.5nW | Total Power - 356629.02nW |
| Delay - 19.6ns | Delay - 13.15 ns |

Thus the Dadda multiplier design 3 has improved performance in area, delay and transistor count which is taken in the 18 nm cadence instrument compared to the Wallace tree multiplier design 3. Due to its dot product multiplication, the Dadda multiplier has better performance than the Wallace tree multiplier.

## VIII. CONCLUSION

The Dadda multiplier therefore delivers the greatest energy, region, delay and amount of transistor used output. Compared to the Wallace tree multiplier, energy consumption and all performance metrics are reduced to a higher extent. This multiplier can be implemented in Image Processing to give a better multiplication. The faster multiplication is successfully achieved by cascading of the two design techniques of the compressor together.

## IX. ACKNOWLEDGMENT

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