A New Converter Topology Designed for Cascaded H Bridge Fifteen Level Inverter

S. Seetharamudu, B. Pakkiraiah

Abstract*: Multilevel inverter (MLI) are used in most of the high-power industrial application and it has many benefits, such as lower harmonic spectrum and low-order switching losses, which will reduce the device's size. A new CHB MLI topology with a tiny number of switches is suggested for this paper. In terms of reduced THD value and worth, this topology is superior to the multilevel converters. With the application of the SPWM method, a 15-level inverter will be simulated and its impact on the harmonic spectrum will be analysed. In MATLAB/SIMULINK software, validation of the suggested topology simulation results were observed.

***Keywords* : Multilevel Inverters, THD, Sinusoidal PWM.**

I. INTRODUCTION

In 1975 Multilevel inverter technology was introduced[1]. The MLIs are most used in high industrial applications. The main benefits of these converters are having low level harmonic value, less switching losses. The multilevel converter output is nearly equivalent to the sinusoidal voltage output waveform[2]. The multilevel converters are basically three kinds one is Diode clamped or Neutral point, flying capacitor and CHB.

According to structure and functionality of the multilevel converter, they have been attention of the present engineers and researchers[3]. On the other side these converters to improve the technology and possibility of industrialization have to increasing use in industry. A number of new multilevel converter topologies have been suggested for MLI. It comprised numerous power electronics driver circuits, switches, Dc voltages and sometimes passive components such as condensers in all suggested topologies[4,5]. The primary intensity of various converter topologies is to decrease the amount of switches in power electronics and thus decrease the complexity of the circuit. In some topologies, symmetric and asymmetric dc voltage sources are also suggested to obtain maximum output concentration using the same amount of electronic appliances[8,9].

Therefore, a new topology for (CHB) based 15-level voltage source inverter is proposed. As with the precise preparation of DC voltage sources and power semiconductor switches, the proposed inverter topology can offer a high number of output levels with smallest necessities to the circuit devices. These proposed topology is consists of seven IGBT switches the pulse given to the switches is based on the Sinusoidal Pulse Width Modulation technique[10,11]. From the proposed inverter circuit it is possible to generate 15 level output voltage with reduced complexities and THD values when compared with conventional CHB 15-level inverter. In addition, the simulation results demonstrate the feasibility of the suggested inverter topology being executed.

II. PROPOSED FIFTEEN LEVEL CHB CONVERTER

One of the fundamental and well known topologies among all multilevel inverters is the CHB inverter. The basic circuit of a 15-level cascaded MLI is shown in fig.1. It include seven switches namely H1,H2,H3,H4,S5,S6&S7 and three asymmetrical dc sources V1,V2 and V3. The proposed multilevel topology is consists of standard H bridge and three auxiliary switches. In auxiliary switching part comprising of a set of succession connected smaller MLI blocks. The multilevel inverter output is divided into dual components in this focused switching topology. One portion is called the level generation part and it is responsible for the favourable polarity level generation. The other portion is called the part of the generation of polarity. The H bridge involves of 4 switches H1,H2,H3 and H4 and is liable for creating polarity of voltage output with the working fundamental. The S5,S6 and S7 are the level selected switches and by selecting the less transition time of switches, there is a decrease in switching loss. The quantity of switches involved in the suggested scheme for the fifteen-level inverter is seven (including H bridge), as the standard incase is 28. Converter topology reduced by using switch count and gate circuits, thus reducing the complication of the general circuit in this series will decrease the installation region and price of the entire setup.

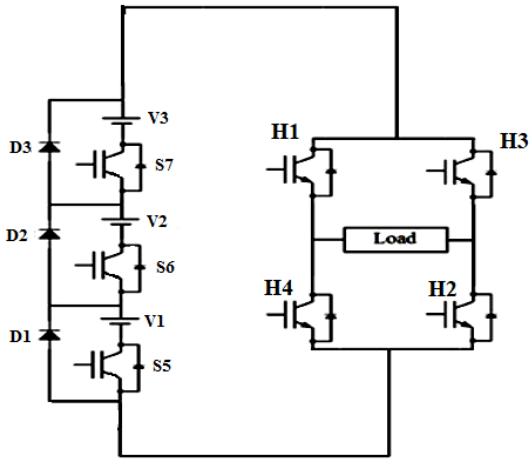

Fig.1. Circuit diagram for proposed Fifteen level inverter

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2.1 Switching sequence operation

Table 1. Switching Sequence of Pulses

S.No.	Switching State							Output voltage levels
	H1	H2	H3	H4	S5	S6	S7	
1	1	1	0	0	0	0	0	0
2	1	1	0	0	1	0	0	V1
3	1	1	0	0	0	1	0	V2
4	1	1	0	0	1	1	0	V1+V2
5	1	1	0	0	0	0	1	V3
6	1	1	0	0	1	0	1	V1+V3
7	1	1	0	0	0	1	1	V2+V3
8	1	1	0	0	1	1	1	V1+V2+V3
9	1	1	0	0	0	1	1	V2+V3
10	1	1	0	0	1	0	1	V1+V3
11	1	1	0	0	0	0	1	V3
12	1	1	0	0	1	1	0	V1+V2
13	1	1	0	0	0	1	0	V2
14	1	1	0	0	1	0	0	V1
15	1	1	0	0	0	0	0	0

Table 1 demonstrates the switches switching procedure to generate separate output voltage concentration Now shape the table 1, only favorable pulses are produced by the fundamental module and it is not responsible for generating adverse pulses. Therefore, guiding the adverse voltage is not important. The sequence, state and output voltage levels generated by the suggested multilevel inverter are displayed in table

2.2. Asymmetric DC Voltage Sources

For the symmetric configuration all sources have equal value V1=V2=V3 =Vdc then the number level equation is given by

$$N_L = 6n+1 \qquad (1)$$

Write to the asymmetrical configuration module where the sources are given as follows

V_1 = Vdc, V_2=2Vdc and V_3 = 4Vdc, then the number level equation is given by

$$N_L = 14n+1 \qquad (2)$$

Now from equation (1) and (2) we can understand the that for identical components quantity used in asymmetric formation of multilevel inverter.

III. PWM TECHNIQUE FOR PROPOSED SYSTEMS

SPWM modulation is one of the most prevalent methods used in a broad range of industrial applications where converters are used for energy switching. The ratio of low carrier(fc) to the modulation frequency (fm) for high-power implementation is the finest type of modulation. The number carriers are required for multilevel inverter is based on 'm-1', where 'm' is level of the inverter. Interaction of carrier wave and refence wave is used to generate a pulse for switches S5,S6 and S7. The fig.2 shows the carrier and reference signals.

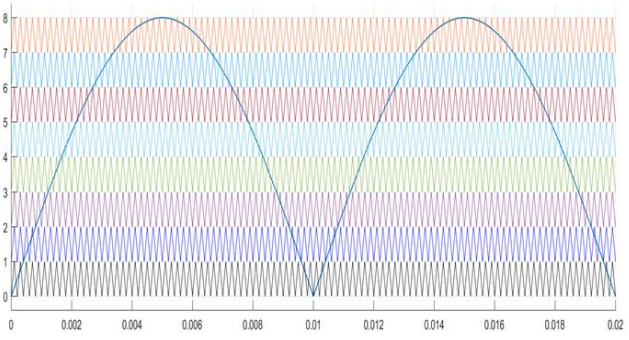

Fig.2 carrier and reference signals

In this proposed fifteen level configuration, eight carrier signals (C1 – C8) are considered and it divides the whole voltage in to seven regions. Suitable value of carrier frequency will be decreases the lower order harmonics. The carrier frequency is equal to 10Khz and reference frequency is same as the fundamental frequency of the system, the fig.3 shows the all eight PWM signals generation and selecting suitable combination of above signals generate a required pulse for our switches S5,S6 and S7.

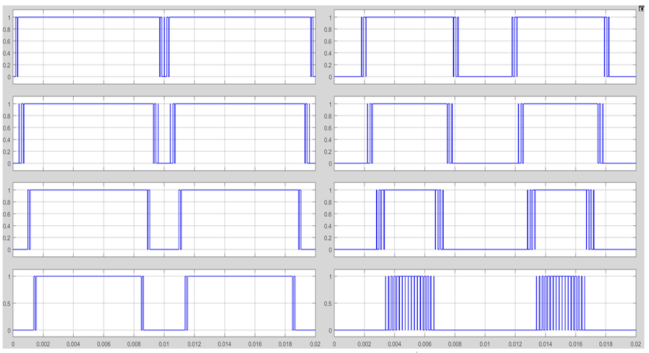

Fig.3. Pulses generation using SPWM

IV. SIMULATION RESULTS

The proposed module was simulated in MATLAB/SIMULINK to validate the result. The standards values of three asymmetrical DC sources V1, V2 & V3 are 50V,100V & 200V have consider for simulation. The fig.4 shows the complete simulation topology of proposed 15 level CHB multilevel inverter.

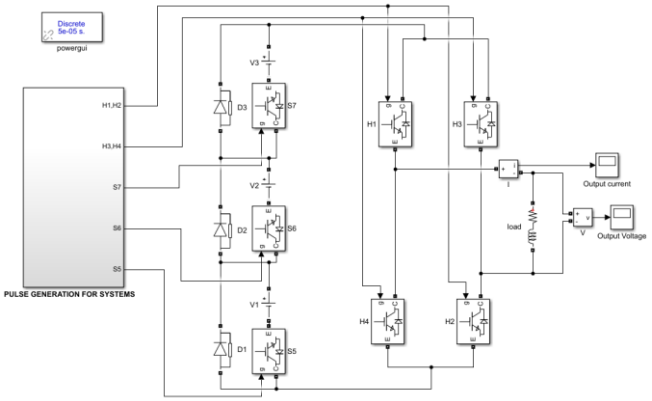

Fig.4 Simulation diagram of proposed 15 level CHB Multilevel Inverter

The pulse generating systems plays an significant role in the entire operation of the inverter as duty ratio of the pulses produced in the pulse generator unit turns on the switches in the suggested model resulting in the growth of stepped voltage across the load. The Pulses are generated by using sinusoidal PWM method and obtained pulses are nearest switching operating time and these pulses are given to all IGBTS used in the module as exposed in fig.5.

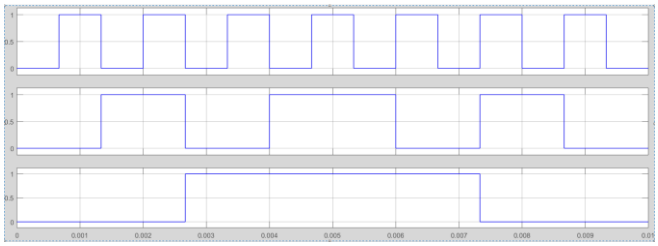

Fig.5 Switching pulses for switches

The simulated harmonic spectrum & voltage output was evaluated using the FFT tool in powergui block. The pulses required to trigger the seven switches in order to obtain the required 15-level output voltage is shown in fig.6.

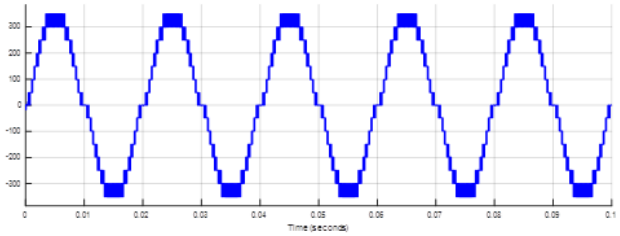

Fig.6 Output voltage with RL load

The harmonic spectrum values for different carrier frequency as shown in table 2.

Table 2. Comparison of THD value for various carrier frequency

S.No.	Carrier frequency Fc	%THD value	Fundamental Value(50Hz)
1	5000	9.19	334.8V
2	7500	8.84	334.3V
3	10000	7.70	334.1V

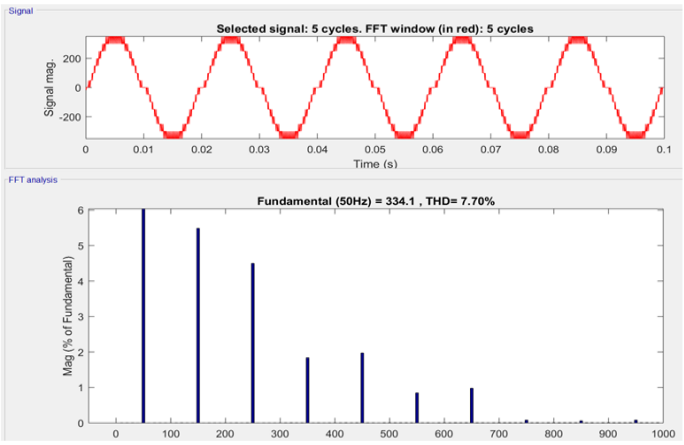

Fig.7 FFT analysis of Output voltage with RL load

Now from fig.6 the output voltage is increased step by step accordingly S5, S6 and S7 switches conduction. The total simulation time is considered as 0.01 sec or positive half cycle with fundamental frequency. Every half cycle the switches(H1,H2,H3 and H4) of H bridge is changed according to fundamental. The conduction sequence of switches are S5, S6, (S5,S6), S7, (S7,S5), (S6,S7), (S5,S6,S7) and similarly decreasing side and the voltage level is obtained +50V, +100V, +150V, +200V, +250V, +300V and +350V respectively. The output voltage wave form 15 level multilevel inverter across the load is nearly sinusoidal and the peak value of output is 350V. The total harmonics distortion (THD) spectrum was analyzed in FFT window and it is obtained 7.70% of Fundamental (50Hz) 334.1V.

V. CONCLUSION

The multilevel inverter topology of the single phase cascaded inverter has been granted to develop outstanding voltage output level with fewer switches and sources of dc voltages. It is observed that the suggested MLI is having less quantity of switches and voltages sources and there is also complete decrease in the complications and size of the circuit, resulting in decrease in switching losses and also an automatic decrease in THD. The simulation results is displayed here for different values of DC source voltages V1=50V, V2 = 100V and V3 = 200V and the peak voltage of fifteen level inverter is 350 V.

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