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Reversible Vedic Multiplier

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Abstract*: *In the new era of technology speed effective advanced multiplier has greatest demand, where they acts as an essential part in almost all high speed processing units which are used currently. As the multiplier is one of the essential components in several computing machines, for instant microprocessors, DSPs (Digital Signal Processors) and quantum computational and combinational systems. The performances of different processors is measured based on number of multiplication completed per second. So efficient multiplier designs are to be found to meet these performance constraints and one such approach which provides solution to above problem is Vedic multiplier. It is simple in structure and increase the efficiency by reducing the unnecessary steps in multiplication. Furthermore, implementing the designed multiplier using reversible gates can decreases the dissipation of power also, which is another essential design constraint that to be met in an embedded system. In the present work, a 4X4 reversible Vedic multiplier is designed; moreover it can offers more efficiency in terms of reversible design parameters such as TRLIC (Total Reversible Logic Implementation Cost) and delay. Code for 4X4 Vedic multiplication operation is written using Verilog HDL programming language and simulation is done using Xilinx 14.7 ISE is targeted to selected FPGA device family as Vertex 6.

Index Terms*: *Modified 2X2 Vedic multiplier, Reversible gates, Ripple Carry Adder, Vedic Multiplier.

I. INTRODUCTION

The word Vedic was discovered from the Sanskrit word Veda means knowledge. Actually Vedic Maths was an ancient Mathematics system and Sri Bharti Krishna Tirthaji was rediscover them, between 1911 and 1918 (1884-1960) [1]. He did a significant research in Atharva Veda and developed 16 formulas and 16 sub formulas. Among Urdhva Tiryakbhayam (UT) is the most efficient one which is a multiplication formula that can reduce steps in multiplication. This formula is suitable for all kinds of multiplications for instant, Binary, Decimal and Hexadecimal etc. The major concept behind this sutra is, that it can generate the partial products easily then after they are summed up in parallel manner, as a result the computational time will be reduced. Due to simple in approach this sutra can be applicable for various mathematics branches for instance, calculus, complex numbers and algebra etc [2].

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As the multiplier is acts as key element in several computing system, major arithmetic multiplication and is frequently used in MAC and DSP etc.

Especially in DSP units it is used to perform DFT, FFT in such cases the multipliers are essential [3].Reversible logic is a prominent research area from the past few decades, whose range is extended to Low power VLSI, Optical computing system, quantum dot and DNA computing [6].

The organization of the paper will begin with an introduction to reversible logic and some examples in section II,section III provides the Urdhva Tiryakbhayam multiplication algorithm, followed by explanation of proposed 2X2 and 4X4 multiplier designs in Section IV and the simulation of proposed designs and comparison with existing designs is done succeeding sections.

II. OVERVIEW OF REVERSIBLE LOGIC

In 1960, R.Landauer demonstrates that energy dissipation in circuits is due to loss of information which are designed using irreversible hardware [4]. As stated by him, for every information bit that is loosed will dissipate kT.ln2 joules of energy, in which K denotes the Boltzmann's constant whose value is $1.38X10^{-23}$J/K and T is Absolute temperature in °Kelvin and its value is 273.16°K. Reversible design is one which does not loss information loss and it automatically takes care of the produced heat caused by information loss. In 1973, Bennett, proved that a circuit or a system will dissipate no energy if it a reversible circuit. Hence reversibility is key design property in circuits to reduce power dissipation [5].

A. Reversible Gate

A reversible gate has same number of inputs and outputs and there exists one-to one correlation them which indicated that inputs can always be retrieved from its outputs. Fig. 1 gives the general representation of a reversible.

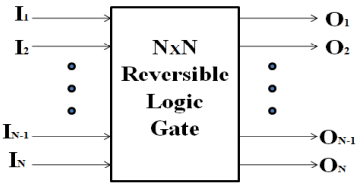

Fig. 1. General representation of NxN reversible logic gate

B. Important Parameter of Reversible Gate

The parameters in optimization of a reversible logic circuit are listed below [7]:

Gate Count (GC): It gives total reversible logic gates used in a circuit.

Ancilla Inputs/Constant Inputs (CI): It indicated how many inputs are kept constant either 0 or 1 for synthesis of a design.

Garbage Outputs (GO): It indicates number of outputs which are not used in the synthesis, but needed to maintain reversibility of a gate.

Quantum Cost (QC): It gives number of primitive gates (1x1 or 2x2) required to implementing a function which is reversible.

Total Reversible Logic Implementation Cost (TRLIC) [7]: It is nothing but the sum of gate count, garbage output, quantum cost of each gate and constant inputs that are maintain to implement the function and it is as follows

$$TRLIC = \Sigma (NG, QC, CI, GO) \quad (1)$$

Design Constraints:

The major design limitations of reversible circuits are as follows:

- It does not permit Fan-out.
- No Feedback will be accepted.
- Minimum number of CI and GC.
- Minimum delay and should offer low Quantum Cost.

III. EXMPLES OF REVERSIBLE GATES

A. CNOT Gate

CNOT gate consists of 2 inputs and 2 outputs which performs the control NOT operation [9], that is if the first input is equal to logic 1 then the second output will be the NOT of B, which is used widely used for fan-out purposes and it's QC of 1and its logic diagram is shown in Fig.2.

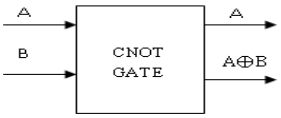

Fig. 2. CNOT Gate

B. Peres gate[9][10]

It consists of 3 inputs and 3 outputs which is designed using a Toffoli and a Controlled Not Gate which acts as a half adder when C equal 0 and it has quantum cost of 4 and it's logic diagram is given in Fig.3.

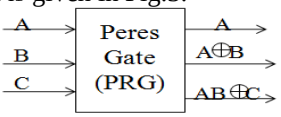

Fig. 3. Peres Gate

C. BVPPG Gate [9]

It is a 5x5 reversible gate which is widely used in multiplication to produce two partial products at the same time. In addition its QC is 10 and logic diagram is in Fig. 4

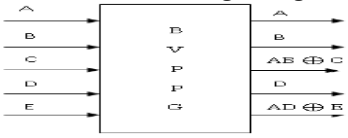

Fig. 4. BVPPG gate

D. BME gate [9]

It has 4 inputs and 4 outputs whose quantum cost QC of 5 and logic diagram is inFig. 5.

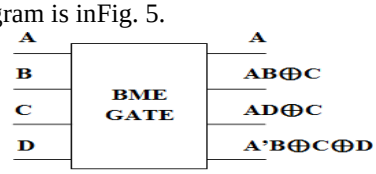

Fig. 5. BME Gate

E. PPG Gate [9]

Partial Product Generation gate is 4x4 reversible gate which is used to generate the 2 partial productions at the same time and has QC of 7 which is less when compare to BVPPG gate and its logic diagram in given in Fig. 6.

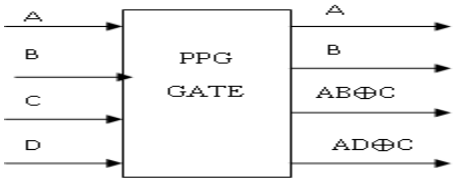

Fig. 6. PPG gate

F. HNG gate [12]

It consists of 4 inputs and 4 outputs which is shown in Fig. 7 and it is used as full adder when its input D=0, moreover it has QC 6.

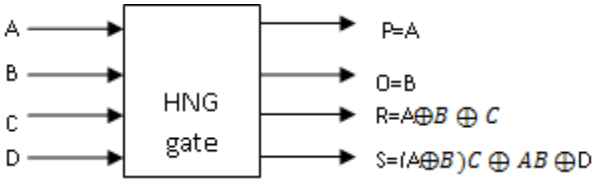

Fig. 7. HNG gate

G. RMUX1 Gate [12]

It is a 3input and 3 output gate which is given in Fig. 8, and its QC is 4.

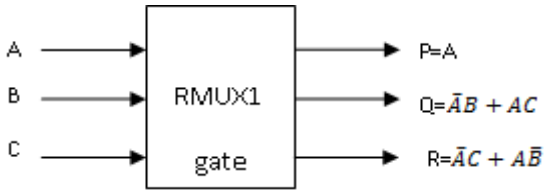

Fig. 8. RMUX1 gate

IV. ALGORITHM FOR MULTIPLICATION USING URDHVA TIRYAGBHYAM SUTRA

Mathematics became easy if the 16 formulae from Vedic are used. Among 16 sutras Urdhva Tiryagbhayam and Nikhilam are suitable for multiplication. Though the Nikhilam sutra is simple to implement but it is limited to the numbers which are nearer to base 10,100, 1000 and in powers of 10. In contrary, Urdhva Tiryagbhayam is the best method for multiplication of any numbers and Vertically and Crosswise is the principle behind this method. Let assume A and B are the binary numbers to be multiplied where A is multiplicand and B is multiplier and produce 4 bit output (q_3q_2 q_1q_0). General procedure for 2x2 multiplication using Urdhva Tiryagbhyam is in Fig. 9[10].

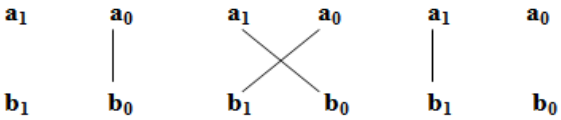

Fig. 9. Line diagram for 2X2 Vedic Multiplication

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V. PROPOSED REVERSIBLE VEDIC MULTIPLIER

A. Reversible 2x2 Vedic Multiplier

Gowthami.P and R.V.S.Satyanarayana designed a reversible 2X2 multiplier with the help of Urdhva Tiryakbhayam [8], in addition 5 reversible logic gates are required in the design namely, two of them are BME gates, one is a BVF gate and rest are Peres and CNOT gate. It has the QC of 17. It has 5 constant inputs and 5 garbage outputs. This design also allows Fan-out and offers TRLIC of 32.

In this the prposed paper, a 2x2 reversible Vedic multiplier is used which is better in terms of TRLIC and also eliminate Fan-out problem [10] and logic diagram of modified 2x2 multiplier is shown n Fig. 10.

A 2x2 Vedic multiplier can be designed using following equations which are further implemented using reversible logic gates [7].

$$q_0 = a_0 b_0 \qquad (2).$$

$$q_1 = (a_1 b_0) \oplus (a_0 b_1) \qquad (3).$$

$$q_2 = (a_0 a_1 b_0 b_1) \oplus (a_1 b_1) \qquad (4).$$

$$q_3 = (a_0 a_1 b_0 b_1) \qquad (5).$$

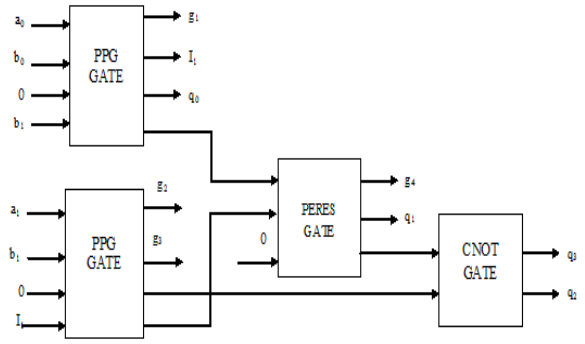

Fig. 10. Modified 2x2 vedic multiplier

Modified 2x2 Vedic multiplier uses four reversible gates, among them two are PPG gates (Partial Product Generator gates) (which are intended to generate the partial products and to avoid Fan out problem), one PERES gate (which acts as a half adder) and one CNOT gate (used for copying the outputs and performs EXOR operation). It has 3 constant inputs and produces 4 GO and it has a QC of 19 and it offers TRLIC of 30 which is better while compare to existing design [8].

B. Reversible 4x4 Vedic Multiplier

In this paper, the architecture of the irreversible Urdhav Tiryakbhayam multiplier [8] is changed by replacing the conventional logic modules with the corresponding reversible modules. The existing reversible 4X4 Urdhav Tiryakbhayam (UT) multiplier [14] was designed using four reversible 2X2 (UT) multipliers, two four bit reversible ripple carry adders, two reversible half adders and one OR gate with a TRLIC of 230.In present work, the same 4X4 Urdhav Tiryakbhayam (UT) multiplier is modified to improve TRLIC and to achieve less delay.

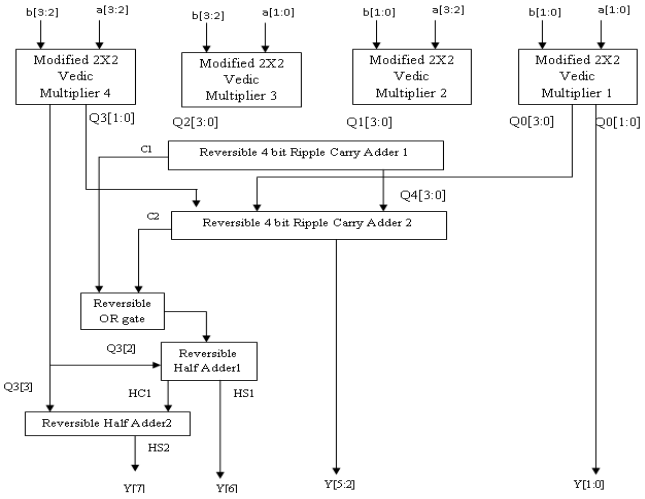

Fig. 11 Reversible 4X4 Vedic multiplier block diagram.

Fig.11 illustrates the Reversible Vedic 4X4 multiplier which has been designed based on modified 2x2 vedic multiplier. In this the output of 2x2 multiplier1 whose inputs are assigned as a [1:0] and b [1:0] forms the LSB bits of final result i.e Y[1:0]. The outputs from second and third 2x2 vedic multipliers are summed up by using the upper Reversible 4-bit Ripple Carry Adder whose sum outputs are q[3:0] and the carry is C1. The sum output of upper adder and remaing bits of first 2x2 vedic multiplier and two LSB bits of fourth 2x2 vedic multiplier are applied to the lower 4-bit reversible adder as inputs. Sum output of lower adder acts as the output bits Y[5:2]. The carry bits C1 and C2 from the adders are applied to the reversible OR gate and the remaing two bits of the output i.e Y[6] and Y [7] are obtained by using of two reversible half adder circuits which is nothng but a Peres gateand above designed Reversible 4X4 vedic multiplier has TRLIC of 215 which is better than existing design [14].

For implementing reversible ripple carry adder 3 HNG gates and 1 Peres gate are used which is given in Fig.12. When the D input is zero the HNG gate can acts as a full adder and if C=0 the Peres gate can acts as a half adder which is shown in Fig. 13 and an OR gate is required to added the carries from two 4-bit ripple carry adders which is implemented by using RMUX1 gate which acts as a OR gate when the inputs assigned as A=A, B=0 and C=B which is given in Fg.14. The designed Reversible 4-bit ripple adder has QC of 22, GC of 4,it has 7 garbage outputs and 4 constant inputs. So, its TRLIC is 37.

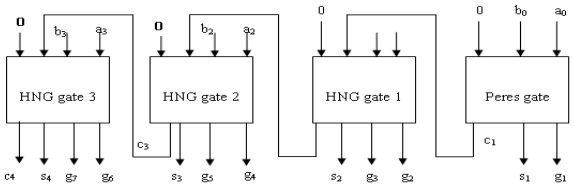

Fig. 12. Implementation of Reversible 4-bit Ripple Carry Adder

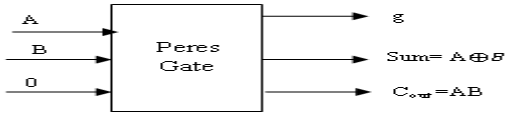

Fig. 13. Implementation of Half adder using PERES gate

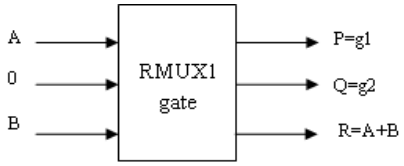

Fig. 14. Implementation of OR gate using RMUX1 gate

VI. RESULTS

Xilinx ISE 14.7 tool is used for functional verification of the designed 2X2 and 4X4 reversible and Verilog hardware description languageis used to write the code for proposed designs and the simulation is done by generating a Verilog test fixture on a target device of Vertex 6 low power FPGA. In order to synthesis the designs Xilinx Synthesis Tool (XST) is used.

A. Reversible 2x2 Vedic Multiplier

The RTL schematic and simulation waveform of modified 2x2 vedic multiplier are shown in Fig. 15 and 16 respectively.

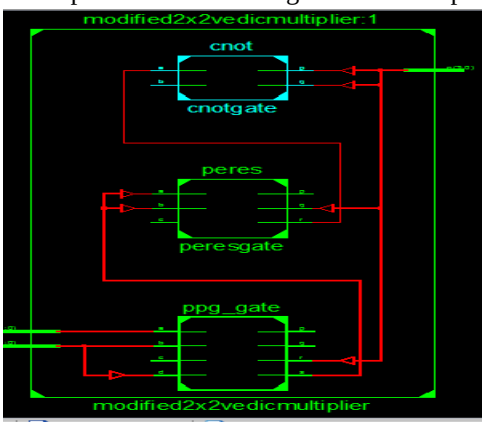

Fig. 15. RTL schematic of modified 2x2 Vedic multiplier

As shown in the above figure modified 2x2 Vedic multiplier uses PPG gate, CNOT and PERES reversible gates in implementation. For the 2X2 multiplier if both the inputs a [1:0] and b[1:0] are binary 11 then it produces a four bit output as q[3:0]=1001 which is shown in Fig. 16.

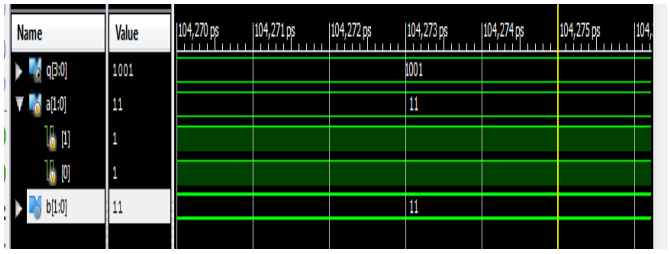

Fig. 16. Simulation waveform of modified 2x2 Vedic multiplier

B. Reversible 4-bit adder

A reversible 4-bit ripple adder 4-bit ripple carry adder is implemented using a half adder (i.e. Peres gate with input C=0) and tree full adders which are implemented using HNG gate and it RTL schematic as well as simulation waveform are given in Fig. 17 and 18 respectively.

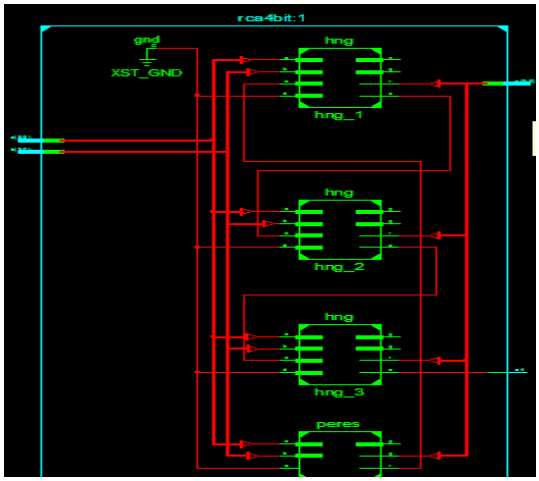

Fig. 17. RTL schematic of Reversible 4-bit ripple adder

For a parallel adder if both the inputs a [3:0] =1001 and b[3:0]=1011 then it produces a four bit output sum as s [3:0]=0100 and the final carry is C4=1 which is shown in Fig. 18.

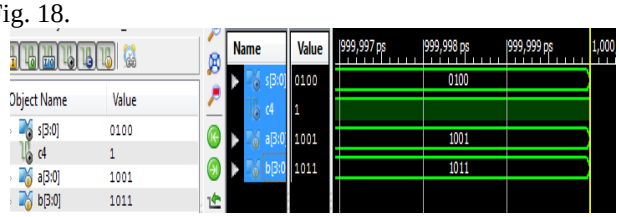

Fig.18. Simulation waveform of Reversible 4-bit ripple carry adder

C. 4x4 Reversible Multiplier

Reversible 4X4 multiplier is designed by using 2X2 multipliers and 4-bit adders and its RTL schematic as well as results are given in in Fig. 19 and 20 respectively.

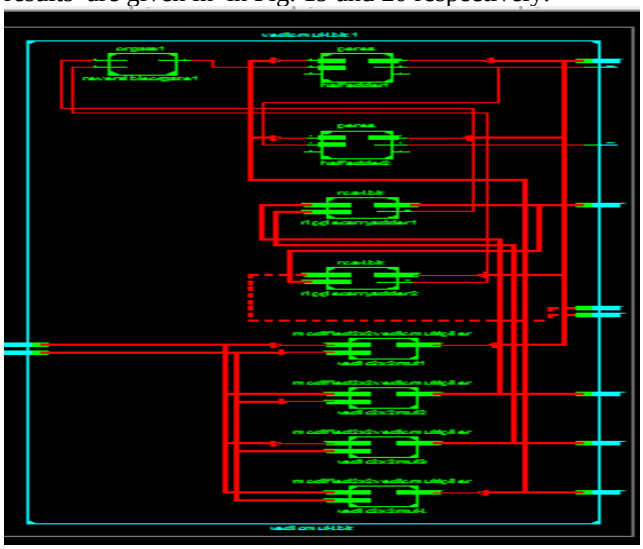

Fig. 19. RTL schematic of Reversible 4X4 Vedic multiplier

A 4x4 multiplier uses four 2x2 multiplers each of TRLIC of 120 and two 4-bit ripple carry adders each has TRLIC of 74 and two half adders each has TRLIC of 7 and one OR gate which offers TRLIC of 7. So, the total TRLIC of the design is 217 only.

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For a 4X4 reversible multiplier if inputs are a[3:0]=0111 and b[3:0]=0111 then it produces an eight bit output Y[7:0]=00110001and if are, a[3:0]=1000 and b[3:0]=1101 then it produces an eight bit output Y[7:0]=01101000 which are shown in Fig. 20.

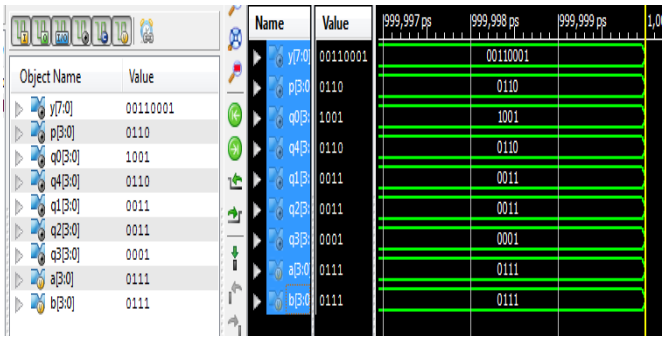

Fig.20. Simulation results of Reversible 4x4 Vedic multiplier

The existing and proposed 4X4 Vedic multipliers are compared in terms of design parameters and are given in Table I whereas, Table II gives the delay of different multipliers.

Table I. Comparison between Reversible 4X4 Multipliers

4x4 Multiplier	Comparison Parameter				
	Quantum cost	*Gate count*	*Garbage outputs*	*Constant inputs*	*TRLIC*
Proposed design	132	27	33	23	215
Design[9]	162	37	62	29	290
Design[10]	150	31	38	31	250
Design[13]	156	31	40	31	258
Design[14]	128	31	40	31	230

Table II. Delay Comparison for Designed 4X4 Reversible Vedic Multipliers

4x4 Multiplier	Delay(ns)
Proposed design	3.991
Conventional Multiplier	9.228
Design[9]	9.566
Design[15]	8.558
Design[16]	7.858

From Table I and II, it is evident that the proposed design has better performance and offers less delay while comparing to the existing designs.

VII. CONCLUSION

In this work a high speed, power efficient 4X4 Vedic multiplier using reversible gates with Vedic sutra was designed. The procedure is carried out until an optimized design should be obtained as compared to the existing designs. The performance of a reversible logic system is measured in terms number of gates used, total quantum cost of the design, number of inputs that are kept constant and number of output that are unused. Lower the values mention above more the efficiency and all these parameters combined in a single term called TRLIC which is summation of all these parameters. Also lower TRLIC implies better performance. Besides, the proposed design also has lower delay and TRLIC is also reduced than the existed designs. Furthermore, more than four bit multiplication can also implement based on these ideas in near future.

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AUTHORS PROFILE

G.Venkata Latha obtained her B.Tech and M.Tech with specialization of Embedded Systems from JNTUK, Kakinada in the year 2012 and 2015 respectively. She published two papers in the area of VLSI and presented papers in three international conferences. Moreover Low Power VLSI and IoT are her areas of interest.

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