FPGA Based Optimized Reconfigurable Base-2 Constant Coefficient Multiplier Architecture for Image Filtering

N. Sambamurthy, M. Kamaraju

Abstract: ***Image convolution using FPGA has been comprehensively used for noise removal of Reconfigurable computing based image Processing Algorithm. Particularly these filters are widely used in embedded computer vision applications like edge detection and Feature extraction analysis. Practical implementation of filter requires enormous computational requirement. The multiplier plays very important role in the image convolution. The existed multiplier design requires more computational complexity for the 3x3 test image. For this the proposed reconfigurable constant coefficient multiplier uses base-2 Common sub expression algorithm. which reduces the computational complexity in a better way. The proposed 2D-convolution in image application is the value of resultant output is multiplication of image pixel with corresponding kernel value. In this work the realization of 2D convolution to be done using proposed constant coefficient multiplier and analyzed using Xilinx Virtex-5 FPGA platform***

Keywords: Field Programmable Gate array (FPGAs), Filters, 2D Filters, Gaussian Mask; BCSE;Mask, Image controller;

I. INTRODUCTION

In spatial Image convolution [1], the each output image pixel is computed by multiplying the values of each input image pixel with the corresponding kernel value. The convolution tap output gives the resultant pixel output. As shown in Fig.1.

Usually to compute the filtering operation for a given symmetric Gaussian kernel size of 3x3 and 3x3 image requires 9 multiplications and 8 summing elements are required.[10]-[11]. The digital convolution [2]-[3] process widely implemented in FPGA [4] for several decades. However these algorithms are computationally expensive.

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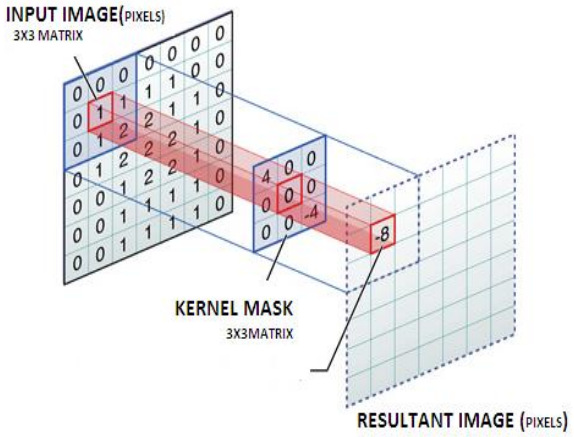

Fig.1.2 Dimensional - Image convolution

II. LITERATURE SURVEY

Nowadays, the image Convolution process is implemented on Graphical processing hardware (GPU) and DSP shows inadequate performance and high outlay. Moreover, ASIC's with rigidity and performance is the main drawback [4]-[8]. Generally, to perform a 2D-image convolution with FPGA, used 65,536 product terms and 65,535 adders are required for 256x256 gray scale image. First, the image size of 3×3 and a kernel mask size of 3×3 were chosen for performing the spatial convolution operation[5].

The Multiplier based convolution hardware [1],[2] is needed for noisy images and video processing. In linear spatial filtering, the multiplier is tobe optimized key component and defines the performance of the linear filter hardware [5],[6]. Therefore, reconfigurable fixed coefficient multiplier hardware architecture for spatial filter has been focused continuously [7].

C.Y.YAOet.al., implemented computational efficient multiple coefficient multiplication (MCM) algorithm for image filtering is designed [8].This MCM algorithm [8] mainly used graph algorithm and common sub-expression algorithm used. The image filtering does pixel by pixel multiplication using the MCM design uses more area and high complexity.

For portable devices The MCM design is not suitable. F. Boracchi introduced for optimal complexity design based multiplier for low power applications. But the multiplier design is generic

and not suitable for filtering [3]. A.G.Dimster suggested the Fixed binary common sub expression algorithm (FBCSE) is eliminate the computational complexity moderately by considering BCSE algorithm across the adjacent coefficients is designed [4],[9],[10].

The Fixed bit common sub expression algorithm [1],[9] Challenges the problem with redundant computational complexity.

The algorithms on a fixed coefficient design are not applicable for Image filter. Because the kernel coefficients are dynamically programmable on the requirement. So that the reconfigurable constant coefficient multiplier architecture is needed for designing the image filter [1].

In this paper the designed Base-2 common sub expression algorithm, reduces the complexity in Bsae-2 common sub expressions form. For designing the image filter with low complexity and power optimized scenarios the reconfigurable constant coefficient multiplier is needed.

Gaussian Mask with image convolution is important algorithm for image denoising of linera filter design. Gaussian filter (G) is defined for the following below equation.

$$G(x,y) = \frac{1}{2\pi\sigma^2} e^{-(x^2+y^2)/2\sigma^2} \quad (1)$$

Where G is the kernel mask, x, y are the image coordinates and σ is the Gaussian parameter. The deviation of σ is large, the image smoothing is higher.for this design σ=1.

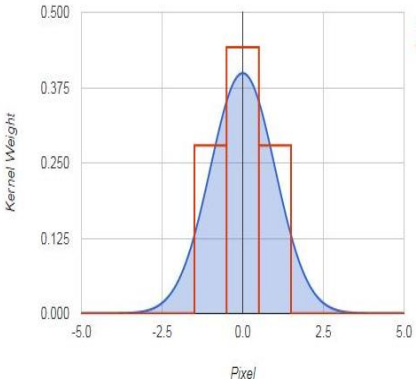

Fig.2. Image 2D-convolution using Gaussian mask with σ=1

Table-I: A 3×3 Test Image

P1	P2	P3
P4	P5	P6
P7	P8	P9

The image pixels are stored in 3x3 matrix is shown in table 1.

Each image pixel is read from the memory and scanned in a sequential order for the atapath performing filtering operation with designed kernel.

Table-II: Gaussian 3×3 Mask

0.077847	0.123317	0.077847
0.123317	0.195346	0.123317
0.077847	0.123317	0.077847

III. PROPOSED ALGORITHM AND HARDWARE DESIGN

Constant multiplication operation between the input image samples and the Gaussian kernel coefficients, for which the word length of the coefficients is 8-bit and it can be written as,

$$\left(\frac{xin}{2}\right).a7 + \left(\frac{xin}{4}\right).a6 + \left(\frac{xin}{8}\right).a5 + \left(\frac{xin}{16}\right).a4 + \left(\frac{xin}{32}\right).a3 + \left(\frac{xin}{64}\right).a2 + \left(\frac{xin}{128}\right).a1 + \left(\frac{xin}{256}\right).a0 \quad (2)$$

Table-III: Constant coefficients design

Coefficients	Binary weights							
a	$\frac{xin}{2}a7$	$\frac{xin}{4}a6$	$\frac{xin}{8}a5$	$\frac{xin}{16}a4$	$\frac{xin}{32}a3$	$\frac{xin}{64}a2$	$\frac{xin}{128}a1$	$\frac{xin}{256}a0$
b	$\frac{xin}{2}b7$	$\frac{xin}{4}b6$	$\frac{xin}{8}b5$	$\frac{xin}{16}b4$	$\frac{xin}{32}b3$	$\frac{xin}{64}b2$	$\frac{xin}{128}b1$	$\frac{xin}{256}b0$
c	$\frac{xin}{2}c7$	$\frac{xin}{4}c6$	$\frac{xin}{8}c5$	$\frac{xin}{16}c4$	$\frac{xin}{32}c3$	$\frac{xin}{64}c2$	$\frac{xin}{128}c1$	$\frac{xin}{256}c0$
d	$\frac{xin}{2}d7$	$\frac{xin}{4}b6$	$\frac{xin}{8}d5$	$\frac{xin}{16}d4$	$\frac{xin}{32}d3$	$\frac{xin}{64}d2$	$\frac{xin}{128}d1$	$\frac{xin}{256}d0$
e	$\frac{xin}{2}e7$	$\frac{xin}{4}b6$	$\frac{xin}{8}e5$	$\frac{xin}{16}e4$	$\frac{xin}{32}e3$	$\frac{xin}{64}e2$	$\frac{xin}{128}e1$	$\frac{xin}{256}e0$
f	$\frac{xin}{2}f7$	$\frac{xin}{4}b6$	$\frac{xin}{8}f5$	$\frac{xin}{16}f4$	$\frac{xin}{32}f3$	$\frac{xin}{64}f2$	$\frac{xin}{128}f1$	$\frac{xin}{256}f0$
g	$\frac{xin}{2}g7$	$\frac{xin}{4}b6$	$\frac{xin}{8}g5$	$\frac{xin}{16}g4$	$\frac{xin}{32}g3$	$\frac{xin}{64}g2$	$\frac{xin}{128}g1$	$\frac{xin}{256}g0$
h	$\frac{xin}{2}h7$	$\frac{xin}{4}b6$	$\frac{xin}{8}h5$	$\frac{xin}{16}h4$	$\frac{xin}{32}h3$	$\frac{xin}{64}h2$	$\frac{xin}{128}h1$	$\frac{xin}{256}h0$
i	$\frac{xin}{2}i7$	$\frac{xin}{4}b6$	$\frac{xin}{8}i5$	$\frac{xin}{16}i4$	$\frac{xin}{32}i3$	$\frac{xin}{64}i2$	$\frac{xin}{128}i1$	$\frac{xin}{256}i0$

2-bit Base-2 common sub expression algorithm (2BCSE): The designed 2-bit base-2 common subexpression algorithm generated partial products from each case given as

$$\frac{xin}{2}a7 + \frac{xin}{4}a6 + \frac{xin}{8}a5 + \frac{xin}{16}a4 + \frac{xin}{32}a3 + \frac{xin}{64}a2 + \frac{xin}{128}a1 + \frac{xin}{256}a0 \quad \text{-------(1)}$$

$X2$

$$a..x1 = y1$$

$$x2 + \frac{1}{4}\left\{\frac{x1}{2} + \frac{x1}{4}\right\} + \frac{1}{16}\left\{\frac{x1}{2} + \frac{x1}{4}\right\} + \frac{1}{64}\left\{\frac{x1}{2} + \frac{x1}{4}\right\}$$

$$x2 + \frac{x2}{4} + \frac{x2}{16} + \frac{x2}{64} \text{---------(2)}$$

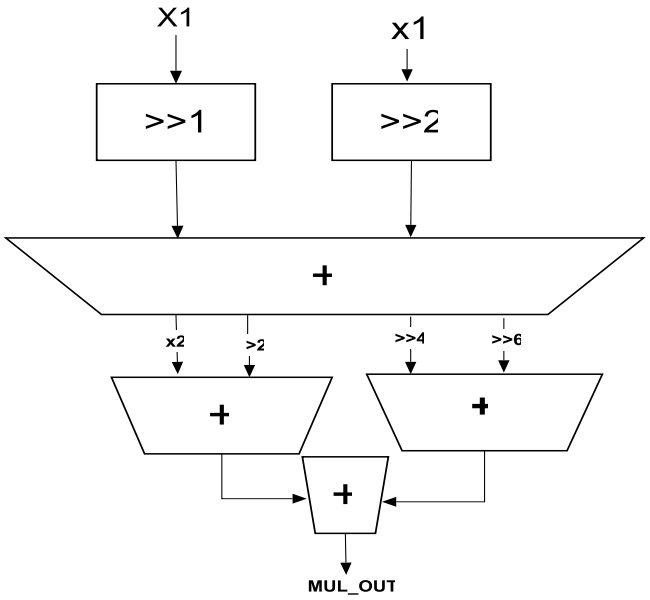

Fig.3: 2- bit Base-2common subexpression algorithm (2BCSE).

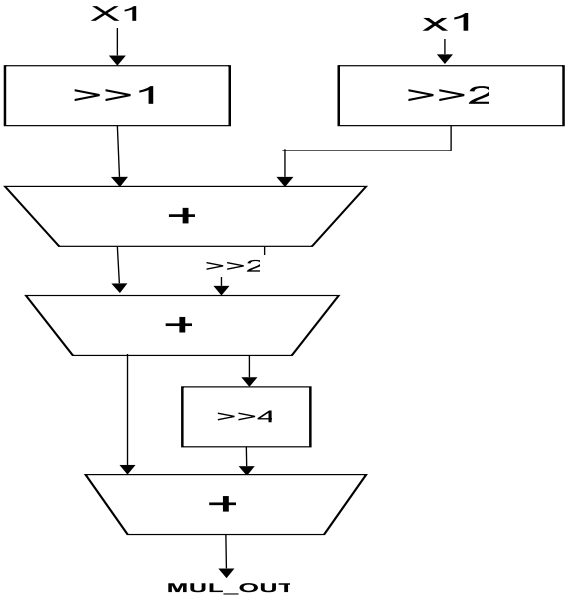

Fig.4: 3-bit Base-2 common sub expression algorithm (3BCSE).

3-bit Base-2 common sub expression algorithm (3BCSE):

The designed 3-bit base-2 common sub expression algorithm used partial products from each case is given as

$$\frac{xin}{2}a7+\frac{xin}{4}a6+\frac{xin}{8}a5+\frac{xin}{16}a4+\frac{xin}{32}a3+\frac{xin}{64}a2+\frac{xin}{128}a1+\frac{xin}{256}a0 \quad \text{---(3)}$$

$$\underbrace{\frac{xin}{2}a7+\frac{xin}{4}a6}_{X2}+\frac{xin}{8}a5+\frac{xin}{16}a4+\frac{xin}{32}a3+\frac{xin}{64}a2+\frac{xin}{128}a1+\frac{xin}{256}a0$$

$$a.x1=y$$

$$x2+\frac{1}{4}\left\{\frac{x1}{2}+\frac{x1}{4}\right\}+\frac{1}{16}\left\{\frac{x1}{2}+\frac{x1}{4}\right\}+\frac{1}{64}\left\{\frac{x1}{2}+\frac{x1}{4}\right\}$$

$$\underbrace{x2+\frac{x2}{4}}_{X3}+\frac{x2}{16}+\frac{x2}{64}$$

$$x3+\frac{1}{16}\left\{x2+\frac{x2}{4}\right\}$$

$$\underbrace{x3+\frac{x3}{16}}$$

The number of adders are reduced further by one. compaerd to 2-bit BCSEalgorithm. This Algorithm requires totally 15 Shift operations and 4 addition operations for performing 8-bit multiplication operation.

The input image is converted into .coe file. The Mat lab image tool used for generating .coe file. An image pixel controller is designed using Finite State Machine (FSM) based image controller to control the access of stored image binary values in the Block RAM.

In Block RAM the memory controller is controlling the flow of image pixels and kernel pixels using pixel and mask controller blocks.

IV. RESULTS AND DISCUSSION

Table- IV: Complexity analysis of Designed algorithm.

Used Element	Existed (FBCSE)	Proposed	
		3-bit BCSE	2-bit BCSE
Adders	4 (8-bit, 3 (9-bit) Total =9*7=63.	1(8-bit), 2 (9 –bit) Total =9*3=27	1 (8-bit), 2 (9bit),1(10-bit) Total =9*4=36
Multiplexers/AND Gates	8(8 input AND logic circuits) Total =9*8=72.	3 Mux's(2:1 Mux's) Total =9*3=27.	2 Mux's(4:1 and 2:1) Total =9*2=18.
Propagation Delay	8(19ns)+7(3.25ns) =166.75ns	3(3.25ns)+3(3.01ns) =18.04ns	4(3.25ns)+2(3.58ns) =20.16

The complexity analysis is performed with existed and designed 2-bit ,3-bit BCSE algorithms. The proposed algorithm used 27 addrers and 27 multiplexers for 3-bit BCSE and 36 addres and 18 multiplexers are for 2-bit BCSE .

Table -V: Comparison Results of the Designed Image filter on FPGA.

	Target Device	LUT'S	Flip flops	SLICES	Number of buffctrls
Proposed					
2-bit BCSE	Xilinx virtex-5	435	167	5	18
3-bit BCSE	Xc5VST-250	412	118	4	15
Existed					
FBCSE		758	112	6	23

The table[5] shows that designed algorithm used the less resources compared to the existed Fixed binary common subexpression (FBCSE).

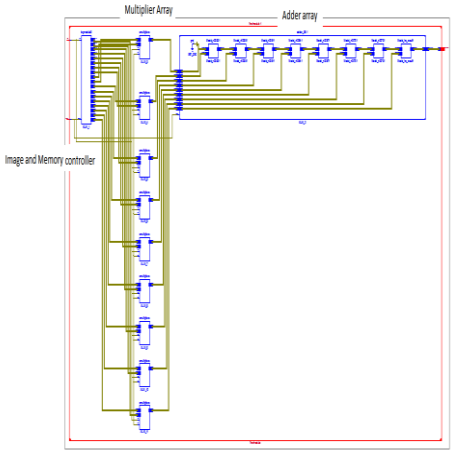

Fig.5: RTL schematic of designed Image filter.

The RTL schematic used 9 multipliers and 8 summing elements with image controller.

Table-VI: Comparative results of Power consumption.

Parameter	Proposed		Existed
Power (mw)	2-bit BCSE MULTIPLIER	3-BIT BCSE MULTIPLIER	FBCSE(Fixed base-2 common sub expression)
	165mw@ 200MHZ	129mw@ 200MHZ	227mw@200MHZ
Critical path delay(ns)	12.294	11.3	15.6

Table-VII: FPGA Resources profile of 2D Image filter using Proposed Algorithm.

Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
Number of bonded IOBs	74	960	7%
Number of buffctrls	16	32	3%
Number of DSP48Es	-	192	0%

The designed BCSE algorithm based multiplier is tested in the image convolution. The 3x3 pixel matrix used 9 multipliers and which are connected in parallel. So that the speed is increased.

V. CONCLUSION

3 bit BCSE and 2-bit BCSE is implemented on Reconfigurable architecture using FPGA with less complexity. The number of resources utilized in the designed multiplier is reduced. The designed multiplier tested in the FIR based Gaussian filter and verified the number of resources are reduced to 90. The 2D convolution process for 3x3 image required clock cycles are 3 approximately. and power consumption of designed image 2d-convolver is takes 100mw for 3-bit BCSE and 165me for 2 bit BCSE.

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