Subthreshold Region based Linear Feedback Shift Register

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***Abstract*: Growing demand for portable devices and fast increases in complexity of chip cause power dissipation is an important parameter. Power consumption and dissipation or generations of more heat possess a restriction in the direction of the integration of more transistors. Several methods have been proposed to reduce power dissipation from system level to device level. Subthreshold circuits are widely used in more advanced applications due to ultra low-power consumption. The present work targets on construction of linear feedback shift registers (LFSR) in weak inversion region and their performance observed in terms of parameters like power delay product (PDP). In CMOS circuits subthreshold region of operation allows a low-power for ample utilizations but this advantage get with the penalty of flat speed. For the entrenched and high speed applications, improving the speed of subthreshold designs is essential. To enhance this, operate the devices at maximum current over capacitance. LFSR architectures build with various types of D flip flop and XOR gate circuits are analyzed. Circuit level Simulation is carried out using 130 nm technologies*.

Keywords: subthreshold region, superthreshold region LFSR; Low Power, DIBL, INWE

I. INTRODUCTION

Now a days, the most prominent developing field is low power based digital integrated circuits implementation and the objective is to attain high chip density and throughput. These requirements are used to achieve various movable applications like pacemakers, cell phones etc.The shorter battery life time enforces a challenge on the power consumption of the portable system, so there is a necessity to cut down the power utilization. The most frequently used methods to diminish the power dissipation viz constant voltage scaling, switched capacitance minimization approaches, interconnect and logic optimization.

The increasing significance of the deep submicron technology devices leads designers to concentrate on minority carriers that are exists under the gate when the gate voltage is smaller than threshold value. These carriers take crucial part in device and circuit performance.

In the beginning, these carriers are neglected as they cause “leakage” current and thus limiting the circuit performance. That current is called as subthreshold current. This current present in a circuit can be utilized for its operation which is termed as sub threshold logic. In this logic the circuit operated (supply) voltage is below the threshold voltage ($V_{dd} < \Phi_t$) nearly few hundred milli volts.

As the complete logic of chip operates in subthreshold region, power dissipation (P_D) can be reduced immensely. However the penalty of speed degradation is also obvious. One favorable method to obtain high speed subthreshold logic design is found by the maximum current over-capacitance ratio of a transistor [1].

Increase in integration density of VLSI Designs, associated components in the structure is inaccessible and examine the chip becomes major challenging task. Different issues like raise in test cost are being experienced by the test industry, when external Automatic Test Equipment (ATE) is used for testing. To solve this problem, on chip built in self test (BIST) architectures are introduced. A building block which is used to generate random test pattern is very crucial in BIST construction. Many test pattern generators are employed in BIST, out of those, LFSR is broadly used due to its capability to generate huge random sequences [2].

II. MOS TRANSISTOR OPERATION IN SUBTHRESHOLD REGION

In general, drain current of a MOSFET is said to be zero when $V_{gs} < \phi_t$, but practically it is not possible. This subthreshold current can be utilized for operating current for a variety of analog and digital circuits in weak inversion region (or subthreshold region). The main advantage working at this region is that the output current is related exponentially with input voltage somewhat than quadratic relationship to the input voltage in saturation region. This increases transconductance of the MOSFET and so getting high gain. The action of the MOS transistor in weak inversion region is similar to the bipolar junction transistor [3]. Different parameters of nMOS and pMOS transistors in weak inversion region are analyzed here.

A. Drain Current

The current conduction in weak inversion region (I_{DSub}) is possible due to diffusion. It can be formulated as [4]:

$$I_{DSub} = I_0 e^{\left(\frac{V_{gs}-\Phi_t}{mV_T}\right)}\left(1 - e^{-\frac{V_{ds}}{V_T}}\right), V_{ds} < 3V_T$$

$$I_{DSub} = I_0 e^{\left(\frac{V_{gs}-\Phi_t}{mV_T}\right)}, V_{ds} > 3V_T \quad (1)$$

(2)

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Where, I_0 is the current when $v_{gs} = \Phi_t$ and is specified by

$$I_o = \mu C_{ox} \frac{W}{L} (m-1) V_T^2$$

Channel width and length of the transistor are W and L , μ is mobility of carrier, C_{ox} is gate- oxide capacitance per unit area, Φ_t is threshold voltage, V_T is Volt-Equivalent of Temperature (V_T = KT/q) and m is subthreshold slope factor ($m=1+C_d/C_{ox}$). Fig.1. displays the drain current versus width of the transistors.

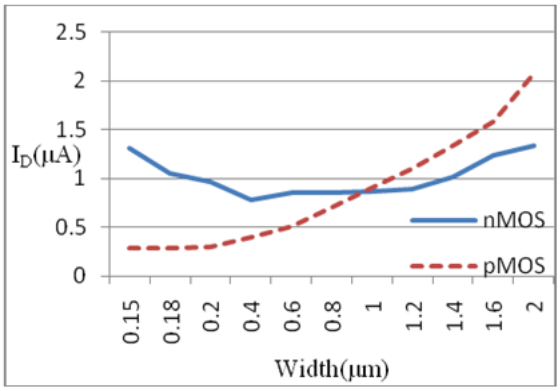


Fig.1. Current Versus Width.

From the above fig., subthreshold current increases with an increase in width of a pMOS transistor. But in case of nMOS transistor, current decreases with an increase in width owing to Inverse Narrow Width Effect (INWE) of threshold voltage, later on current raises with an increase in width.

B. Threshold Voltage

The MOS transistor threshold voltage differs with source-to-body voltage (V_{sb}) and drain to source voltage(V_{ds}) as stated below:

$$\Phi_t = \Phi_{t0} - \gamma V_{bs} - \lambda V_{ds} \quad (3)$$

Where ϕ_{t0} is ϕ_t with zero bias, γ is body effect parameter, λ is Drain Induced Barrier Lowering (DIBL) coefficient.

At the beginning transistor's threshold voltage raises with increasing its width as a result of INWE [5]. After that it remains constant. Fig.2 presents nature of threshold voltage versus width of transistors.

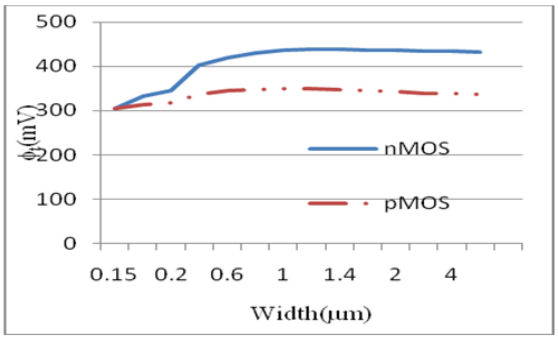


Fig. 2. Threshold Voltage Versus Width

C. Capacitances

The circuit speed is effected by the total capacitance switched during transitions. Here the gate and diffusion capacitances are taken to get the total capacitance performance of MOS transistor against its width. Fig.3. shows that capacitance versus width of transistors.

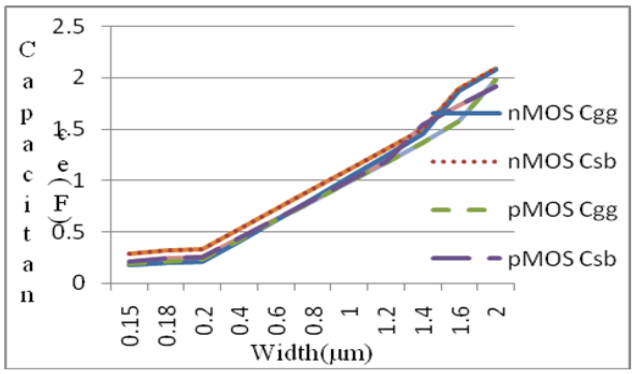


Fig. 3. Capacitance Versus Width.

From the above figure, the capacitance in subthreshold region raises with increase in width.

The relationship between Load capacitance (C_L), Supply voltage (V_{DD}) and mean current (I) in CMOS Logic are given by

$$t_p = \frac{C_L V_{DD}}{2I}$$

(4)

Where t_p is Propagation delay.

The above mathematical statement presents that propagation delay is directly proportional to supply voltage also inversely proportional to current over capacitance. For attaining maximum speed, the high current over capacitance is required.

D. Current-Over-Capacitance (COC) ratio

The current over capacitance in weak inversion region is determined by

$$COC = \frac{I_D}{C_{gg} + C_{Sb}}$$

(5)

Where I_D is Drain current, C_{sb} is source to bulk capacitance and C_{gg} is total gate capacitance [6].

Fig .4. shows the COC ratio versus various widths of MOS transistors.

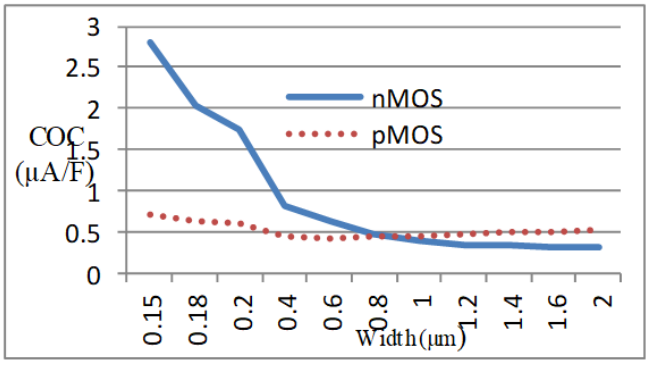


Fig. 4. COC Ratio Versus Width

Above fig. states that, the best COC value take place at least width (i.e. 0.15μm) by nMOS transistor but in case of pMOS leading COC exits at two points, one is at minimum width (i.e. 0.15μm) and other is at widths above 1.4 μm. The widths of pMOS and nMOS transistors are chosen in this work according to the maximum COC ratio and are

1.4um for PMOS and 0.15um for nMOS transistors.

III. LINEAR FEEDBACK SHIT REGISTER

In LFSR input of the first flip flop is a linear operation of past registers output. Two main components employed to construct it are D flip-flops and modulo-2 adders (XOR). The linearity property of LFSR comes from XOR gate. XOR function is linear binary operation because any single change of an input is causing an output change, independent of the state of other input. It is principally a shift register with a feedback, when clock signal is applied, then signal transmitted through the LFSR from one stage to later. So, the output sequence generated with shift register depends on the signal feedback to the input of modulo two adders. Due to this nature LFSRs are used in several applications like error correction and detection, scrambler and descrambler circuits in communication, data encryption and decryption circuits in cryptography. Fig.5 represents 4-bit LFSR Architecture and its simulation results.

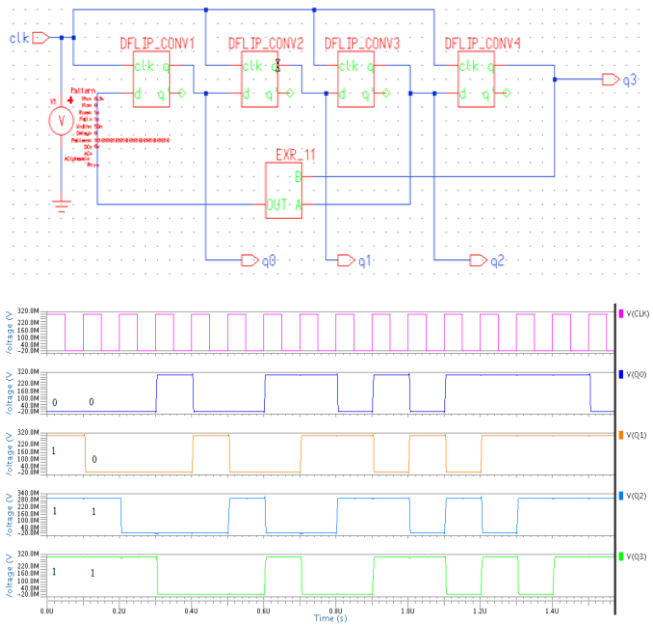


Fig.5. 4-bit LFSR Architecture and Its Simulation Result.

From the result of 4-bit LFSR where the initial state is "0111".Once the clock is applied the feedback function output data is fed to the first flip flop and meanwhile the flip flops data is shifted successively generating the next state "0011". For each shift, it generates a new state.

The 4-bit LFSR produces 15(2^4-1) states because it cannot generate "0000" state.

Input which is influenced by outputs is called taps.

Grouping of taps and their location are commonly termed as polynomial. For example: polynomial X^4+ X +1 represents the taps are taken at the first, fourth bit positions calculated from left. The end '1' in the polynomial means X^0, it always appears in feedback path but does not resembles to a tap. Not all the polynomials used by LFSR will generate a maximum length sequence. The primitive polynomials are characteristic polynomials of an n-bit LFSR which generates maximum possible sequences (i.e., $2^n - 1$) and also called as irreducible polynomials [7], [8].

IV. ELEMENTS OF AN LFSR

An elements of LFSR are Data flip flops and modulo-2 adders. Flip flops are engaged for constructing the shift register while XOR is employed in design of feedback path. Composition for different flip flops and XOR gates operated at weak inversion region are discussed in this section.

A. Flip Flops

Data flip flop tracks the input; it means that output changes according to input when input data is given on D input and remains in the same state until the input changes. Realization of LFSR is presented by four architectures of master slave D flip flops [9].

Basic NAND Flip flop:

Two Data latches are resided by D flip flop as shown in Fig.6. When the master D latch clocked at logic '0', it said to be active and allows input signal. For the time being, the slave latch remains idle. The slave latch is an active and it transmits input signal from master output to slave output, when a clock signal switches from low to high; at that time master latch turn into idle and blocks a new input.

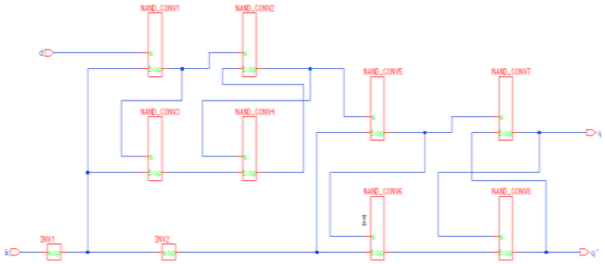


Fig.6. Basic NAND Flip Flop

Flip Flop using Transmission Gates (TGMS):

It composed four inverters and four transmission gates as shown in Fig.7. The activation and deactivation actions of master and slave stages are forced by complementary clock signals. Upper transmission gate and inverter in each stage are used to hold the signal when it is in inactive state.

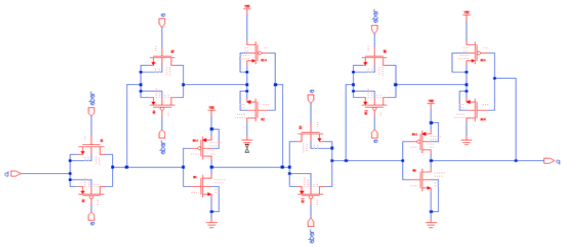


Fig.7. Flip Flop using Transmission Gates

Clocked CMOS (C^2MOS) Flip Flop:

C^2MOS Flip-flop exhibits in Fig.8 and is made with C^2MOS-logic style. This logic is implemented by nMOS and pMOS transistors in the form of a pull-down and pull–up structure.C^2MOS architecture is constructed by a conventional CMOS logic circuit with high impedance output, master and slave actions depend on 'c' and 'cbar' signals.

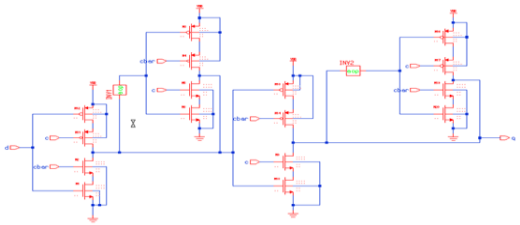


Fig. 8. C^{2}MOS Flip Flop

Power PC Flip Flop:

This flip-flop is designed by using both Transmission gate and C^{2}MOS logic as given in Fig.9. It consists of cascaded master and slave latches and they are controlled by complimentary clock signals. Each latch composed of one transmission gate, one C^{2}MOS inverter and one static CMOS inverter. When a clk is at logic zero, the master receives the reversed D input at its output. At the same time the slave holds the value of D input caught by the past clock cycle. When the master latch clocked at logic one, it holds the reversed input i.e. allowed during the clk is logic zero. Now slave latch takes reversed input hold by master latch i.e. original D value.

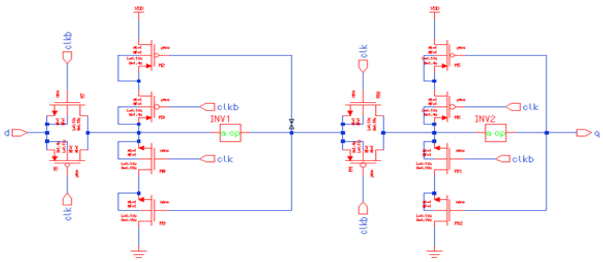
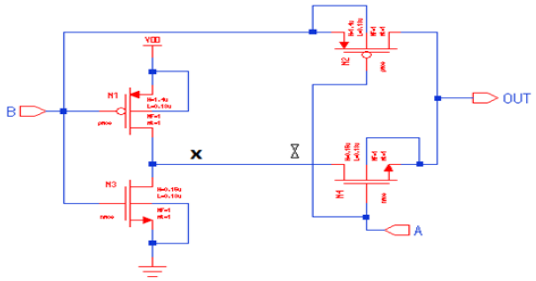


Fig.9. Power PC Flip Flop

B. XOR Gates

XOR gates play a major role in pseudo random sequence generator i.e. LFSR. It is essential to design XOR circuit with low power and better reliability. Fig. 10 shows different XOR gate circuits [10].



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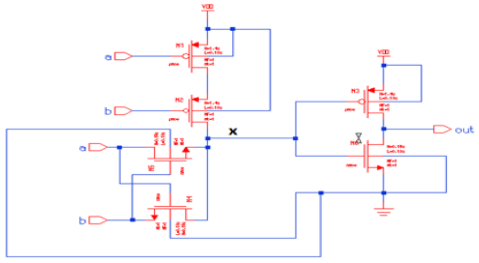

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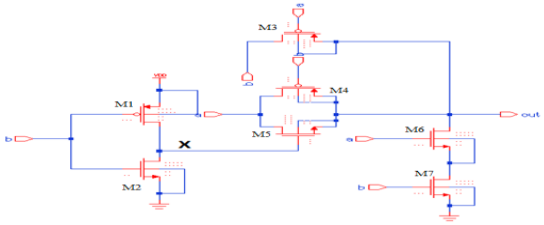

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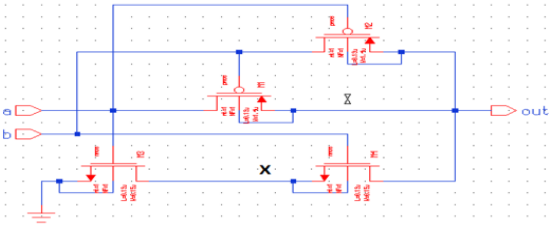
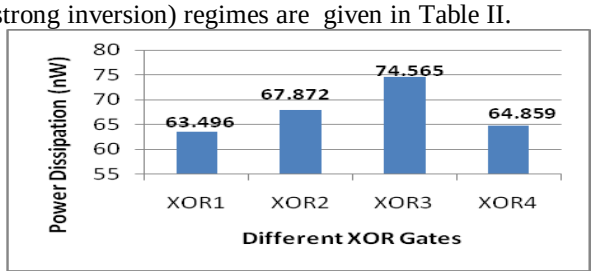


(d)

Fig. 10. Various XOR architectures.
(a) Inverter XOR gate (XOR1).
(b) XOR gate using Pass Transistor Logic (XOR2).
(c) 7T XOR gate (XOR3). (d) Power Less XOR gate (XOR4).

V. Simulation Results

This section presents simulation results of the LFSR architectures as per the following simulation environment, at CMOS 130nm technology, supply voltage V_{DD}=0.3V and 10MHz operating frequency. The fig.11. shows the power dissipation of 4 bit LFSR with various Flip Flops and XOR circuits and minimum power dissipation of each case is tabulated in Table I. P_D and PDP of 4 bit, 8 bit and 16 bit LFSR structures in subthreshold and super threshold (or strong inversion) regimes are given in Table II.



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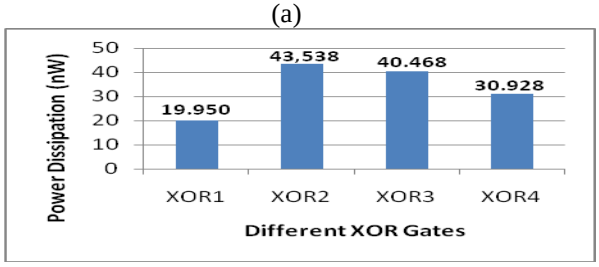

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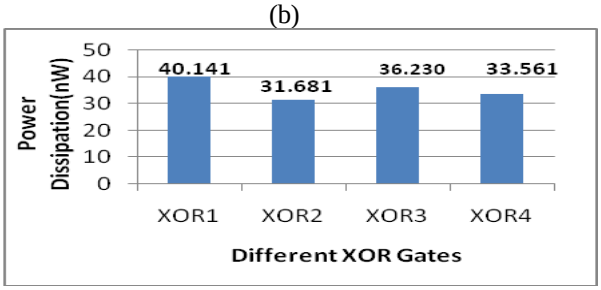

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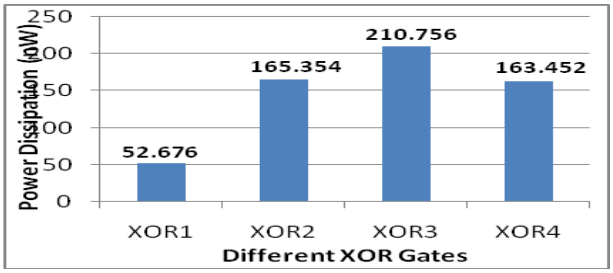

(d)

Fig. 11. Power Dissipation of 4-bit LFSR with different D Flip Flops and XOR gates.
(a) Basic NAND (b) TGMS (c) C^2MOS (d) Power PC

Table-I: 4 Bit LFSR Power Comparison Results

LFSR	Minimum Power Dissipation (nW)
Basic NAND D Flip-flop with Inverter XOR	63.496
TGMS D Flip-Flop with Inverter XOR	19.9509
C^2MOS D Flip-Flop with PTL XOR	31.6812
Power PC D Flip-Flop with inverter XOR	52.6761

Table II: 4,8,16 bit LFSR Power and PDP Comparison

LFSR	P_D in weak inversion region (nW)	P_D in Strong inversion region (mW)	PDP weak inversion Region (J)	PDP Strong inversion Region (J)
4-BIT	19.95	3.4492	3.7802×10^{-17}	3.6095×10^{-09}
8-BIT	125.619	5.677	6.5697×10^{-15}	2.9690×10^{-10}
16-BIT	165.019	7.955	3.6350×10^{-16}	1.7496×10^{-11}

IV. CONCLUSION

Subthreshold design is an imminent option in the semiconductor arena accomplishing ultra-low power utilization. The power delay product improves for the design implementation based on component optimization in subthreshold operation. So LFRSs are designed in subthreshold region. The comparison is made among different circuits in terms of power and PDP.

The simulation results illustrate that LFSR designed using TGMS Flip Flop and inverter XOR circuit has less power dissipation i.e. 19.9509 nW. The same LFSR is designed in strong inversion region and the value of power dissipation found to be 3.45 mW. Hence LFSR operating in sub threshold region has less power dissipation than LFSR operating in super threshold region. 4-bit, 8-bit and 16-bit LFSR's performance in both weak and strong inversion regimes are analyzed and power, power delay product (PDP) comparison results are placed.

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