

Impact on Gain and Noise : ECG Amplifier & Comb Filter Design using OTA

Rohith Bala Jaswanth B, V. V. K. D. V. Prasad, M. Kamaraju

Abstract: The research paper ventures a novel modelling strategy of finite gain and noise of an electrocardiogram (ECG) amplifier at 0.18, 0.5 and 0.9 micron standard CMOS technologies respectively. An active comb filter is used to design the amplifier for removing the selected frequencies of numerous signals. The presented filter is configured with only Operational Transconductance Amplifiers (OTAs) and capacitors that makes it apt for implementation of monolithic integrated circuits (ICs). The relevance of this analog circuit is verified for a suitable test signal of 60 Hz as in the ECG signal. Using Cadence Virtuoso analog design environment, the effect of transistor channel length and width is examined for analysis of noise and bandwidth. It is observed that the performance in terms of noise and gain considerably increases for advanced technology node. However, for a suitable supply of bias current, a portable ECG system can also provide an improved bandwidth performance of advanced CMOS technology.

Keywords : Bias current, Electrocardiogram (ECG), Harmonic distortion (HD), Integrated circuits (ICs), Operational transconductance amplifier (OTA), Switched capacitor (SC), Voltage controlled current source (VCCS).

I. INTRODUCTION

In recent years, the clinical practices widely used the computerized electroencephalogram (EEG), electrocardiogram (ECG), and magneto-encephalogram (MEG) systems [1] due to their suitable property of processing and recording of different biomedical signals. The advantages of using such systems are multi-fold such as 1) consequent comparison and evaluation process can be enabled by the assembly of a large signal database, and 2) feasibility can be increased with the broadcasting of biomedical signals over communication networks in real time [2]-[4]. The realization of this portable ECG/EEG recording is significant for monitoring the biological subjects without any limitation of the mobility [1]-[8]. Using such devices, the monetarization of a subject's ECG/EEG can be successfully made to operate in an out field physical concepts [8]. In many compact applications, it is utmost required to reduce the device weight and size without compromising the quality of recording.

Revised Manuscript Received on August 20, 2019.

* Correspondence Author

Rohith Bala Jaswanth B*, Electronics and Communication Engineering, JNTUK, Kakinada, India. E-mail: jaswanth.78@gmail.com

Dr. V. V. K. D. V. Prasad, Electronics and Communication Engineering, Gudlavalluru Engineering College, Gudlavalluru, India.

Dr. M. Kamaraju, Electronics and Communication Engineering, Gudlavalluru Engineering College, Gudlavalluru, India.

The primary goal is to process the ECG/EEG monitoring system in the absence of consciousness of the biological subject [9]-[12]. It can be accomplished by using an integration of IC, and combining with Analog circuitry used at the front end and a remote computer can be used to perform the telemetry operation on the bio-potential signals [10]. In order to measure a single bio-potential signal, a few researchers [12]-[15] have been reported the implementation of AFE using the IC approach. However, in practice, the signals of EEG and the ECG are categorized to be weak, with amplitude up to 100 and 5 milli volts respectively [16]. For normal operation, the bandwidth of ECG signal of 0.1 - 150 Hz range. Additionally, one can obtain a voltage of a half-cell as ± 300 mV and a maximum noise voltage is $< 30 \mu V_{pp}$ for a bandwidth ranging from 0.1 - 150 Hz. The above mentioned voltages can be obtained due to the phenomenon of the interface between the electrode and skin. For a 50/60 Hz supply (mains), the common-mode interface voltage primarily controls the ECG signal. As, for example, if a patient becomes departed from the earth ground, estimated signal of common-mode that sets with a human body would be as high as 1 mg [15]- [17].

To preprocess a cardio signal, it is required to amplify the signal by 10-100 times by using a pre-amplifier with small input noise. One of the most popular techniques of implementing an ECG monitoring system is the switched-capacitor (SC) integrated circuit topology [18]-[19]. However, the circuit of Sample & Hold (S&H) of the topologies of switching are not fit due to its leakage problem and large time constant (in milliseconds or more). In order to remove the leakage, it is normally required to adopt the leakage-reducing mechanism in SC integrated circuitry [20]. Hence, the researchers find a way to use a low-power operational transconductance amplifier (OTA) based filters. Filters are generally configured with OTA in integrating circuits of open loop counting Comb (OTA-C) [19]-[26]. In these filters, to identify a low transconductance value in the order of nano-amperes per volt, the integrated devices (ICs) are normally operated in the subthreshold region. In OTA-based filters, the performance of the filter circuits are primarily dominated by the operational amplifiers and the time constants can be resolved from the limited transconductance to the capacitor ratio.

For analog filter based circuit designing, the operational amplifiers (Op-Amps) are the primary functional units. However, the limitations on bandwidth and slew rate of operational amplifiers lead the analog designer to search for other possibilities. Recently, operational g_m amplifier



(OTA) is considered as the most suitable constructional blocks in analog signal processing (ECG amplifiers) due to its higher bandwidth, slew rate, and transconductance gain [27]-[32]. In addition a current input is used to regulate the amplifier's g_m . Hence, the circuits developed using OTAs are most likely to possess intrinsic electronic control of parameters such as the cutoff frequency, quality factor, gain of a filter,

and the oscillatory conditions for an oscillator [28], [33], [34]. The designing of a systematic OTA-based filter, the

following are observed: 1) determining the filter's specification and set up can be appropriate for the procuring of bio signals; and 2) determining the suitability of building cell to construct this filter with a chosen topology. Certain characteristics such as tolerance and bandwidth of the ECG signal primarily decides the first consideration. However, the second consideration needs to be obtained by a detailed analytical model based on the non-ideal factors produced by OTA. In designing of continuous-time filter, the performance of the analog circuit normally depends on the harmonic distortion and the signal power.

This research paper presents the novel gain and noise modelling approach using an analog comb filter based notch filter. The presented filter is developed using all OTAs and capacitors. Therefore, it can be referred as an OTA-C comb filter and suitable for the implementation of integrated circuits (ICs). In practice, the transconductance gain and the intrinsic noise are described as behavioral models for constructing the basic block. Each of the basic blocks is represented by an OTA consisting of PMOS and NMOS transistors. The aspect ratio of each transistor in the proposed filter are designed at CMOS 0.18,0.9 and 0.5 micron technology nodes. The comb filter parameters are easily tuned electronically using bias current of the OTAs. The designed transistor based filter circuit is simulated for different bias currents at a suitable ECG test signal of 60 Hz. Further the paper is formulated into 3 sections: The modelling and designing technique is depicted in Section 2. The Section 3 demonstrates the ECG performance, such as gain, bandwidth and noise at different technology nodes. Finally, Section 4 draws a brief summary of the paper.

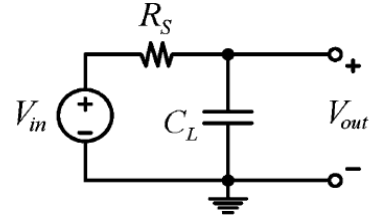
II. MODELLING AND DESIGNING

The OTA is the elemental chunk of an In-amplifier which is used for ECG amplification. Designing of the OTA design is performed as a series connection pairs with the current mirroring circuitry. In the proposed designing technique, PMOS devices are preferred over NMOS due to the less flicker noise [33]. In order to diminish the 1/f noise, the transistor's W/L ratio contained in the first stage amplifier need to be improved. No variation in the noise performance is evidenced due to the second stage amplifier set up.

The Fig. 1(a), shows an RC passive filter of order one which is the series connection of a resistor voltage source transformed into the Norton's equivalent current source. However, an active filter realization contains, replacing the

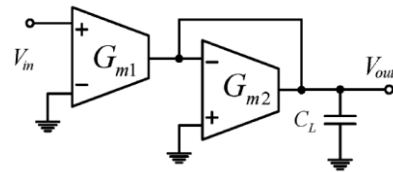
passive components by the real OTA's circuits and can as illustrated in Fig. 1(b). The filter circuit incorporates an equivalent grounded resistor and an input V to I transducer of closed OTA. Its transfer function can be defined as [26]

$$\frac{V_{out}}{V_{in}} = -\frac{G_{m1}}{sC_L + G_{m2}} \tag{1}$$



(a)

To analyze the performance of the first order filter, the modelling of OTA nonlinearity is an important factor. For the designing of active filter in Fig. 1(b), several non-linear effects such as nonlinear output current for different input pairs, finite output resistance of the current sink / source, etc. can be observed. Therefore, it is almost impossible to evaluate the response of system, without considering the effect of non-linear models. The non-linear model primarily includes the modelling of intrinsic noise and limited magnitude gain of the OTA based filter circuit. Modelling of these factors are discussed in following sub-sections.



(b)

Fig.1. A first-order filter circuit: (a) Passive RC network and (b) Active OTA realization circuit.

A. OTA Finite Gain

In general, the infinite gain of an OTA can be obtained from equation (1). However, in practical circuit, a large integrator loss can be happened by a finite resistance that is again due to the channel length modulation. It further influences the overall response of the filter circuit. Therefore, considering the output response of OTA as $1/g_o$, the transfer function of Fig. 1(b) can be expressed as [26]

$$\frac{V_{out}}{V_{in}} = -\frac{G_{m1}}{sC_L + G_{m2} + 2g_o} \tag{2}$$

To analyze the gain, a general architecture of a voltage-mode OTA comb filter is designed as in Fig. 2 [35].

The active network of this architecture primarily consists of 1) n number of internal nodes, denoted as x_i , where $i = 1, 2, 3, \dots, n$; 2) an active network with n number of transconductors(input side), G_{mbi} ; 3) a collective feed forward and transconductors(feedback), G_{mij} ; 4) a feed forward

transconductors, G_{md} ; and 5) an output summer consisting of transconductor, G_{mci} , G_{mo} . Similarly, the passive network consists of 1) input capacitors, C_{bi} , where $i = 1, 2, \dots, n$; and 2) a grounded and floating capacitor, C_{ij} , where $1 \leq i < j \leq n$.

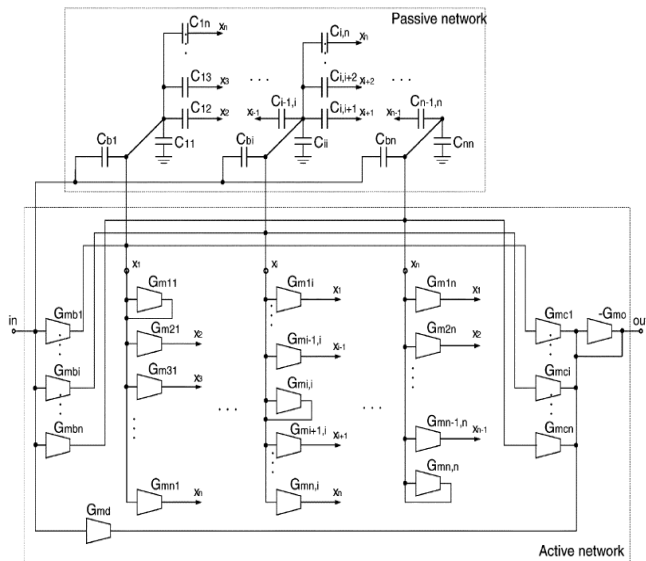


Fig.2. General block diagram of a voltage mode OTA comb filter [35]

Now, considering the voltage at each node x_i , the transconductance gain (G) in matrix form can be expressed as

$$G = \begin{bmatrix} G_{m11} & G_{m12} & \dots & G_{m1n} \\ G_{m21} & G_{m22} & \dots & G_{m2n} \\ \dots & \dots & \dots & \dots \\ G_{mn1} & G_{mn2} & \dots & G_{mnn} \end{bmatrix} \quad (3)$$

All the matrix parameter values can be obtained from [35]. Using the modelling expression of (3), the basic behavioral model has been developed with SIMULINK tool. The designed basic filter is integrated in higher-order filter circuit to demonstrate the performance.

B. OTA Noise

The performance of OTA is primarily influenced by the following two main sources of noise: 1) flicker and 2) thermal noise. The Flicker noise, defined as a noise system that primarily produces an inverse frequency with the power density curve. At low frequency band, the flicker noise specifically impacts the transconductance of OTA. The other term of Flicker noise is $1/f$ noise due to its inverse noise power spectral density to the frequency. Thermal excitement leads to thermal noise. It can occur for any applied voltage. In ideal condition, the output noise of OTA is affected by these two types of noise factors.

The noise of an OTA is expressed by an equivalent input-voltage noise source shown in Fig. 3. In this representation, the noise of a CMOS transconductor input

noise source (v_n) [26]. Therefore, the spectral density, modeled as

$$S_n(f) = \frac{S_t}{g_m} + \frac{S_f}{f} \quad (4)$$

where S_t and S_f are represented as thermal and flicker noise components. The magnitudes of these two parameters are primarily dependent on the transconductor topology and biasing.

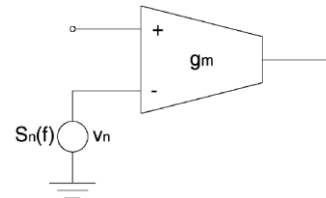


Fig.3. OTA noise representation using an input-output voltage noise source

According to the general noise equation in HSPICE Elements and Device Models Manual NLEV = 2 [26], the input $1/f$ noise power spectral density can be derived as

$$S_{f,in} = \frac{KF}{C_{OX} \cdot W_{eff} \cdot L_{eff} \cdot f^{AF}} \quad (5)$$

Where the KF is a coefficient and AF is exponent constants of flicker noise respectively; W_{eff} is the width of effective channel and L_{eff} are the channel length; the oxide capacitance per unit area is represented by C_{OX} . Moreover, the PSD of input thermal noise is modelled in terms of OTA transconductance gain (G) and can be expressed as

$$S_{th,in} = \frac{4 \cdot \gamma \cdot k_b \cdot T}{G} \quad (6)$$

Where, KB and T represent the Boltzman's constant and the temperature in degree Kelvin, respectively. The value of γ is primarily dependent on the operating region of a transistor. Most of the transistors of OTA are supposed to function in the sub threshold region in order to cater the frequency and low power requirements of an OTA comb filter. Thus, the value of γ is chosen as $(1/2\kappa)$ for sub-threshold operation. The typical value of κ is 0.7 and $\kappa = 1/\eta$, where η represents the slope factor [36], [37].

III. GAIN AND NOISE ANALYSIS

Earlier, the portable devices of ECG monitoring were based on discrete components for designing of Analog FE. These devices were cumbersome for system recognition and deplete power. Now-a-days, with the advancement of VLSI technology, the portable ECG devices provide an attractive solution of monitoring tasks as



a number of components can be reduced together to obtain a less power consuming ability.

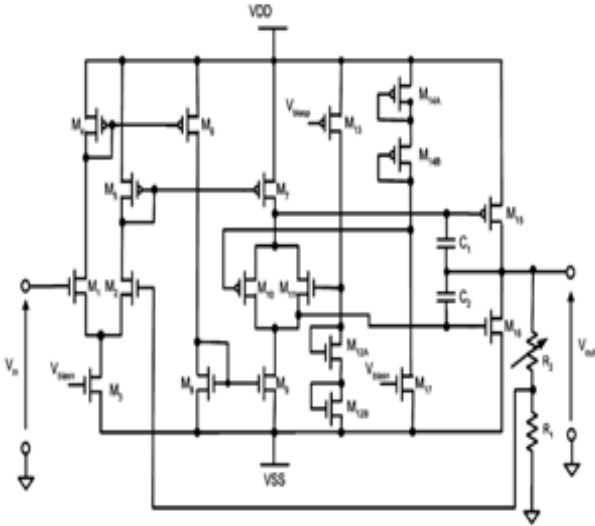


Fig.4. Circuit schematics for simulation

Thus, the OTA based ECG system topology becomes popular in recent times. This section presents the performance analysis of an OTA based ECG system of phase, gain, noise and bandwidth as well.

In analyzing the performance [40], the OTA of Fig. 4 is simulated using cadence virtuoso analog design environment at 0.18, 0.5 and 0.9 micron technology nodes of CMOS [38], [39]. The sizes of the (MOS) transistors are given in Table below. The biasing voltages used in simulation are $V_{dd} = 1.8$ V and $V_{ss} = -1.8$ V. Input voltage is 1V sine signal [39]. R_1 and R_2 in Fig. 4 are the imbalance between the resistors, which can affect the factor called gain. Therefore, the I/O relationship of the OTA is established as

$$V_{out} = V_{in} \times \left(\frac{R_2}{R_1} + 1 \right) \quad (7)$$

Table- I: Dimensions of MOS Transistors at Different Technology Nodes

Transistor Name & type	Channel width (μm)	Channel Length (μm)	Technology Node (μm)
NMOS: $M_1, M_2, M_3, M_8, M_9, M_{11}, M_{12A}, M_{12B}, M_{16},$ and M_{17}	1.8	0.18	0.18
	5	0.5	0.5
	9	0.9	0.9
PMOS: $M_4, M_5, M_6, M_7, M_{10}, M_{13}, M_{14A}, M_{14B},$ and M_{15}	4.5	0.18	0.18
	12.5	0.5	0.5
	22.5	0.9	0.9

Using the circuit schematic of Fig. 4 and the transistor dimensions from Table I, the analysis of gain and noise are described in the following sub-sections.

A. Gain and Bandwidth Analysis

Physiological signal such as ECG signal primarily contains the mains line harmonics and its frequencies along with signal at input. The recommended comb filter is composed to defeat undesired signals of fundamental frequency of 60 Hz in ECG signal. The values of the internal capacitors C_1 and C_2 in Fig. 4 are chosen as 5 μF and 21 nF, respectively. The variable resistance (R_2) is adjusted to 100

k Ω by biasing the current of the corresponding OTA circuit. For a fixed bias current of 263.4 μA , the phase vs frequency response at 0.18 μm , 0.5 μm and 0.9 μm are showcased in Figs. 5, 6 and 7, respectively. Similarly, the gain vs frequency response at 0.18 μm , 0.5 μm and 0.9 μm are shown in Figs. 8, 9 & 10, respectively. Both the phase and gain factor increases at 0.18 μm technology nodes. However, the overall cutoff frequency (*i.e.*, 3 dB bandwidth) reduces at 0.18 μm technology node as compared to 0.5 and 0.9 μm technology nodes. The primary reason behind is that for an increase of transistor width and channel length (*i.e.*, at higher technology nodes), the current through the transistor channel increases. It encouragingly increases the overall gain and phase of an OTA based ECG system. However, for an increase in overall gain, the bandwidth (*i.e.*, the frequency range the op-amp can respond to) decreases. At lower frequencies, due to a lesser electromagnetic induction effect, a less amount of signal is interfered inside and hence there is a better match between the effective amplitude of the output and the predicted gain. Thus, the overall bandwidth for 0.18 μm technology node reduces. The quantitative values of bandwidth for different technology nodes are summarized in Table II.

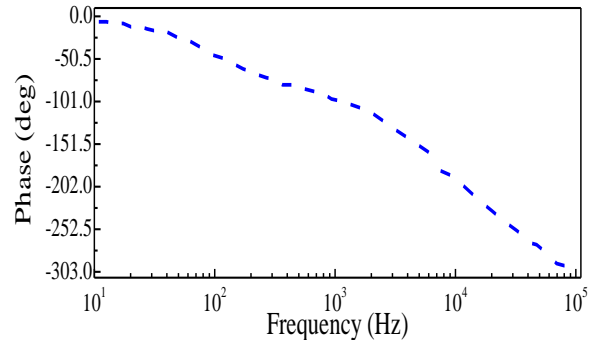


Fig.5. Phase margin analysis at 0.18 μm technology node

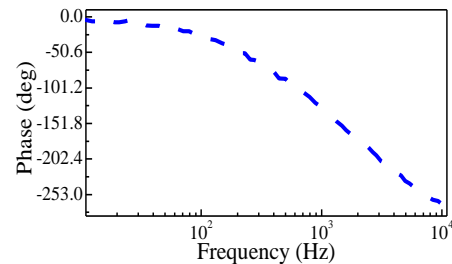


Fig.6. Phase margin analysis at 0.5 μm technology node

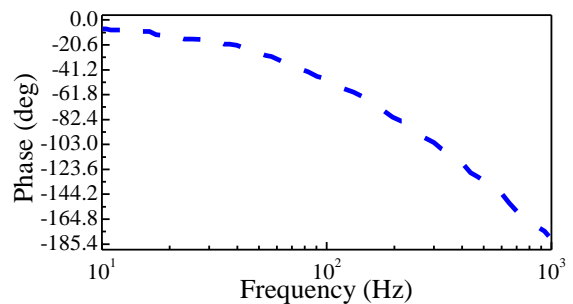


Fig.7. Phase margin analysis at 0.9 μm technology node

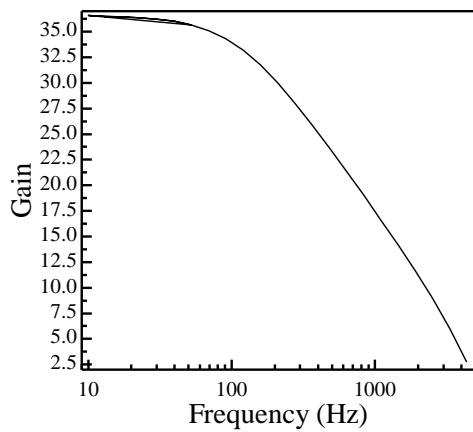


Fig.8. Frequency response of OTA at 0.18 μm technology node

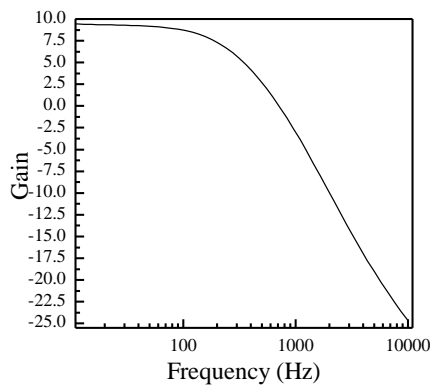


Fig.9. Frequency response of OTA at 0.5 μm technology node

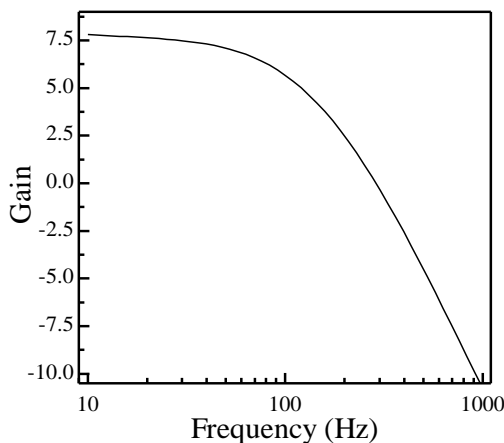


Fig.10. Frequency response of OTA at 0.9 μm technology node

Table-II: The bandwidth of OTA based ECG for different technology nodes

Technology Nodes (μm)	Gain (dB)	Bandwidth (Hz)
0.18	36.21	105.72
0.5	9.78	136.20
0.9	7.73	283.36

B.Noise Analysis

In order to analyze the noise in OTA, firstly the correct input source configuration is required. Therefore, a Voltage Controlled Voltage Source (VCVS) is considered for reference. However, for a common mode gain simulation, it is required to change the values from ± 0.5 to 1. It is required to put a non-zero input common-mode voltage. This idea is used for the noise analysis.

Here, the thermal & flicker noises analysis is done in Cadence for different technology nodes of 0.18, 0.5 and 0.9 microns. The quantitative values of noise at different technology nodes are summarized in Table III. It is observed that at 0.18 μm technology node, the ECG system performs an improved noise factor at 60 Hz frequency.

Table-III: Flicker and Thermal Noise of an ECG for Different Technology Nodes at 60 Hz Frequency

Technology Nodes (μm)	Flicker Noise (nV)	Thermal Noise (μV)
0.18	1.16	5.62
0.5	2.76	47.86
0.9	9.18	68.31

IV. CONCLUSION

This research paper presented an active Comb-C filter. The filter is constructed with all OTAs and capacitors. All the PMOS and NMOS transistors are designed at 0.18, 0.5 and 0.9 microns CMOS technology nodes. The bias current of this analog circuit is primarily controlled by the controlling voltage of the OTA.

The performance is analyzed for different factors of transistor channel length and width. It has been observed that although the ECG performance in terms of gain, bandwidth and noise increase at advanced technology node, but the effective bandwidth reduces for lesser channel length. However, the bandwidth at 0.18 μm technology node (*i.e.*, for advanced VLSI system) can be increased for an increase in bias current of OTA. Therefore, the portable OTA based ECG system can provide an improved performance at 0.18 μm CMOS technology

REFERENCES

1. J. Willems, "Common standards for quantitative electrocardiography," *J. Med. Eng. Techn.*, vol. 9, 209–217 (1985).
2. N. S. Jayant and P. Noll, *Digital Coding of Waveforms*, Englewood Cliffs, NJ, Prentice-Hall, 1984.
3. U. E. Ruttiman and H. V. Pipberger, "Compression of the ECG by prediction or interpolation and entropy coding," *IEEE Trans. Biomed. Eng.*, 26(11), 613–623 (1979).
4. J. R. Cox; F. M. Nolle; H. A. Fozzard; G. C. Oliver, "AZTEC: a preprocessing program for real-time ecg rhythm analysis," *IEEE Trans. Biomed. Eng.*, 15(2), 128–129(1968).
5. S. M. S Jalaeddine, C. G. Hutchens, R. D. Strattan, and W. A. Coberly, "ECG data compression techniques: a unified approach," *IEEE Trans. Biomed. Eng.*, 37 (4), 329–343(1990).
6. J. P. Abenstein, and W. J. Tompkins, "New data reduction algorithm for real-time ECG analysis," *IEEE Trans. Biomed. Eng.*, 29(1), 43–48 (1982).
7. W. C. Mueller, "Arrhythmia detection program for an ambulatory ECG monitor," *Biomed. Sci. Instrument*, 14, 81–85(1978).
8. J. D. Bronzino, *Medical Devices and Systems*, CRC Press, Taylor & Francis, (2006).

9. O. B. C. Tsutomu, K. D. Norie, H. F. Manabu, N. G. Satoshi, M. Masako, N. Emi, and M. Tadao, "Electroencephalographic measurement of possession trance in the field," *Clin. Neurophysiol.*, 113(3), 435–445 (2002).
10. N. Utsuyama, H. Yamaguchi, S. Obara, H. Tanaka, S. Fukuta, J. Nakahira, S. Tanabe, E. Bando, and H. Miyamoto, "Telemetry of human electrocardiograms in aerial and aquatic environments," *IEEE Trans. Biomed. Eng.*, 35 (10), 881–884 (1988).
11. A. C. Metting van Rijn, A. Peper, and C. A. Grimbergen, "High quality recording of bioelectric events. II: A low-noiselow-powermultichannel amplifier design," *Med. Biol. Eng. Comput.*, 4, 433–440 (1991).
12. G. McGlinchey, S. Pietkiewicz, R. Frank, P. Schmidt-Andersen, and F. Hansen, "A programmable medical data acquisition system chip," in *Proc. IEEE Custom Integrated Circuits Conf.*, pp. 9.4/1–9.4/6, (1988).
13. T. Desel, T. Reichel, S. Rudischhauser, and H. Hauer, "A CMOS nine channel ECG measurement IC," in *Proc. 2nd IEEE Int. Conf. ASIC*, 115–118, (1996).
14. R. Martins and F. A. Vaz, "A CMOS IC for portable EEG acquisition systems," *IEEE Trans. Instrum. Meas.*, 47(5), 1191–1196 (1998).
15. K. A. Ng and P. K. Chan, "A CMOS Analog Front-End IC for Portable EEG/ECG Monitoring Applications," *IEEE Transactions on Circuits and Systems—I: Regular Papers*, 52 (11), (2005).
16. J. G. Webster, *Medical Instrumentation: Application and Design*, 3rd ed. New York: Wiley, 1998.
17. A. C. Metting Van Rijn, A. Peper, and C. A. Grimbergen, "High-quality recording of bioelectric events. I: Interference reduction, theory and practice," *Med. Biol. Eng. Comput.*, 28, 389–397 (1990).
18. L. Lentola, A. Mozzi, A. Neviani, and A. Baschirotto, "A 1- A front end for pacemaker atrial sensing channels with early sensing capability," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, 50 (8), 397–403 (2003).
19. K. Lasanen and J. Kostamovaara, "A 1-V analog CMOS front-end for detecting QRS complexes in a cardiac signal," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, 2584–2594 (2005).
20. L. S. Y. Wong, S. Hossain, A. Ta, J. Edvinsson, D. H. Rivas, and H. Nääs, "A very low power CMOS mixed-signal IC for implantable pacemaker applications," in *Proc. IEEE Solid State Circuits Conf.*, 318–319 (2004).
21. S. Solís-Bustos, J. Silva-Martínez, F. Maloberti, and E. Sánchez Sinencio, "A 60 db dynamic-range CMOS sixth-order 2.4 Hz lowpass filter for medical applications," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, 47, 1391–1398 (2000).
22. A. Veeravalli, E. Sánchez-Sinencio, and J. Silva-Martínez, "Transconductance amplifier structures with very small transconductances: A comparative design approach," *IEEE J. Solid-State Circuits*, 37(6), 770–775 (2002).
23. C. D. Salthouse and R. Sarpeshkar, "A practical micropower programmable bandpass filter for use in bionic ears," *IEEE J. Solid-State Circuits*, 38 (1), 63–70 (2003).
24. E. Rodríguez-Villegas, A. Yúfera, and A. Rueda, "A 1.25-V micropower Gm-C filter based on FGMOS transistors operating in weak inversion," *IEEE J. Solid-State Circuits*, 39 (1), 100–111 (2004).
25. X. Qian, Y. P. Xu, and X. Li, "A CMOS continuous-time low pass notch filter for EEG systems," *Analog Integr. Circuits Signal Process.*, 44, 231–238, (2005).
26. S. -Y. Lee and C. -J. Cheng, "Systematic Design and Modeling of a OTA-C Filter for Portable ECG Detection," *IEEE Transactions on Biomedical Circuits and Systems*, 3(1), (2009).
27. G. Ferri, V. Stornelli, and A. di Simone, "A CCII-based high impedance input stage for biomedical applications," *Journal of Circuits, Systems and Computers*, 20 (8), 1441–1447 (2011).
28. R. K. Ranjan, S. P. Yalla, S. Sorya, and S. K. Paul, "Active Comb Filter Using Operational Transconductance Amplifier," *Active and Passive Electronics Component, Hindawi*, vol. 2014, Article ID 587932, 1–6 (2014).
29. A. Fabre, O. Said, F. Wiest, and C. Boucheron, "High frequency applications based on a new current controlled conveyor," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, 43(2), 82–91 (1996).
30. M. T. Abuelma'atti and N. A. Tasadduq, "New current-mode current-controlled filters using the current-controlled conveyor," *International Journal of Electronics*, 85 (4), 483–488 (1998).
31. K. N. Salama and A. M. Soliman, "Active RC applications of the operational transresistance amplifier," *Frequenz*, 54 (7-8), 171–176 (2000).
32. P. Visocchi, J. Taylor, R. Mason, A. Betts, and D. Haigh, "Design and evaluation of a high-precision, fully tunable OTA C bandpass filter implemented in GaAs MESFET technology," *IEEE Journal of Solid-State Circuits*, 29 (7), 840–843 (1994).
33. R. L. Geiger and E. Sánchez-Sinencio, "Active filter design using operational transconductance amplifiers: a tutorial," *IEEE Circuits and Devices Magazine*, 1(2), 20–32 (1985).
34. S.-H. Yang, K.-H. Kim, Y.-H. Kim, Y. You, and K.-R. Cho, "A novel CMOS operational transconductance amplifier based on a mobility compensation technique," *IEEE Transactions on Circuits and Systems II: Express Briefs*, 52 (1), 37–42 (2005).
35. S. Koziel, R. Schaumann, and H. Xiao, "Analysis and Optimization of Noise in Continuous-Time OTA-C Filters," *IEEE Trans. on Circuits and Systems—I: Regular Papers*, 52 (6), (2005).
36. Y. Tsvividis, *Operation and Modeling of the MOS Transistor*, 2nd ed. New York: Mc Graw-Hill, 1998.
37. E. A. Vittoz and J. Fellrath, "CMOS analog integrated circuits based on weak inversion operation," *IEEE J. Solid-State Circuits*, 12 (6), 224–231 (1977).
38. *Predictive Technology Model*, ptm.asu.edu/.
39. *International Technology Roadmap for Semiconductors*, 2016 editions, <http://www.itrs.net>.
40. R. Gregorian, *Introduction to CMOS Opamps and Comparators*, 1st ed. New York: Wiley, (1999).

AUTHORS PROFILE



Mr. Rohith Bala Jaswanth B is a Research Scholar, pursuing Ph.D from Jawaharlal Nehru Technological University, Kakinada, and Andhra Pradesh, India. He has been working as an Academician in the capacity of An Assistant Professor in Gudlavalluru Engineering College, a reputed Autonomous Engineering College in Andhra Pradesh, India. Apart from regular Academia, the zeal to explore new technologies and a penchant towards pursuing research in the field of Analog & Digital Electronics has made him to do the research work in a governmental organization in Andhra Pradesh. His keen interests are inclined more towards devices and technologies of Analog & Digital IC design. His areas of Interest include Low Power VLSI, Probability Theory and Estimation, Pulse & Digital Circuits, Biomedical Engineering, Linear & Digital ICS and Applications.



Dr. V. V. K. D. V. Prasad, working as a Professor and Head of the Department, of Electronics & Communication Engineering, in Gudlavalluru Engineering College, an Autonomous NBA accredited College in Andhra Pradesh, India. He received Ph.D for his work in Signal Processing; in 2011 from Jawaharlal Nehru technological University, Kakinada, India. His areas of Interest include Signal Processing, Electrostatics, Electromagnetic fields and Transmission lines. He developed an abstract technical trait that addresses various other fields where digitalization can be achieved. His research findings are in the methodology used, problems encountered and thepractical implications of composite features and filtering coefficients in advanced filters. Mr. Rohith Bala Jaswanth B is a Research Scholar, pursuing Ph.D from Jawaharlal Nehru Technological University, Kakinada, and Andhra Pradesh, India. He has been working as an Academician in the capacity of An Assistant Professor in Gudlavalluru Engineering College, a reputed Autonomous Engineering College in Andhra Pradesh, India. Apart from regular Academia, the zeal to explore new technologies and a penchant towards pursuing research in the field of Analog & Digital Electronics has made him to do the research work in a governmental organization in Andhra Pradesh. His keen interests are inclined more towards devices and technologies of Analog & Digital IC design. His areas of Interest include Low Power VLSI, Probability Theory and Estimation, Pulse & Digital Circuits, Biomedical Engineering, Linear & Digital ICS and Applications.



Dr. M. Kamaraju, is working as a Professor and Mentor of Academic Strengthening and Advancement, Electronics & Communication Engineering Department, Gudlavalluru Engineering College, An autonomous Engineering institute, Andhra Pradesh, India. He received the doctorate in 2012 from Jawaharlal Nehru technological university, Hyderabad for his work in the area of Low power VLSI design entitled "Power Optimized Programmable Embedded controller". His ongoing research interest spread in the areas like Microprocessors and Microcontrollers, Embedded Systems, Bio-Medical Engineering, VLSI Design, Analog and Digital Communication.

