International Journal of Engineering and Advanced Technology (IJEAT)
ISSN: 2249-8958 (Online), Volume-8 Issue-6S2, August 2019

Design and Analysis of Multiplexer Based 4-Bit Flash ADC

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Abstract: ***In reality, signals exist in analog format. The digital circuits are more convenient than analog circuits with respect to processing speed and efficiency in transmission. Hence there is a great demand for ADC converters. The typical Flash ADC contains resistor ladder circuit, comparator and code converter. The most advantageous parameter of Flash ADC is its speed. Hence it can be used in variety of applications such as micro electronics, wireless sensor networks, transceivers. Flash ADC still suffers from minimum resolution and consumes large amount of power. However these are due to its complexity in terms of chip area requirement in comparison with other ADCs. This new technique of four bit Flash ADC using TIQ comparator is implemented here. Here, a comparison is brought between the input signals with internal built threshold using TIQ comparators. It avoids the too much resistor usage in ladder network. In general, 2^N-1 number of TIQ comparators is required to design N-bit flash ADC. TIQ output was encoded into binary by an encoder. A new MUX based encoding technique has been used to enhance the conversion speed for achieving highest sampling rate with low power dissipation. The design is simulated in Mentor Graphics environment using 130nm technology and result shows a deep reduce in the power consumption i.e.0.833µW and conversion speed 15.393ns for 4-bit ADC.***

Keywords: Parallel type of ADC, Multiplexer, CMOS comparator, power consumption.

I. INTRODUCTION

In nature, light, sound, video etc are analog. For processing these signals in digital world, ADC is required. However DAC will be required to get back analog. In systems, to integrate signals of both analog to digital converters have crucial role. As the world is digitized there is wide range of applications ranging from audio communications to medical electronics. There are wide varieties of ADC's architectures that are available, which varies in terms of performance, area and power. So that a vast investigation of alternative ADC design techniques is required. Now a day the digital systems are designed with ICs by establishing the interconnections between them to improve the speed of the system. Also input/output (I/O) bandwidth is important concern. The interconnections of the chips are used with high speed links. The term high-speed link refers to communication link between input/output (I/O) through channel by increasing necessity of bandwidth; whereas parallel channels are used to improve the data rate. In oscilloscope ADCs are used in the range of GHz with minimum feature size of resolution. These converters are used in audio and video communication applications. The different types of ADCs existing are pipeline, SAR, Sigma Delta etc. In pipeline ADC, speed of conversion time is high, but which has medium resolution. SAR ADC is used in applications which require fastest operation with medium range of resolution. Sigma-delta used for high resolution and slow speed with maximum resolution. Lastly, parallel comparator ADC is one of the fastest converters with less resolution. It has high end applications such as communication links with good data rate, instrumentation and control, oscilloscopes. In this work, designing of comparator is one of the challenges in the design of 4-bit Flash ADCs. Hence, here, Threshold Inverter Quantization (TIQ) Comparator is used in the comparator block.

Manuscript published on 30 August 2019.
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II. LITERATURE SURVEY

Power dissipation is one of the most important parameter considerations when deigning CMOS circuits. As there is an exponentially growth of increasing of ICs in the circuit, the dissipation of power is also increasing. In CMOS, along with quiescent power dissipation, other component switching power which is also greatly influenced by the charging and discharging of the current flowing through the load capacitance. This also affected by the frequency of the clock signal. Such losses are reducible using adiabatic technique. In this technique, instead of forming the charging path from supply voltage to load capacitance C_L and then discharging path to lower potential the energy can be recycled to sinusoidal supply voltage. Instead, power losses exist due to the R_{ON} of the switches. The low clock frequencies of operating signals are used to minimize that amount of power dissipation. There are several adiabatic logic families are available in literature each one has its own advantages with some limitations. Wang and Yuan gao (2012) in their paper proposed that ADC plays a prominent role in power management applications. In survey, several researches have given different ADC architectures which has small in area, high speed with low power. ADC can be implemented for an input range of 1.3V to 3.05V and the clock frequency ranges from 0Hz to 35MHz suitable for power management applications. The performance characteristics of window ADC are developed with flash, delay-line and pipeline ADC. Surchuri Tiwari and Abhishek Kumar (2016) proposed that, In TIQ comparator the internal built threshold voltage is compared with the incoming input signal, which eliminates need of power hunger overhead resistor ladder network.

Since the input reference voltage is in built for TIQ comparator which increases ADC's conversion speed and also results in lowering the power consumption. In several papers, power efficient ADC architectures are given for high speed link receivers with less area. Later single-slope A to D conversion is given with low C_{in}, good intrinsic linearity, and low power. Power dissipation is crucial for battery operated devices. The flash converter is not only simple to design but also efficient in speed, which is limited only in comparators. With the usage of unique value of resistors in voltage divider logic, successive binary count output is in proportional with the continuous input information.

III. ADC ARCHITECTURES

In literature, several ADC architectures are available. The multiple ADCs designed are successive approximation, pipeline, dual slope and sigma-delta, flash etc., has different specifications in terms of speed, accuracy, conversion time, etc.

A. Flash ADC

These also referred as parallel comparators. The parallel logic performs high speed operation as compared to other ADCs .These has best applications in high bandwidth requirement. A massive 2^N resistive network with high dissipation power with low resolution and for high resolution, it requires more expenditure. These flash ADCs have its best applications in satellite, radar communication systems, data acquisition systems. Fig. 1 shows the basic blocks of Flash ADC. For N- bit conversion, it needs $2^N - 1$ comparators. The resistor ladder comprises of resistors (2^N in number), each and every node generates the $+V_{ref}$ which can be given as input to individual comparators. Every comparator's reference is ±1LSB less than it's above immediate comparator's reference voltage. Comparison among input, ref voltages is done here. If input is higher than reference, 1 is produced at output. If inputs less than reference, 0 is produced. Input analog information is somewhere in between Vx4 and Vx5, then comparators X1 through X4 output setup output as high(1) and the other remaining comparator outputs generates as 0.For input signal, its equitant thermometer code is generated by comparator. In mercury thermometer, as the mercury always rises to the appropriate temperature in the mercury column, the thermometer code encoded into stream of bits by thermometer-to-binary encoder. At high frequency, these typically offer low gain, it becomes quite difficult. The new design is offering low offset voltage; input offset of every comparator is less than ±1LSB of the converter. If not, the comparator offset may treat its output as wrong. In such case, digital code will not be equilant with thermometer code. Each comparator is included with regenerative latch where output result can be stored. While positive feedback, the end state is compulsory to be any one of logic '1' or logic '0'.

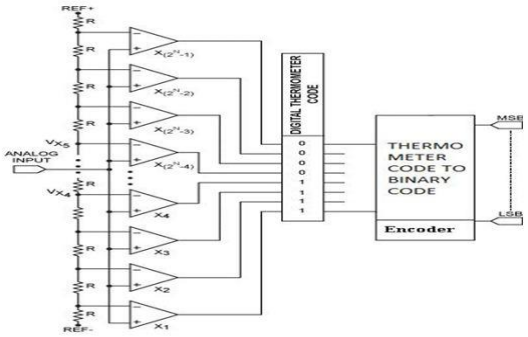

Fig. 1. Block diagram of flash ADC

IV. CMOS FLASH TYPE ADC

Flash ADC with array of comparators, comparison is done between input voltages with a large collection of accelerating V_{ref}. The comparators turnout unambiguously represents the input in an exceedingly measurable thermometer code, which is converted into binary format. In general, flash ADC contains two important blocks namely TIQ comparator and an encoder.

A. TIQ Comparator Block

TIQ comparator comprises of two cascaded inverters. CMOS is preferred here as it shows its best low power dissipation with considerable high speed. The comparator plays a crucial role in ADC architecture design. Its task is to assign the input voltage 'Vin' to any one of logic '1' or logic '0',in comparison with fixed reference voltage. If V_{in} is higher than V_{ref}, then the output is assumed as `1'.if V_{in} is lesser, then output is assumed as '0'. Differential latch and dynamic comparator structures are used in ADC CMOS architectures in general. At the earliest it was termed as clocked comparator and latter it termed an chopper comparator. To work at high speeds, such comparators area unit sometimes enforced with bipolar semiconductor device technology. For SoC implementation, Bi-CMOS technology is necessary for integrating both high speed and a digital signal method on constant substrate.TIQ comparator was designed with cascading of CMOS inverters, which works as comparator for prime speed along with needy low power consumption. Many researchers have used this TIQ comparator in high speed flash ADCs. The proposed TIQ comparator is developed not only for higher speed but also for higher resolution.

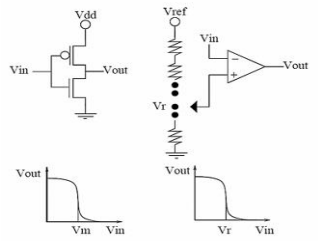

Fig. 2. CMOS inverter used as a comparator

In Fig. 2 the comparison of differential voltage signals along with inverter based comparator with respect to similarities and differences. CMOS inverter is a very basic and simplest possible circuit which can be replaced by resistor ladder and differential input voltage comparator. The inverter circuit works at high speed in comparison with differential input voltage comparator network. The benefits of CMOS inverter are:

1. Its Steady state power dissipation is very little.
2. VTC exhibits full dynamic range between 0 to V_{DD}.
3. The VTC transition has very sharp cutting edge.

In a normal Flash ADC, many voltage comparators are connected in parallel and the ref voltage V_r is established at nodes by the massive resistor ladder network. This TIQ technique avails a digital inverter that acts as voltage comparator. Due to this, switching threshold V_m is internal to the inverter, its value dependent on transistor size. The switching threshold voltage of inverter V_m is noted at V_{in} = V_{out} intersection on VI curve as shown in Fig. 3.It is the point of intersection as shown

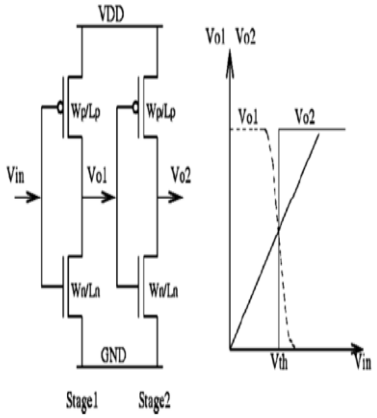

Fig. 3. Cascade of 2 inverters as a TIQ

B. Comparator and its VTC Characteristics

Designing of comparator is quite difficult. However, many researchers and engineers have done a great job in designing and redesigning many times in spite of using the Modern CAD tools in VLSI. The TIQ approach with lot of benefits such as simple, faster, avoiding resistor ladder, highly convenient and best suited for the standard CMOS technology at lower supply voltage without need of switches, clock signal, coupling capacitors, etc. The switching threshold, V_m is noted at the point,V_{in} = V_{out} on VI characteristics of an inverter mathematically,

$$V_m = \frac{r\,(V_{DD} - |V_{Tp}|) + V_{Tn}}{1+r} \text{ with } r = \sqrt{\frac{k_p}{k_n}} \quad (1)$$

Where V_{Tp}, V_{Tn} are thresholds of PMOS, NMOS respectively. At the first inverter, quantization level of analog input is set by V_m ,which depends on the PMOS and NMOS 'W/L' ratios. Voltage gain is increased by the second inverter and it helps to reduce the propagation delay. In Fig. 3, the slope of V_{out} is represented higher than one of V_{out1}. The value of threshold varies depending on transistor sizes. On the inverter VTC plot V_a and V_b indicates the variation from the VTC of V_{out}. Thus required values of V_a and V_b can be possible by enhancing the PMOS and NMOS widths respectively. The result can be affirmed by using the inverter threshold mathematical statement

$$V_m = \frac{\sqrt{\frac{\mu_p W_p}{\mu_n W_n}}\,(V_{DD} - |V_{Tp}|) + V_{Tn}}{1 + \sqrt{\frac{\mu_p W_p}{\mu_n W_n}}} \quad (2)$$

Where μ_p,μ_n are the motilities of positive and negative charge respectively. Making an assumption that both transistors are working in active region, thickness of the gate oxide (Cox), the lengths of two transistors (L_p and L_n) for both transistors are same. On observation on above equation, V_m is shifted depending the ratio of transistor widths (W_p/W_n). Hence,raise in W_p(width of PMOS) makes V_m(switching voltage) larger, and increasing W_n (width of NMOS)results in V_m (switching voltage) goes smaller on the VTC. The variation of different switching voltages along with different PMOS widths is given in Table I.

For designing fifteen number of TIQ comparators which uses different widths of the PMOS, NMOS having fixed length transistors. However, chain of CMOS inverters are used for comparing the voltage signals, by verifying the V_m sensitivity with respect to other parameters of the TIQ flash ADC.

Table-I: Switching Voltages For Different PMOS Widths

TIQ No.	W_p(µm)	W_n(µm)	V_m(switching voltage)(V)
1	0.17	0.17	2.039
2	0.24	0.17	2.212
3	0.34	0.17	2.390
4	0.48	0.17	2.574
5	0.68	0.17	2.755
6	0.96	0.17	2.940
7	1.35	0.17	3.104
8	1.92	0.17	3.271
9	2.75	0.17	3.432
10	3.51	0.17	3.534
11	5.45	0.17	3.705
12	7.61	0.17	3.822
13	10.75	0.17	3.931
14	15.17	0.17	4.021
15	21.42	0.17	4.113

C. Multiplexer based Encoder

An encoder is a device that converts information from one coded information to another for purpose of standardization, speed or compressions. A simple encoder gives a binary output coded value to an active input line. For an ADC the encoder circuit will express thermometer code in terms of binary code. The design of Thermometer to binary encoder can be done using different techniques like Fat tree, ROM type, logic based, multiplexer based. Out of variety of encoders, multiplexer based encoder takes less hardware, least critical path.

Fig. 4 shows the design of 2x1 MUX using transmission gate logic.

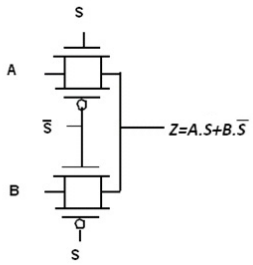

Fig. 4. Transmission Gate based 2*1 Multiplexer

Multiplexer, one of the circuits that give single output as per accordance to multiple inputs. Here, 2*1 multiplexer based encoder is used and the functionality is given in Table II. The multiplexers here are designed using transmission gates for better accuracy. A 2*1 multiplexer is the circuit which having 2 input lines and one output line with single select line.

Generation of binary code from thermometer code is one amongst the most style problems with any flash ADC encoder. So many ways exists for this conversion.

a) Indirect conversion

One additional intermediate stage is needed here, which might modify the parameters like enhancement in power, current dissipation, propagation delay etc.

Table-II: Truth Table Of 2*1 Multiplexer

Input A	Input B	Selection S	Output Z
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

b) Direct Conversion

In this methodology, truth table is used to write the logic expressions of thermo-meter code in terms of binary code. This technique is efficient in terms of the parameters like reduction in power dissipation, propagation delay etc. The truth III table shows expressing thermometer code in terms of binary code. The comparators output is in the form of Thermometer code. So, encoder is required here to express the thermometer code in terms of binary code. The principle of this code converter is given follows The Thermometer code input, T8 is directly equal to G_3(Gray code). So B_4 is written as directly T8. For getting G_2, the T12 input assumed as one select line of 01 logic cell of multiplexer. T4 is attached at input '0' of 0 logic cell and input '1' is grounded. For G_1, T14 assumed as select line for 02 logic cell of multiplexer and for 03 logic cell of multiplexer, T6 acts as select line.

When T6 is '0', T2 is directly equal to G_1. As soon as T6 is '1', 02 logic cell output is selected. Considering 02 logic cell, when '0' is observed on select line, then T10 is picked up for G_1. For T14 equal to '1', G_1 is '0' so 02 logic cell input is grounded. To get G_0, allot T13 to input '0' and allot input '1' of 04 logic cell of multiplexer to ground by assuming select line with T15.04 logic cell output is given to input '1' of 05 logic cell and T9 to input '0' by taking T11 as select line. The output of 05 logic cell is given to input '1' of 06 logic cell and T5 to input '0' by taking select line as T7. The output of 06 logic cell is attached to input '1' of 07 logic cell of multiplexer and T1 is attached to input '0' by select line is assumed as T3.G_0 is collected at the output of 07 logic cell. Here, the concept of grounding reduces the hardware, such that there is a great reduction in overall power consumption. The multiplexer based encoder circuit is given in Fig. 5.

Table-III: Function Table Of Thermo-meter Code into Binary

T15	T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	B4	B3	B2	B1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1
1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	0
1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	1	1	1
1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	0	0	0
1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	0	0	1
1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0	1	0
1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	1	0	1	1
1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	1	1	0	0
1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

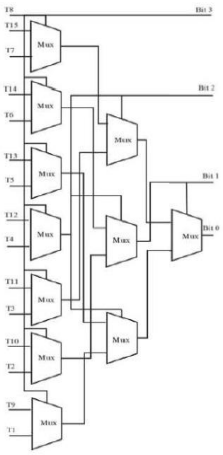

Fig. 5. Multiplexer based Encoder

The Boolean expressions can be observed here are

$$G_3 = T_8$$
$$G_2 = T_4\bar{T}_{12}$$
$$G_1 = T_2\bar{T}_6+(T_{10}\bar{T}_{14})T_6$$
$$G_0 = T_1\bar{T}_3+(T_5\bar{T}_7+(T_9\bar{T}_{11}+(T_{13}\bar{T}_{15})T_{11})T_7)T_3 \quad (3)$$

Then, the code conversion from gray to binary requires an XOR gate as follows

$B_4=G_3$ (4)
B_3=XOR of (B3, G2) (5)
B_2=XOR of (B2, G1) (6)
B_1=XOR of (B1, G0) (7)

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V. RESULTS

Fig. 6. shows RTL schematic of 4-Bit ADC with input port as "a" and output port as numbered from B_1 to B_4 .The combination of TIQ Block with Comparator Block results in 4 Bit Flash ADC Architecture with necessary connections and applied analog signal to port "a" with frequency of 1MHz and V_{hi}=1.2V,V_{lo}=0V.

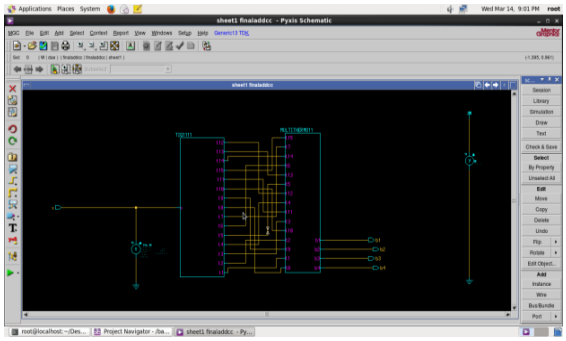

Fig. 6. RTL design for Flash ADC (4 bit)

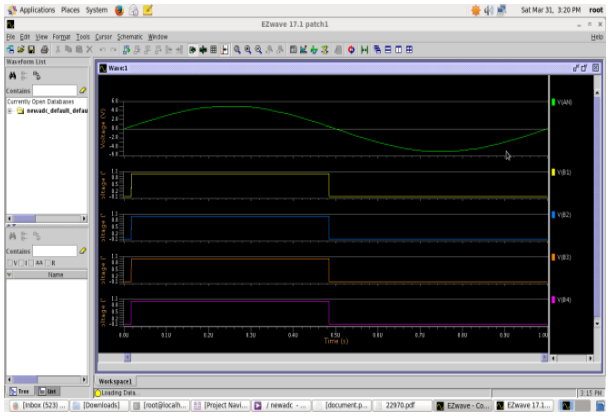

Fig. 7. Simulation Waveform of 4 Bit Flash ADC

In Fig. 7 the simulation waveforms of four bit Flash ADC are shown with the analog input voltage signal, V_a with frequency 1MHz and corresponding output binary values are plotted.

Table-IV: Power Analysis Report Of 4 Bit Flash Adc

Digital outputs	*Max (V)*	*Min (V)*	*P-P(V)*	*Avg(uV)*
Analog input	5	-5	10	225.15
B_1	1	-74.8	1.0001	467.26
B_2	1	-91.52	1.0001	467.26
B_3	1.0027	-600.9	1.0023	467.27
B_4	1.035	-905.2	1.023	467.27

Here a simple and fast 4-bit flash ADC architecture has been implemented with new comparator style that uses two cascaded inverters and multiplexer based encoder. Flash ADC achieves higher data sampling rate and operates at low voltage with low power consumption. All the simulations are carried out by MENTOR GRAPHICS TOOL with 130nm process technology. A viable attempt is made and achieved by designing low power Flash ADC using CMOS logic structures. In this work, the results are given in Table IV and V respectively and achieved the power dissipation of 0.833 µW and delay is obtained of 15.393nsec. The design and simulation of different blocks along with integration of Flash ADC has completed here with supply voltage 1.2V using 130nm CMOS technology.

Table-V: Comparison Of Various Parameters For Four Bit Adc With Mux Based Encoder

Parameter	*Reference1*	*Reference2*	*MUX based Encoder*
Technology (nm)	90	130	130
Sampling Frequency (GHz)	5	1	1
VDD(V)	1.2	1.2	1.2
Delay (ns)	9.29	9.29	15.393
Power Dissipation (µW)	184.8	1.833	0.833

VI. CONCLUSION AND FUTURE WORK

The power consumption by encoder block within the flash ADC is very large. To minimize such amount of power mux based encoder is used along with cascaded inverters as a comparator in this work. Functionality of encoder and TIQ was verified using MENTOR GRAPHICS tool. Further, it was observed that, in many flash ADCs of 4 bit, the dissipation of power is higher when compared with designed ADC. This encoder which operates at 1GHz consumes 0.382µW at 1.2 V voltage source. In future, the Flash ADC must excel with planning of a greater speed high exactness by reducing size of CMOS comparator, Flash ADC operating at faster rate, low offset comparator, Flash ADC with low power.

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