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Stacking Techniquefor Low Power Sram

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Abstract*: Static random access memory leakage current is becoming one of the critical issues for low-power systems. SRAM-based FinFET Double Gate has become a better option for profound submicron techniques owing to its better short channel effect. In this work, we review some of the leakage current sources and low power reduction technique to reduce leakage. As animprovement of our research work,6T SRAM memory cells can be implemented using independent gate FinFET which gives lower leakage as well as better performance over the shorted gate FinFET mode. This is also implemented using stacking technique to decrease leakage. Therefore, the power devoured by the different SRAM cells is likened with the Tanner tool in 45 nm technique.

***Keywords*: Fin FETs, High-performance, Short channel effects (SCEs), Low power (LP) mode, Independent gate (IG) mode, Shorted gate (SG) mode.**

I. INTRODUCTION

One of the most significant problems commonly faced by CMOS circuit design is the decrease of energy usage. The supply voltage is reduced to decrease the power consumption. While lowering the supply voltage may seem a good idea but it increases the gate delay which further reduces the operating frequency. A big demand in sub-micron CMOS technology is For highly dense circuits and their dependence on leakage current due to the density of the oxide and the required voltage.There is an increase in the leakage currents during technology scaling. Under OFF state, a smallsub threshold leakage currentflows from the drain to source terminals.When Innovation synergizes, the capacitor baseline voltage reduces, and the leakage current rises.. Similarly,as the current flows from the gate to the substrate through the gate oxide, gate leakage current is caused. The transistor leakage current of the door rises. as the over the linear region of the transistor decrease. [1]The proposed SRAMs are designed by using DG MOSFETs. This has lower SCE, leakage power and leakage currentthan bulk CMOS. To achieve higher integration, lower current and less leakage DG MOSFETS are used to design.[2] As technology scales down to the nanometer region supply voltage must be minimized to maintain the dynamic voltage at reasonable level. Whenever power consumption increases, leakage also get incremented. This papers deals with the reduction of power in 6T SRAM using FinFET. FinFETs are more compatible over the CMOS process. FinFET channels are perpendicular to the substrate so that it increases the electrostatic control of the gate to achieve less SCE. It has excellent scalability, low leakage and parametric variation. In FinFET the second gates are just opposite to the first gate. There are two types of FinFETs.. In tied gate FinFET ,opposite The doors are linked together and work like a normal three terminal device and in independent mode both gates are biased independently. This improves the performanceandalsoreduces the leakage . Memory plays a vital role in the chip area of microprocessor. Due to large size memory it increases the power consumption in the circuit. SRAM cell scalability is achieved by using supply voltage and threshold voltage scaling. FinFET technology can be used to increase the data stability in SRAM. For nanoscale memory circuit design FinFET is highly desirable to reduce SCE and leakage.[3]

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II. DIFFERENT TYPES OF FINFET MODES

FinFET s can be the replacement for bulk CMOS technology. Its low leakage and SCE effects make FinFETs a desirable option for memory system. Memory modules are most important for digital and computer system. The main drawback of memory cell is high leakage. Clock network consumes more power than others. FinFET provides less leakage and it offers better control over the channel.
There are four types of FinFET modes, namely Shorted gate mode, Independent gate, hybrid mode and low power mode. In shorted gate mode,the two sides areshorted together so it looks like a terminal device, provides better control over the channel but gives higher leakage. Next independent gate mode both gates are biased independently so that it increases the gate control also reduces the leakage. In low power mode higher threshold voltage is given to pmosand lower threshold is applied to the nmos transistor due to this variation in voltage minimum leakage is achieved but it gives mismatch delay in the circuit. Hybrid mode is a combination of both independent and low power mode.[4]The inverter schematic model is shown in fig.1 in shorted gate mode inverter both transistors back gates are connected to its front gate.In independent gate inverter n gates back gate is connected to front gate and p gates are biased at high voltage. This reduces number of transistor and switch capacitance in the circuit. In low power mode back gates are biased at high voltage and n type back gates are biased at low voltage. This is important for low power application also increases the delay. Hybrid mode provides low leakage and low switching capacitance.

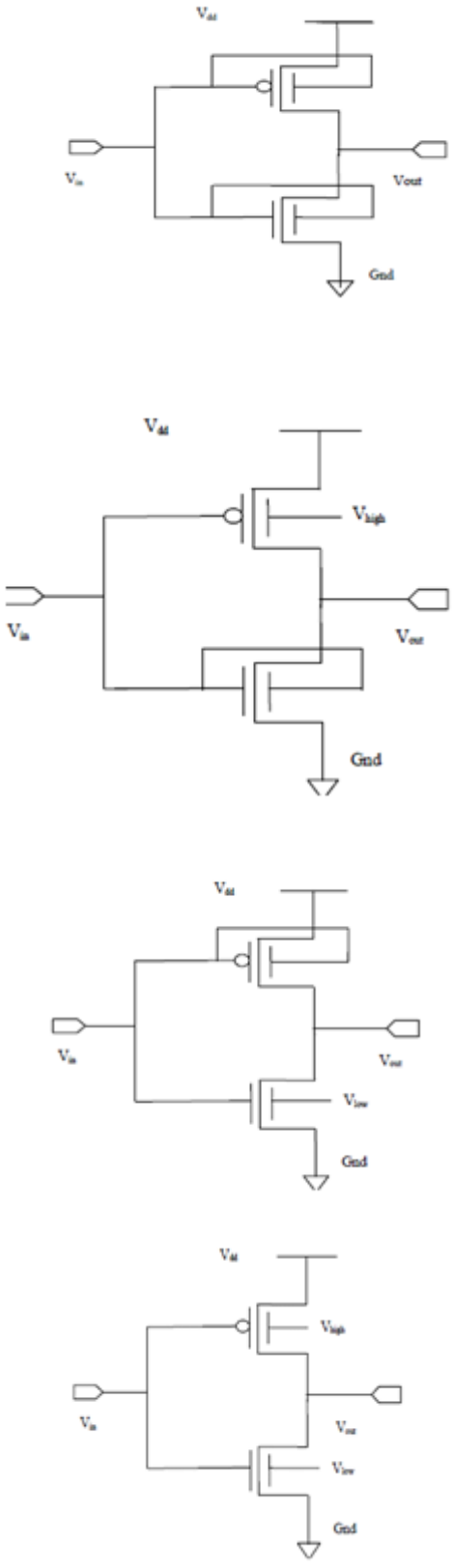

Fig.1 (a) SG mode (b) Independent Mode (c) Low power mode (d) Hybrid

III. DIFFERENT SOURCES OF LEAKAGE

Junction Leakage :Junction leakage is mainly occurs in the source or drain to the substrate ,when the transistor is not in use. OFF nmos transistor drain to substrate voltage is equal to supply voltage. This increases the leakage in the substrate through reverse bias diode. Junction leakage is mainly influenced by the doping concentration. It highly depends on temperature.[5]

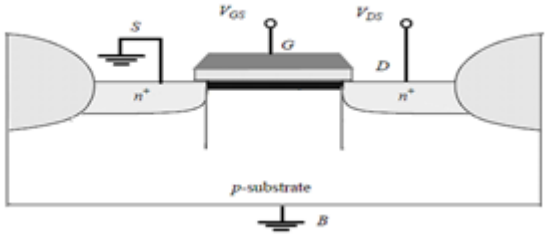

Fig. 2 Sources of Leakage

A.Drain Leakage Induced Gate:

It is triggered by a elevated field effect at the MOSFET transistor drain intersection. The VDD and the parked gate are connected to the nmos transistor drain. Deep degradation occurs when the holes are cleared to the substrate at the same moment that electrons are collected at the drain coming from the GIDL current. Crossing doping is extended while the channel doping is small. This is mostly due to DIBL and punching out while having reduced plane stability in the stream. The GIDL new extends with more thin gate oxide and greater supply voltage.[6]

B.Gate Direct tunnel leakage:

Maintaining good aspect ratio is very challenging parameter is technology scaling. Minimizations of vertical dimensions are harder than horizontal dimension with the silicon scaling. The position of the inversion layer in the silicon substrate for a transistor with a typical bias is 1 nm from the gate oxide and channel interface, taking into consideration the quantum mechanical effects. As a result, The efficient density of the oxide rises by 0.3 nm. In view of the charge scattered on each side of the layout, the 1 nm oxide bridge is limited to an efficient oxide density of 1,7 nm.[7]

C.Sub-threshold leakage:

The subthreshold leakage current streams from drain to source when entry to cause energy is not exactly the threshold voltage. The transistor is worked in week inversion mode. In strong inversion drift current is dominant, subthreshold current acts as the dispersal current of the smaller movers. For instance while low input is connected nmos is OFF and pmos is ON and the voltage is high. The gate to source voltage is zero yet at the same time a current is flowing in OFF nmos due supply voltage potential of the channel to source voltage.[8]

IV. PROPOSED INDEPENDENT GATE 6T SRAM WITH STACKING TECHNIQUE

The proposed independent gate 6T SRAM opposite gates are biased independently. It is modelled to reduce outflow current and increases the presentation of the circuit. Fin has minimum width. SRAM has three modes of process namely standby mode, read mode and write mode. in standby mode both bit line lines are detached from the power supply and remains in the same state as long as linked to the power source. For the read procedure, the term line is kept high and the bit rows are preloaded.

Vdd. Node Q stores 0 and BL is discharged through nmos transistors. The access transistor act as high threshold voltage device with weaker conducting current to tied gate SRAM. During write 0 operation the node BL gets discharged and BLS is charged . In this approach leakage current is measured which very lower when compare to convention 6T SRAM. The 1 bit SRAM cell is designed by using 45nm. The parameters will change depends on the nano meter technology.[9]

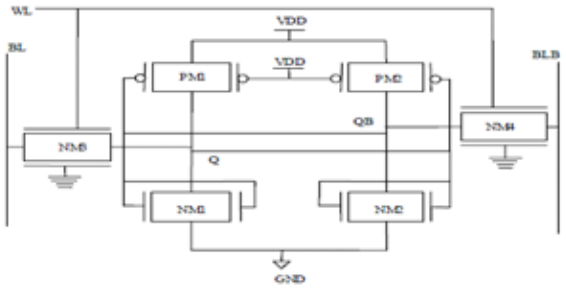

Fig. 3 Independent 6T SRAM design

D.Independent gate Stacking 6T SRAM

In modified SRAM cell ,the transistor M4, M10, M6, M8 forms the cross coupled inverter. The primary methodology of the proposed framework is to diminish the leakage current in the SRAM cell. At the point when more than one transistor between power supply to the ground has less leakage than one and only transistor in any power supply to the ground way. Leakage control transistor is embedded in close to the cut off area. Two leakagenmos and pmos are embedded between pull up and pull down transistor. The drain nodes are associated together to frame the output node of inverter. The source nodes are associated with the pull up and pull down logic separately. Switching is controlled by voltage potential. Leakage control transistor is associated with the cut off region.[11-16]

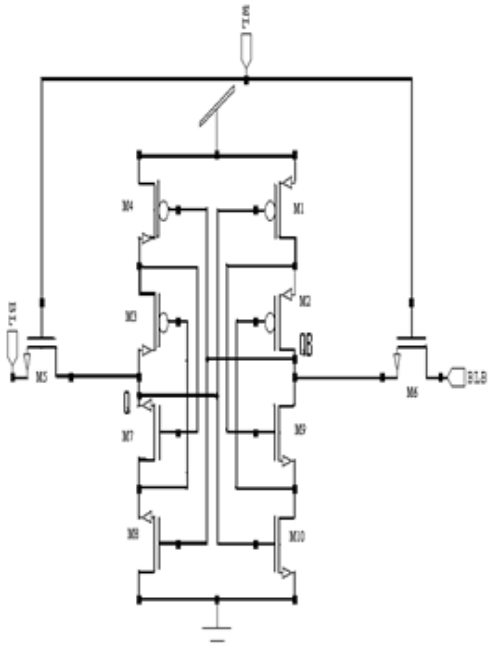

Fig. 4 Independent gate stacking 6T SRAM

V. SIMULATION RESULTS

In this paper, 6T SRAM cells are structured using two different technique, SRAMs are previously designed using tied gate FinFET and next one is Independent gate FinFET. In conventional 6T SRAM both pmos and nmos gates are shorted together but it gives higher leakage. Here 45nm FinFET technology is used. TSPICE using PTM model is appliedfor simulation of the shorted and independent 6T SRAM and the results are compared. Fig.5 shows the simulation structure of convention 6T SRAM cell. Its simulation graph is given in Fig.6 here both the BL and BLB are in opposite sign and BL follows the WL also the power measurement is shown simulation result.[10]

Fig.7 shows the simulation output and leakage current characteristics of stacking FinFET SRAM cell and simulation graph of the same is shown in fig.8[17-20]

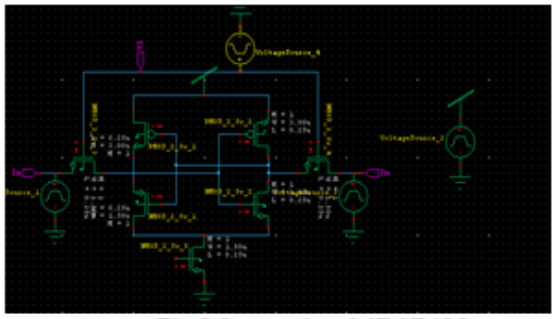

Fig.5 Conventional 6T SRAM

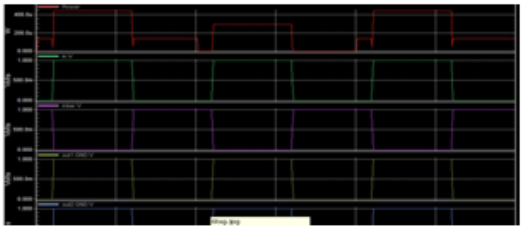

Fig.6 Simulation graph of convention 6T SRAM

Table.1 shows the comparison result of conventional and proposed technique. Power and delay measurement of conventional FinFET SRAM and Independent 6T SRAM are shown. Independent with stacking gives better control to the gate so that power consumption is reduced but delay is increased.

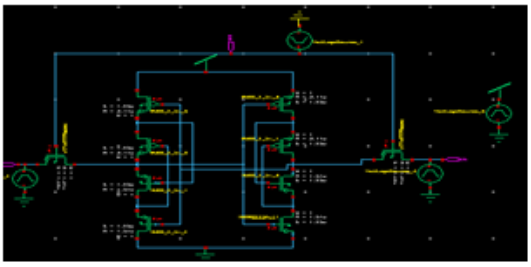

Fig.7 independent gate with stacking technique

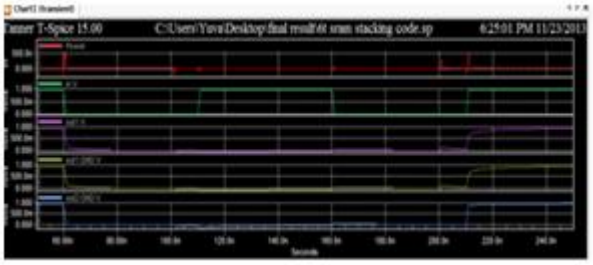

Fig.8 Simulation graph

Table.1 Comparison of technique

S.NO	Techniques	Power
1	Conventional 6T SRAM	2.616419e-014
2	FinFET6T SRAM	8.473101e-015
3	FinFET 6T SRAM using Stacking technique	2.339218e-19

VI. CONCLUSION

In this paper, FinFET SRAM have been examined as far as the leakage–delay tradeoff, and contrasted with bulk circuits. Low-power buffing and robust 6 T SRAM cells, taking into consideration FinFET, have been suggested in this job.. The planned stacking expands the resistance between power supply to the ground with the goal that it minimizes the leakage in 6T SRAM chamber. The TSPICE models for the 45 nm techniques were used to determine the effectiveness of the cells. In comparison to previous normal CMOS SRAM work, the suggested scheme had a low energy utilization rate and read entry time with a better static Noise Margin.

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