International Journal of Engineering and Advanced Technology (IJEAT)
ISSN: 2249-8958 (Online), Volume-8 Issue-6S2, August 2019

BIST for Reconfigurable System on Chip (SOC) for Micro-Vibration Measurement

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Abstract*: This paper presents methodology for testing mixed signal circuits in the SOC configured for micro vibration measurement. The SOC for micro vibration measurement contains a Bi morph sensor and front end electronics containing an amplifier, peak detector interface with A/D converter and memory. The amplifier is tested by applying triangular stimuli input generated by Test Pattern Generator (TPG) configured in the FPGA. The peak detector is tested by applying a test pulses generated by test generator system. The outputs of the test circuit are analyzed by output response analyzer (ORA) in the FPGA. The required hardware for testing analog as well as digital circuits of the SOC are configured by the on chip portion of FPGA and FPAA. The whole SOC can be tested by applying stimuli generated in TPG and checking the output by comparing patterns stored in memory with reference pattern using ORA. Simulation results are reported for counter and test ADC.

***Keywords* : Output response analyzer, Test pattern generator, SoC and FPAA..**

I. INTRODUCTION

Testing is an important activity at different levels to validate a design. In normal case the complete testing of a mixed signal integrated circuit occupies a large area and power. A mixed signal circuit needs analog as well as digital stimuli to test its different portion. There are various approaches for testing mixed signal circuits. The faults occurring in analog circuits can be categorized as hard faults and soft faults. The hard faults
(Catastrophic) are those which categorize circuit performance to differ catastrophically different than normal performance [1,2]. A catastrophic fault is similar to stuck at fault in digital test domain where every component can either stuck open are stuck short. A stuck fault occurs when component output is not connected to rest of the circuit. The stuck short fault occurs when component output is shorted. The soft fault refers to changes in a circuit that do not affect it connectivity but results in circuit function out of specification. The important test approaches is based on oscillation built in self test. In this type of test circuit is converted in to an oscillator and its parameter like oscillation frequency is determined. These parameters are compared with parameter of simulated test circuit and suitability of a circuit under test is determined. For this the fault is injected in the circuit under test and testing can be done for all types of faults. In our work a reconfigurable system on chip (shown in figure 1) has been simulated by configuring digital portion in FPGA and analog portion in FPAA. Implementation on FPGA and FPAA is done for rapid proto typing and in future, one can get ASIC fabricated for this system. The amplifier and peak detector and other analog circuits are tested by applying test stimuli generated by TPG and the output of Device Under Test (DUT) is analyzed by Output Response Analyzer (ORA). The whole BIST hardware is configured on existing FPGA and FPAA resources available on SOC. The section II presents BIST architecture and operation. The detailed descriptions of test pattern generator (TPG) and ORA are given in section III and IV. Section V reports simulation results for testing different parts of SOC. Section VI presents conclusion.

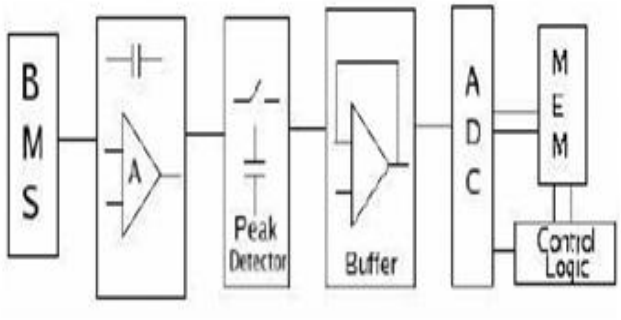

Fig 1 Vibration monitoring Reconfigurable SOC.

II. BIST ARCHITECTURE AND OPERATION

Following portion discusses the BIST configuration for various part of the SOC.

A.BIST Configuration for Peak Detector

For detection of fault in capacitor, we are proposing a system consist of a constant current source, a switch to control the charging of the capacitor, comparator which will compare the results stored in ROM, and using ADC of the SOC. The sequence of test is as follows:

1. A defined period of the pulse is applied, so that, capacitor will get charged to known voltage, which will be converted to digital through ADC and the value is analyzed by ORA from the value stored in ROM as shown in figure 2.

Manuscript published on 30 August 2019.
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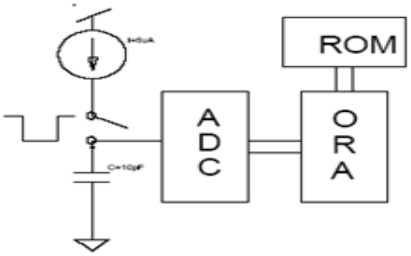

Fig 2.Test Configuration of Peak Detector.

2. The catastrophic faults are also tested from the proposed test structure, if the capacitor is shorted then ADC output will be zero, and if capacitor is open then, ADC output will show a fixed value despite of any period of the applied pulse.

B. BIST Configuration for Amplifier

For analyzing amplifier, a triangular waveform is generated using test pattern generator and applied to the DUT (configured as amplifier), and the output of DUT is then fed to ADC and output of ADC is analyzed using ORA with delayed value of test pattern generator. In case of any discrepancies in these outputs, the ORA will signal the fault condition. BIST configuration of amplifier is shown in figure 3.[6-10]

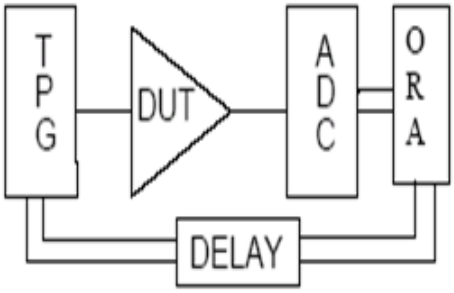

Fig 3 BIST configuration for Amplifier

C. BIST Configuration for Complete system

In order to test the complete SOC, the different stimuli is generated to simulate various vibration signal using Test Pattern Generator (TPG) containing linear feedback shift register and counter, the output of Linear Feedback Shift Register (LFSR) is fed to DAC and Low Pass Filter (LPF) to generate required stimuli. The output of test pattern generator is applied to DUT to monitor the fault condition by using ORA as shown in figure 4.[11]

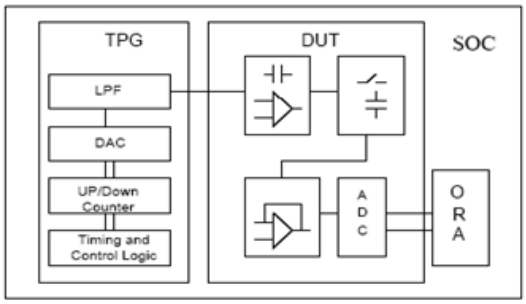

Fig.4 BIST Configuration of Complete System.

III. TEST PATTERN GENERATOR

The test pattern generator consists of up/down counter with its output fed to digital to analog converter. The analog output of DAC is filtered by using a low pass filter. The low pass filter is configured using a CAB of FPAA. The up/down counter and its timing and control logic is configured using FPGA as shown in figure 5[17-20]

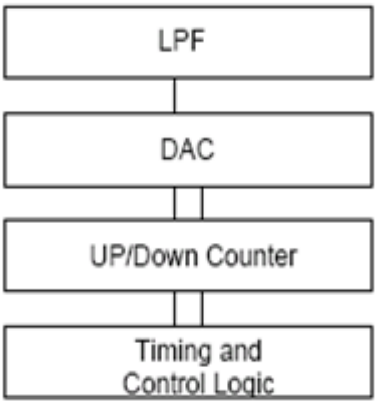

Fig.5 Test Patern Generator.

IV. OUTPUT RESPONSE ANALYZER (ORA)

The ORA analyzes the output of the ADC from the value code generated from TPG by subtracting them. The accumulator in the ORA determines the pass/fail status of the BIST by expecting the final sum to be within a predetermine range of values [3]. One of the advantages of digital ORA is that, the results can be directly read from the system digital interfaces during system level testing. The size of the double precision accumulator should at least 16 bits when ADC and DAC are less then 8 bits. The figure 6 shows the configuration of ORA.

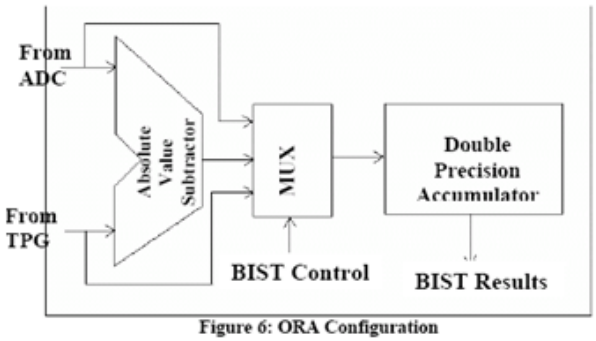

Figure 6: ORA Configuration

Fig.6 ORA Configuration.

IV. SIMULATION RESULTS

A 10 bit counter is designed as a part of test pattern generator and is operated in up counting mode. Figure 7 shows 10 bit outputs of this counter. This counter will be used to generate test stimuli for testing different part of test system

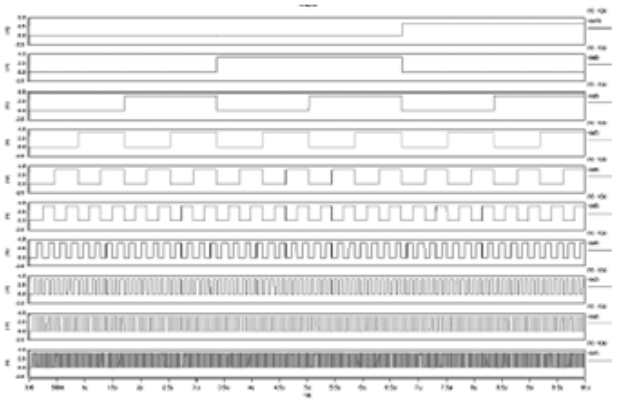

Fig.7 Plots of output10 Bit Counter.

A 7 bit ADC is designed and a simulated test pattern which is shown on the top of figure 8 is applied at the input of this ADC. The 7 bit outputs of ADC are shown in figure 8 in response to this stimulus.

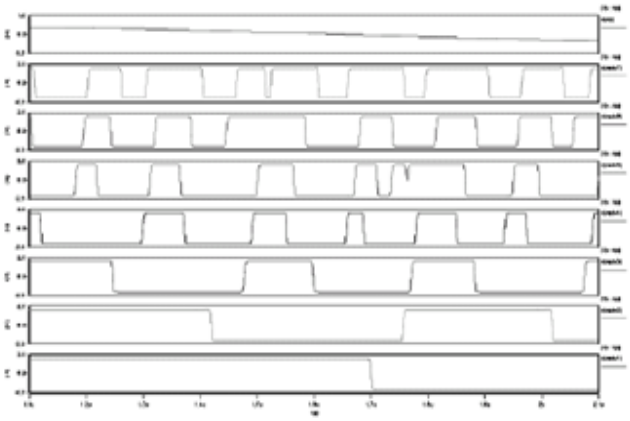

Figure 8: Plot of output of 7bit ADC in response to Test Stimuli

Fig.8 Plot of output of 7 bit ADC IN response to Test Stimuli.

VI.CONCLUSION

The BIST architecture for different portion of vibration monitoring system is discussed in the paper. With the help of this arrangement stuck open and stuck short fault in different part of the system can be detected. Simulations of different faults in the test circuit are done by injecting faults. The stimuli required for testing are generated using TPG, which in turn generates different arbitrarily signals using counter and LFSR. The ORA analyzes the responses from ADC and TPG in the digital domain and generates the pass/fail status signal about the test circuit.

REFERENCES

1. Kongkham, D. & Sundararajan, M. 2019, "Distributed wideband sensing method for faded dynamic spectrum access", International Journal of Innovative Technology and Exploring Engineering, vol. 8, no. 10, pp. 4309-4312.
2. Balaji, S., John Paul Praveen, A. & Mohanraj, R. 2019, "Recognizable proof and analysis of palm print in biometric authentication system using bayes techniques", International Journal of Innovative Technology and Exploring Engineering, vol. 8, no. 9 Special Issue 3, pp. 1126-1129.
3. Kavitha, G., Priya, N., Velvizhi, R. & Allin Geo, A.V. 2019, "Parallel computation in correspondence and signal processing", International Journal of Innovative Technology and Exploring Engineering, vol. 8, no. 9 Special Issue 3, pp. 1136-1139.
4. Hema, R., Sundararajan, M. & Balaji, S. 2019, "Smartphone control robot with automatic firing gun", International Journal of Innovative Technology and Exploring Engineering, vol. 8, no. 9 Special Issue 3, pp. 625-627.
5. Kaliyamurthie, K.P., Sundar Raj, B., Velvizhi, R. & Shanmugapriya, K. 2019, "Dual band paper substrate CPW antenna for wireless applications", International Journal of Innovative Technology and Exploring Engineering, vol. 8, no. 9 Special Issue 3, pp. 605-608.
6. Geo, A.V.A., Arunachalam, A.R., Michael, G. & Elankavi, R. 2019, "Evaluating architecture using compact modalities", International Journal of Innovative Technology and Exploring Engineering, vol. 8, no. 9 Special Issue 3, pp. 836-838.
7. Theivasigamani, S., Jeyapriya, D. & Anita Davamani, K. 2019, "Anamoly analyzing and exploring for wireless sensor networks", International Journal of Innovative Technology and Exploring Engineering, vol. 8, no. 9 Special Issue 3, pp. 1116-1118.
8. Jeyapriya, D., Theivasigamani, S., Velvizhi, R. & Nandhini, P. 2019, "Program detection in wireless feeler networks", International Journal of Innovative Technology and Exploring Engineering, vol. 8, no. 9 Special Issue 3, pp. 1194-1195.
9. Gowri Sankaran, B., Karthik, B. & Vijayaragavan, S.P. 2019, "Image compression utilizing wavelet transform", International Journal of Innovative Technology and Exploring Engineering, vol. 8, no. 10, pp. 4305-4308.
10. Gowri Sankaran, B., Karthik, B. & Vijayaragavan, S.P. 2019, "Weight ward change region plummeting change for square based image huffman coding", International Journal of Innovative Technology and Exploring Engineering, vol. 8, no. 10, pp. 4313-4316.
11. Hema, R., Sundararajan, M. & Balaji, S. 2019, "Smartphone control robot with automatic firing gun", International Journal of Innovative Technology and Exploring Engineering, vol. 8, no. 9 Special Issue 3, pp. 625-627.
12. Rangaswamy, K. & Rajabhushanam, C. 2019, "Congestion control in wireless network using TCP friendly rate control (TFRC)", International Journal of Recent Technology and Engineering, vol. 8, no. 2 Special issue 3, pp. 1598-1602.
13. Tamil Selvan, S. & Sundararajan, M. 2019, "Performance Parameters of 3 Value 8t Cntfet Based Sram Cell Design Using H-Spice", International Journal of Recent Technology and Engineering, vol. 8, no. 2 Special issue 5, pp. 22-27.
14. Vinoth, V.V. & Kanniga, E. 2019, "Steganographical techniques in hiding text images – system", International Journal of Recent Technology and Engineering, vol. 8, no. 2, pp. 6535-6537.
15. Saravana, S., Balaji, S., Arulselvi, S. & John Paul Praveen, A. 2019, "Reliable power quality monitoring and protection system", International Journal of Innovative Technology and Exploring Engineering, vol. 8, no. 9 Special Issue 3, pp. 644-645.
16. Sundaramoorthy, A. & John Wiselin, M.C. 2019, "Single patch antenna with multiple feed", International Journal of Innovative Technology and Exploring Engineering, vol. 8, no. 9, pp. 1743-1747.
17. Velavan, R., Bharanidharan, S. & Sheeba, B. 2019, "EMF pollution - Causes, effects and protection", International Journal of Innovative Technology and Exploring Engineering, vol. 8, no. 9 Special Issue 3, pp. 1166-1168.
18. Veer, R.A., Arulselvi, S. & Karthik, B. 2019, "Construction of ensemble square classification approaches in MIMO OFDM", International Journal of Engineering and Advanced Technology, vol. 8, no. 5, pp. 2039-2041.
19. Agitha, W. & Kaliyamurthie, K.P. 2019, "Improved energy efficient in WBAN using MAC with cloud computing", International Journal of Innovative Technology and Exploring Engineering, vol. 8, no. 8, pp. 2405-2408.
20. Kastro, G.G. & Wiselin, M.C.J. 2019, "Design and analysis of stub loaded resonator", International Journal of Recent Technology and Engineering, vol. 8, no. 1 Special Issue4, pp. 272-283.

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