Superscalar Pipelined Matrix Multiplier in VHDL

S. Arulselvi, S. Balaji, R. Hema

Abstract*: Parallel processing is used by simultaneous information processing to boost the computing velocity of the computer system. Parallel processing is implemented by pipeline processing.. In this paper we presented design of a A[100][100] x B[100][100] Pipelined Matrix Multiplier and its results is stored in P[100][100] matrix. We present design and stimulate a functional Pipelined Matrix Multiplier Unit. By which we can learn about the working of Pipelined Matrix Multiplier and how pipelining works. We also get the knowledge of clock timing and learn to make a timing critical design. In this Pipelined Matrix Multiplier Unit design we use design compiler, which is a module of Synopsys tools that uses lsi_10k library and BCCOM method to synthesis the design and simulate the design through VCS compiler.

Keywords: Parallel processing, Pipelining, Matrix multiplier, Clock timing, design area.

I. INTRODUCTION

Now days as complexity of processor is increasing ,so we have to bothered about computational speed of computer system. parallel processing is design technique in computer architecture which is used to increase the computational speed of computer. Parallel processing is done by three ways. These are pipeline processing, array processing and Vector processing. Here we presented two-dimensional Pipelined design task which was challenge in previous paper [1-4]. Pipelining is a method of decomposing a continuous method into sub-operations, each sub-operation being carried out in a unique devoted section that operates at the same time as all other sections.

The paper includes designing, simulating and synthesizing a pipelined matrix multiplier. Basic idea of the paper is Multiplication of two 100X100 element matrices A & B, and store their product in matrix P:

$$A = \begin{matrix} A0,0 & A0,1 & A0,2 & \ldots & A0,99 \\ A1,0 & A1,1 & A1,2 & \ldots & A1,99 \\ A2,0 & A2,1 & A2,2 & \ldots & A2,99 \\ & & \vdots & & \\ A99,0 & A99,1 & A99,2 & \ldots & A99,99 \end{matrix}$$

$$B = \begin{matrix} B0,0 & B0,1 & B0,2 & \ldots & B0,99 \\ B1,0 & B1,1 & B1,2 & \ldots & B1,99 \\ B2,0 & B2,1 & B2,2 & \ldots & B2,99 \\ & & \vdots & & \\ B99,0 & B99,1 & B99,2 & \ldots & B99,99 \end{matrix}$$

$$P = \begin{matrix} P0,0 & P0,1 & P0,2 & \ldots & P0,99 \\ P1,0 & P1,1 & P1,2 & \ldots & P1,99 \\ P2,0 & P2,1 & P2,2 & \ldots & P2,99. \\ & & \vdots & & \\ P99,0 & P99,1 & P99,2 & \ldots & P99,99 \end{matrix}$$

Where $P_{ij} = A_{i,0} \times B_{0,j} + A_{i,1} \times B_{1,j} + A_{i,2} \times B_{2,j} + A_{i,3} \times B_{3,j} \ldots + A_{i,99} \times B_{99,j}$

for all $0 \le I \le 99$ and $0 \le j \le 99$.

II. FOUNDATIONS OF THE PAPER

- A and B are pre-stored in a memory module. Elements of A,B and P are 32-bit unsigned numbers.
- P should be stored in memory.
- The data and address ports for the memory module are 32-bit.
- The arithmetic unit can only operate on register-type data (in a register file).
- At most we can read two elements from a register file in one cycle.
- It takes one cycle to store one element into a register file.
- The results of the ALU cannot directly be written into the memory block.
- The increase of two matrices will begin when an input signal called START is asserted.
- PMM will assert and output signal called “DONE” when multiplication is done.

III. OBJECTIVES

Design and stimulate a functional Pipelined Matrix Multiplier Unit.

To learn about the working of Pipelined Matrix Multiplier and how pipelining works.

Successfully synthesize the design using design compiler using lsi_10k library and BCCOM method.

To get the knowledge of clock timing and learn to make a timing critical design.

How two dimensional pipeline process works.

IV. STEPS TAKEN TO ACHIEVE PAPER GOALS

The paper involved extensive work. Following steps were taken to achieve the desired goal:

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First step involved understanding the PMM and the concept of pipelining datapaths.
Second step involved dividing the entire pipelined datapaths into appropriate stages. The design was divided into:
Memory Unit.
Control Unit with Register.
Fetch Unit.
ALU.
Write-back Unit.
Top Unit.
These stages were equally divided among the two project partners.
Once each one of the individual modules was designed, simulation of each module was done to check its functionality. After confirming the functionality of each of the individual module, the module were synchronized to avoid any syntax error. The next step involved making a Top module that instantiated each module in it. A test file was made to check the entire design. Simulation of the design was carried out and he results were checked.
After confirming the functionality of the entire design, synthesis of each individual module was carried out to check the timing of each module. The Top module was then synthesized taking the largest clock period of the individual module synthesized. Some modifications were made to the multiply module to reduce its clock period [5-9].

A. Memory design

Microprocessor product that require inputs from the user generally include two types of memory :-Read-only memory (ROM or EPROM) and R/W memory. The first consideration of the memory design is the memory size here in this design memory size is 2^32 bytes bi-directional [10-14].

.we have implemented Random-access memory (RAM).Design specification are as fallow-

DATA_IN_P: Apply the data bits

DATA_OUT_AB: output data of AB matrix which is 32 bit wide.

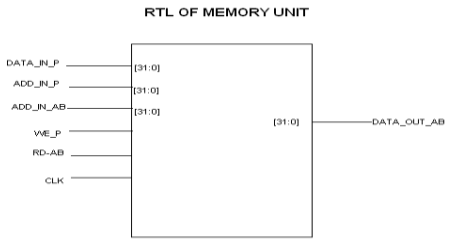
CLK : It is clock signal used to synchronize between datapath and Controller of pipeline design.

RD_AB: Active the read input.

WE_P : Active the write input.

ADD_IN: Applying the binary address of desired word into address line .it is 32 bits wide. ADD-IN-P And ADD-IN-AB are address line of two matrix elements A[10]B[10] and P[10] respectively.

Fig1(a)



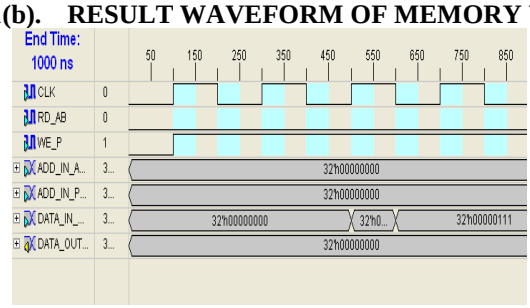
V. SIMULATION RESULTS

If you are using *Word*, use either the Microsoft Equation Editor or the *MathType* add-on (http://www.mathtype.com) for equations in your paper (Insert | Object | Create New | Microsoft Equation *or* MathType Equation). "Float over text" should *not* be selected.

A. Memory Unit

Chronologic VCS simulator copyright
1991-2003Contains Synopsys proprietary information.
Add_in_ab= 10004 , Data_out_ab= 7251 Add_in_p= 4 , Data_in_p= 40
$ finish at simulation time 30

Fig.1(b). RESULT WAVEFORM OF MEMORY UNIT



B. CONTROL WITH REGISTER UNIT Memory design

This module is designed by writing Verilog code in Design complier. Here we are free to use FSM state machine as per design requirements. We are using Mealy state model, it is some what take less space than Moore model of state machine design.

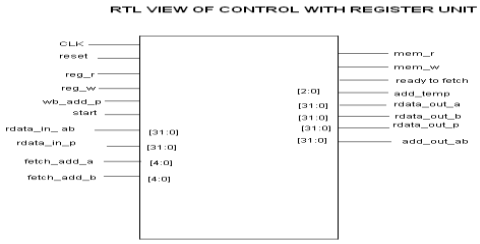
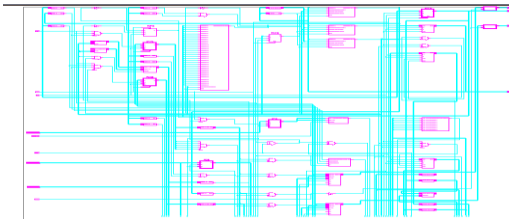


Fig.2. TOP VIEW OF CONTROL AND REGISTER UNIT

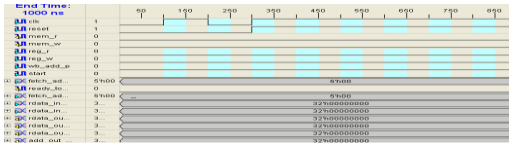


C. Control Unit

Chronologic VCS simulator copyright 1991-2003
Contains Synopsys proprietary information.

V C S Simulation Report
Time: 40
CPU Time: 1.380 seconds;
Data structure size: 0.3Mb
August 1 1:37 2007

RESULT WAVEFORM OF CONTROL AND REGISTER UNIT

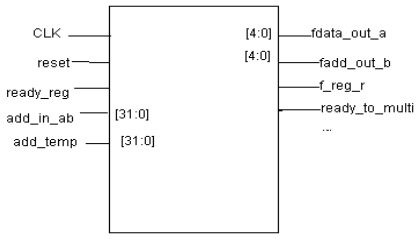


D. Design of Fetch unit

It is one of the important part of design in pipelined matrix design.In this design clk ,reset ,ready_reg are our inputs port of fetch unit.

Fig.3

RTL VIEW OF FETCH UNIT

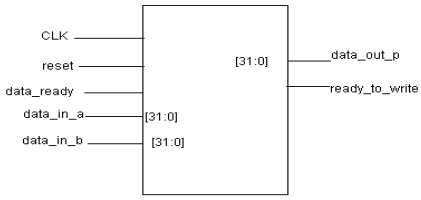


E. Design of ALU with Multiplier

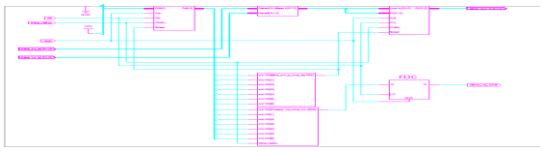
The arithmetic logic unit determines the micro operation to be conducted by arithmetic or logic. In this module each element row of A matrix is get multiplied to the column element matrix of B, then after addition operation finally the results is stored in P matrix . By choosing the different parts in the layout, the control unit that runs the CPU bus scheme guides the information flow through the register and ALU [15].

Fig.4

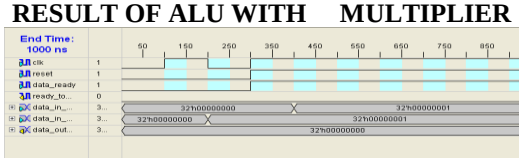
RTL VIEW OF ALU WITH MULTIPLIER



TOP VIEW OF ALU WITH MULTIPLIER



RESULT OF ALU WITH MULTIPLIER

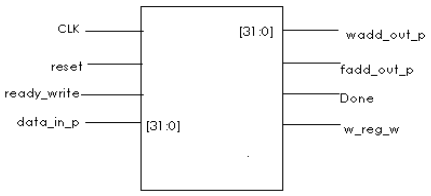


F. Design of write back unit

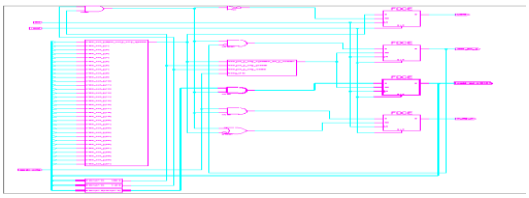
The easiest and most frequently used procedure is to inspect the transfer operation of the primary memory module, whereby the cache memory is accessed in sequence if it includes the term at the given address, its name is written –through technique, this technique has the benefit that the primary memory always carries the same information as the cache. Write back device is introduced here, although this device will update the cache place during write procedure [16].

Fig.5

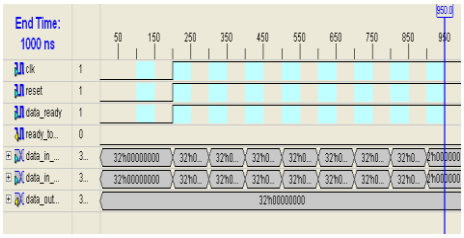
RTL VIEW OF WRITE BACK UNIT



TOP VIEW OF WRITE BACK UNIT



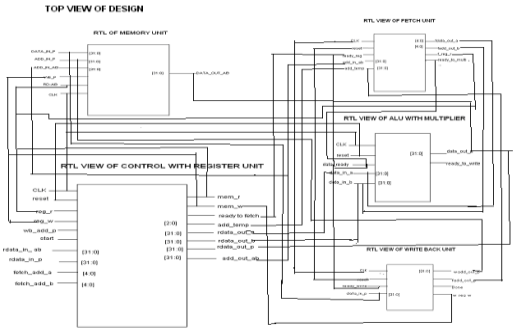
RESULT OF WRITE BACK UNIT



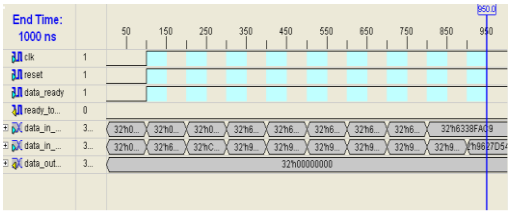
G. TOP VIEW OF PIPELINED MATRIX MULTIPLIER

After writing verilog code for each module, we will proceeds for top level design in design compliers, then synthesis the design ,we will simulate the design “top.v” in VCS compiler[17-20]. Finally we got schematic view of pipelined matrix multiplier.

Fig.6 Top view of pipelined matrix multiplier



RESULT WAVE FORM OF PIPELINED MATRIX MULTIPLIER



VI. SYNTHESIS REPORTS

```
Designer= "Anil Kumar sahu"
 search_path = ".  /sw/synopsys/syn/libraries/syn "
link_library = "* lsi_10k.db"
target_library = "lsi_10k.db"
symbol_library = "lsi_10k.sdb"
default_schematic_options="-size infinite"
read -format verilog {"/Mtech207/anil/synopsys/top.v"}
create_schematic -size infinite  -gen_database
current_design top
link
create_clock -period 10 find (port CLK)
set_dont_touch_network  find (clock CLK)
set_input_delay  -max 0.8 -clock CLK all_inputs() - CLK
set_input_delay  -min 0.2 -clock CLK all_inputs() - CLK
set_output_delay -max 0.8 -clock CLK all_outputs()
set_output_delay -min 0.2 -clock CLK all_outputs()
set_max_area 0
set_operating_conditions -library "lsi_10k" "BCCOM"
uniquify
compile -map_effort  medium  -boundary_optimization
report_attribute
report_area>area_r_a.out
report_constraints -all_violators>constraints_r_a.out
report_timing -path full -delay max -max_paths 1 -nworst
1>timing_r_a.out
```

8.VERIFICATION OF DESIGN TRIAL:

```
Information: Updating design information... (UID-85)
 ****************************************
Report :                          Design area
Design :                          top.v
Version:                          2000.05-1
****************************************
Operating Conditions: BCCOM   Library: lsi_10k
Wire Load Model Mode: top
  Point                    Incr       Path
  clock CLK (rise edge)    0.00       0.00
  clock network delay (ideal)
  R1/U2229/Z (IV)          0.14       1.12 f
  data arrival time                   34.78
 clock CLK (rise edge)     10.00      10.00
 clock network delay (ideal)  0.00    10.00
  A1/data_out_p_reg[31]/CP  0.00     10.00 r
  library setup time        -1.25     8.75
  data required time        8.75
  ---------------------------------------------------------
  data required time        8.75
  data arrival time         34.78
  ---------------------------------------------------------
  slack (VIOLATED) -26.03
```

VII. CONCLUSION

In this paper, we looked at some issue relating to the design of low latency pipelined matrix multiplier as well as high throughput matrix multipliers. in this paper we are also showing of two-dimensional parallel pipeline process which speed up our design but disadvantages is that we required more cell area to fabricate this design while speed is much improved then its Prior design proposed work . This paper is quantitative technique for analysis of pipelining in digital systems, using measure of effectiveness, delay, cost /operation and time /operation. Hence area, speed power is main criteria for system performance.

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