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High Speed, Low Area Exact Speculative Carry Look Ahead Adder using MGDI Technique

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Abstract*: The Exact Speculative Carry Look Ahead Adder using the Modified-GDI (Modified-Gate Diffusion Input) is suggested in this work. The delay, area and power tradeoff plays a vital role in VLSI. We already know that designs which are of CMOS style occupy more space may consume more power consumption. The switching behavior of the circuit cause the heating up of integrated circuits affects the working conditions of the functional unit. The adders are the main parts of several applications such as microprocessors, microcontrollers and digital signal processors and also in real time applications. Hence it is important to minimize the adder blocks to design a perfect processor. This work is proposed on a 16 bit carry look ahead adder is designed by using MGDI gate and 4T XOR gates and a speculator blocks. The proposed MGDI carry Look Ahead adder occupies 68% less area and the power consumption and the propagation delay also drastically reduces when compared to the conventional carry Look Ahead adder why because the number transistors drastically reduces from 1448 (Conventional) to 456 (Proposed CLA). The simulation results of the proposed design implemented in Xilinx.

***Keywords* : MGDI; 4T XOR; CLA; Speculator; Area; Power Consumption; VLSI; ASIC.**

I. INTRODUCTION

In VLSI, a wide-range of development results in minimizing of different parameters. It affects the overhead in delay, power as well as area. Major logic blocks like microprocessors, ALUs and DSPs use the Multipliers and Adders as basic logic blocks. Hence, to enhance these major blocks, it is required to optimize the performance of the multipliers and adders in terms of the aforementioned parameters. An improvement in GDI technique [1-3] which is termed as MGDI is used to solve this issue. Though there is a tradeoff among power, area and delay, high speed logic blocks are essential. The Cognitive Radio has spectrum sensor which uses the basic logic blocks and also its support in IoE (Internet of Everything) is major [4-6].

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At present, the physical interfaces are very important to integrate all the functional units to work as an integral unit and the big challenges are faced to achieve the desired logic. Sensors and actuators are the transducers to convert the input signals to the processors which perform the conditioning activity in a hardware unit. The process time is the key factor in measuring the performance any design which needs optimization. The adders optimized in terms of speed by means of using the appropriate methods to reduce the delay of the circuit which is suitable for this work too. Using appropriate technique, it is possible to reduce the delay and optimize the design area with possible low power requirements within the allowable degradation limit [7]. With the help of speculative method, the accuracy can be traded off to achieve circuit speed and power. Such adder is termed as Exact Speculative Adder (ESA), while the inexact speculative adders concentrated majorly on accuracy of their results.

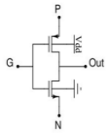


Fig. 1: MGDI Cell

By maintaining the same accuracy, there are lots of possibilities to reduce the delay of the circuit using numerous methods. This work uses the modified GDI based exact speculative CLA method and the results are analyzed. Using one set of PMOS and NMOS in MGDI, all the basic logic functions are possible to obtain as an advantage. Compared to conventional CMOS technology, the modified GDI structure is given in Fig. 1. In Fig. 1, one can understand that the common input to gate is G, the input to NMOS is N while the PMOS input is P. Like conventional CMOS circuit, the substrates of PMOS and NMOS are connected to V_{dd} and *gnd* respectively. Table 1 represents the logic functions which can be obtained using modified GDI [1].

Table 1: The logic functions of modified GDI

N	P	G	Out	Function
'0'	B	A	$\bar{A}B$	F1
B	'1'	A	$\bar{A}$+B	F2
'1'	B	A	A+B	OR
B	'0'	A	AB	AND
C	B	A	$\bar{A}B$+AC	MUX
'0'	'1'	A	$\bar{A}$	NOT

Table 2: MOS transistors used in CMOS and mGDI for various logics.

Function	CMOS (no of transistors)	mGDI (no of transistors)
F1	6	2
F2	6	2
OR	6	2
AND	6	2
NAND	4	4
MUX	12	2
NOT	2	2

In CMOS method, it requires 6 to 12 transistors. But many of the basic logic functions are possible in MGDI with only 2 transistors [2]. The number of transistors in CMOS and MGDI are in Table 2.

To design the carry look ahead adder needs the logic gates like XOR, AND and OR gates with either 2, 3, 4 or 5 inputs. To design all these type of logic gates it requires more number of transistors and also the area and power consumption increases. Nowadays the size of all electronic equipment are very small like mobile phones and DSP kits, Microprocessors and Embedded systems.

In this paper an Exact Speculative CARRY LOOKHEAD ADDER is proposed by using MGDI technique. by using this technique the area required to design is drastically reduces when compared to the existing methods. The remaining sections of this paper provides the discussion on existing method, proposed method, analysis, verification, simulation results and conclusion.

II. EXISTING METHOD

The conventional inexact speculative adder for n-bit addition is given in Fig. 2. In this figure, the *n*-bit input are divided into 4-bit blocks with the value of $x = 4$. For the *x*-bit adder, the blocks feed the value of operands. Unlike the conventional ISA architecture, the adder unit has been replaced with 4-bit CLA ensures the high speed working conditions. In the following paragraphs, explanations with details of blocks along with various sub modules of the existing adder are given.

Adder Blocks and Speculators: Before discussing the circuits, arrangements and functions of the ESA, it is required to know some of the notations. The addition operands for addition are named as *A* and *B* for an n-bit adder with $A = \{ _0, _1, ... _{-1}\}$ and $B = \{ _0, _1, ... _{-1}\}$; Here, the sum output are expressed as $S = \{_0,_1, ..._{-1}\}$. Fig. 2(b) represents the speculator block at gate level representation which is used in this paper as a speculator. This block is based on CLA logic to speculate the output carry for each 4-bit adder block. Speculation is carried out for '*r*' MSB bits of each block where *r* is less than the size of block, (i.e., $r<x = 4$). Subsequently, the input carry for each speculator block is 0 (or 1) which introduce positive (or negative) errors respectively. The output carry, which is denoted as, from each speculator block is fed as an input carry for the adder block succeeding it, as shown in Fig.2. Now, each 4-bit adder block need not wait for the input carry from the preceding 4-bit adder block. Instead, all such adder blocks perform simultaneously additions on receiving input carries from the concerned speculator blocks.

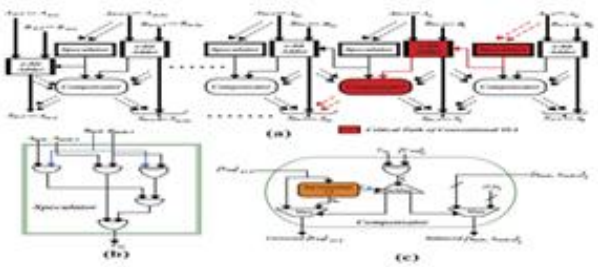


Fig. 2: (a) n-bit conventional ISA adder. (b) Gate level representation of speculator block. (c) Digital architecture of compensator block.

In the above existing method all the blocks are designed by using logic gates based on the Boolean expressions. There are mainly three blocks those are the adder, speculator and compensator. In the above circuit x bit adder means it is 4 bit carry Look Ahead adder it internally consists of carry generation circuit and also it consists of four XOR gates and also OR and AND logic gates to generate sum and carry [8-12].

In previous the next full adder can wait until the carry propagated to it because of this the operation or speed may be reduced. Due to this reason one can designed a speculator block to generate the carry to the next stage. The compensator block can generate the corrected sum results for the given inputs. By using CMOS Technology the above method requires 1448 transistors for a 16 bit addition. In the above method it consists of four blocks, each block consists of adder of bit size 4, compensator and speculator. All these blocks are designed by using logic gates.

III. THE PROPOSED METHOD

This section describes the proposed Exact Speculative Carry Look Ahead Adder and the MGDI based AND gates and OR gates. The use of MGDI gates reduces the design area.

3.1 The Proposed Exact Carry Look Ahead Adder

Because of the use of MGDI gates, the proposed method the number of transistors can drastically reduce from 1448 to 456 transistors only based on MGDI technique. Due to this the dynamic power consumption reduces and speed of the operation also increases. The following section will explain and shows the proposed Exact Speculative Carry Look Ahead Adder.

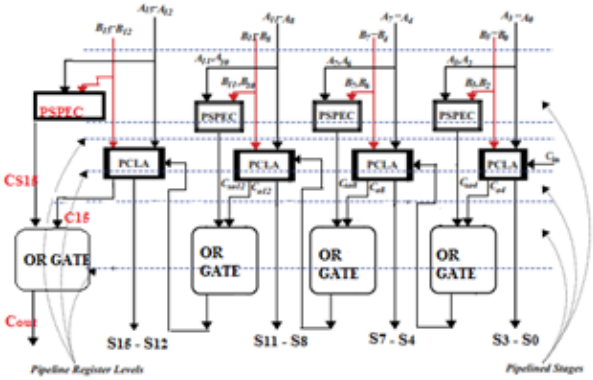


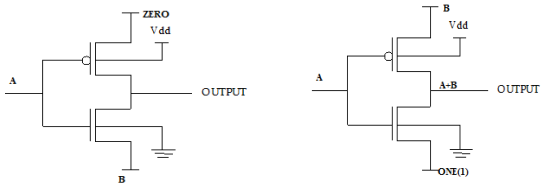
Fig. 3: The Proposed Exact Speculative Carry Look Ahead Adder.

In this to get the carry for the next stage a speculator and a two input or gates are used. Here the total logic gates are designed by using MGDI technique and instead of using 12 transistor, the XOR gates use only 4 transistor to generate the sum bits and the CLA adder, in its internal circuit it consists of 5, 4, 3 and 2 inputs based AND and OR gates. For example consider 5 inputs AND gate, to design this it requires 12 transistors in pull up and pull down paths and to get the correct output an inverter is attached to it.

Hence it increases the design area and also propagation delay increases and speed also reduced. In order to avoid all these types of trade off in the proposed method all the blocks are design with only NMOS and PMOS transistors pairs called as MGDI technique. The following will explain the internal blocks of carry Look Ahead adder.

3.2 MGDI Logic Gates

The structure of 2 input AND gate and OR gate are shown in Fig. 4(a) and Fig. 4(b) respectively. MGDI logic gate single NMOS and single PMOS transistors. The gate terminals of both transistors are connected to one input and the PMOS drain is connected to the logic zero.



(a). AND gate (b) OR gate

Fig. 4: MGDI based two input gates

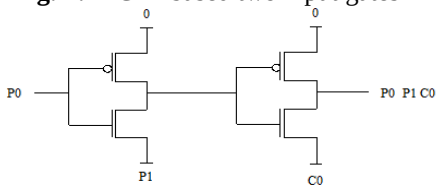


Fig. 5: MGDI based three input AND gate

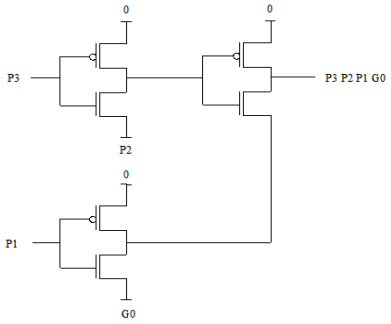


Fig. 6: MGDI based four input AND gate

The source of NMOS is connected to another input and the output collected at the terminals of NMOS drain and PMOS source (both are tied together). The substrate of PMOS and NMOS are connected to the V_{dd} and ground respectively. Three inputs AND gate can be constructed by cascading two 2-input AND gates as shown in Fig. 5 while the Fig. 6 shows the Four input MGDI gates in similar fashion. These kind of MGDI structures help a designer to reduce the circuit area remarkably by using 4 transistor for three input logic gates and 6 transistors for four input logic gates against 8 and 10 transistors respectively in a CMOS technology. Similarly the three inputs and four inputs MGDI type of OR gates can be constructed.

To design a conventional XOR gate 12 transistors are required. Hence the area required by a design which uses XOR gate may increases along with increase in propagation delay. Hence to reduce the number of transistors in the proposed method, a 4T XOR gate is constructed as in Fig. 7. It has NMOS and PMOS transistors similar to the CMOS Inverters. The overall circuit of this 4T XOR is a simple structure obtained by cascading two CMOS Inverters. In the first stage the PMOS drain is connected to the V_{dd} and source is connected to the NMOS drain and source of NMOS is connected to the ground.

The gate terminals of both PMOS and NMOS are connected to the input1. The output of the first stage is connected to the source of second stage NMOS and drain of second stage PMOS is connected to the input 1. The gate terminals of the second stage PMOS and NMOS are connected to the Input 2 and the source of PMOS and drain of the NMOS of the second stage are tied together to get the XOR output. When the V_{dd} is ON, based on the condition of Input1, either PMOS or NMOS is ON and generate the complement. The operation of 4T XOR GATE is listed in Table 3 for various logic combinations of inputs.

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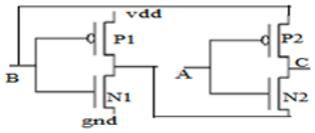


Fig. 7: 4T XOR gate

Table 3: Switching state of Transistors and function of 4T XOR gate

Inputs		PMOS P1	NMOS N1	PMOS P2	NMOS N2	OUTPUT A XOR B
A	B					A
0	0	ON	OFF	ON	OFF	0
0	1	OFF	ON	ON	OFF	0
1	0	ON	OFF	OFF	ON	1

3.2 Speculator

Speculator is a block which consists of MGDI AND gate and OR gates which helps the adders to reduce the design area. The block diagram of speculator as shown in Fig. 8 consists of three AND gates one OR gate and one XOR gate. To reduce the design area in the proposed method all these logic gates are replaced by MGDI AND gates and OR gates. The XOR gate is replaced by 4T XOR gate in Fig. 8. The output of the speculator and the carry out of the 4 bit adder are passes through the 2 input MGDI OR gate. The output of the MGDI-OR gate is used as carry input for the next stage.

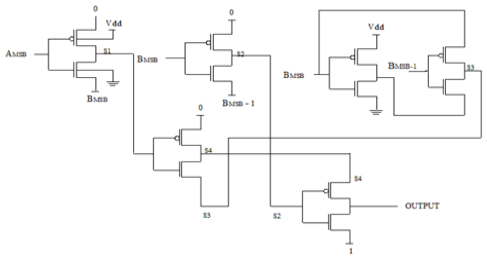
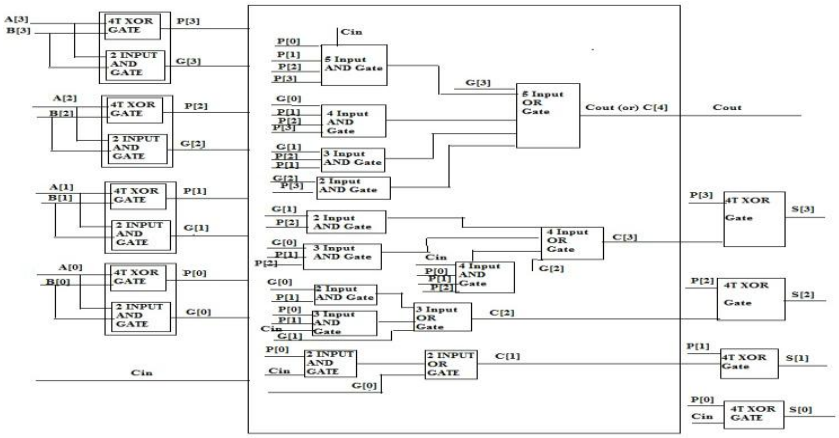
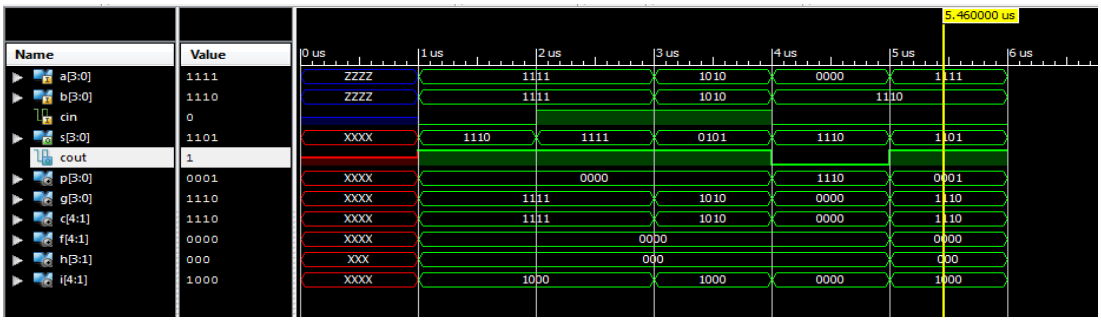


Fig. 8: Speculator block

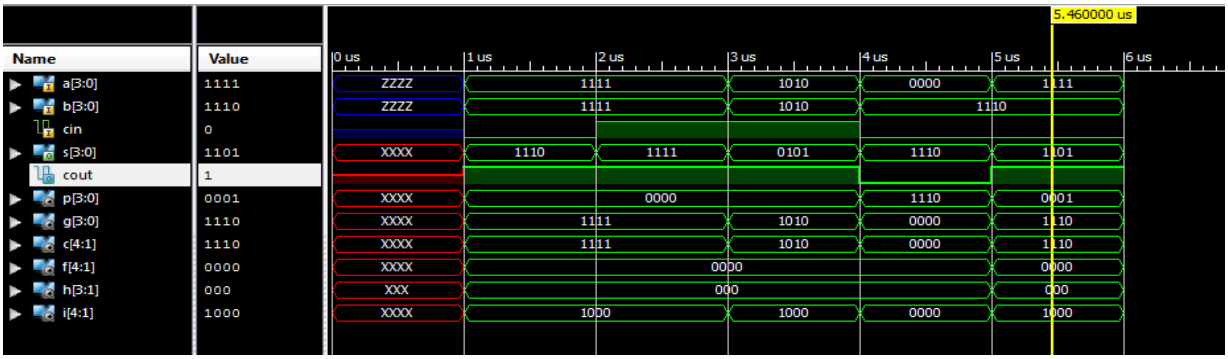


a. **Fig. 9: Parallel Carry Look Ahead Adder (PCLA)**



b.

c. **Fig. 10: Simulation result of 4 bit Parallel Carry Look Ahead Adder (PCLA)**



d.

e. **Fig. 11: Simulation result of 16 bit Exact Speculative Carry Look Ahead Adder**

3.3 The 4-BIT CARRY LOOK AHEAD ADDER:

The 4 bit carry Look Ahead adder [13-15] is faster as it is constructed with minimum transistors due to which the circuit is simpler as shown in Fig. 9. Here in this proposed 4 bit PCLA, the internal structure of the CLA is totally replaced by the MGDI technique. To design the 16 bit CLA, one can follow the cascading of four 4-bit adders with the speculator and OR gate by referring Fig. 9 itself.

IV. SIMULATION RESULTS

The simulation of the 16 bit exact speculative can be performed using Xilinx software. The output waveform consists of the 16 sum bits and one final carry and intermediate wire segments and inputs. It reveals that it requires less time to give the output. The speed of the operation increases as the delay is lower due to circuit simplicity. The 16 bit exact speculative CLA occupies less design space due to the use of MGDI method along with speculator. The simulation results of 4 bit and 16 but CLA are given in Fig. 10 and Fig. 11 respectively. The comparative analysis of conventional and proposed CLA are given in table 4.

Table 4: Comparative analysis of conventional CMOS and proposed CLA

Type of 16 bit CLA	Technology	Operating Clock Frequency	Device Count	% of Area utilization
CMOS based CLA	90 nm	224.57 MHz	1448	--
Proposed - MGDI based CLA	90 nm	344.64 MHz	456	68 %

V. CONCLUSION

Low area and high speed exact speculate CLA adder type of the ESA logic was presented. This design has been proposed to increase the speed of the operation and reduce power consumption and reduce the area respectively. Experimental results showed that the proposed one with a maximum frequency of 344.64 MHz and the conventional adder operates at a frequency of 224.57 MHz in 90nm ASIC and FPGA arrangements respectively. Subsequently the proposed method reduces the transistor count drastically from 1448 to 456 transistors only i.e., 68% lesser then the existing method. By using this MGDI technique the power consumption and area reduces when compared to the CMOS technology. The design works with a considerably good role in the design of consumer electronics as well as future trending electronic gadgets for IoE and many other modern-day applications. However, the power issue can be eliminated by some extent using suitable design approaches.

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