

FPGA Based Performance Analysis of Multistage CIC Decimation Filter Design with former CIC Filter for WiMAX Applications



V Jayaprakasan, Sudhir Kumar Madhi, V.G.Hamsaveni, S.Priyanka, S.Vijayakumar

Abstract: The motto of this paper is to design and realize decimation filter using CIC filter. The main drawback of this filter is there is large droop in pass band and very less attenuation in stop band. So, to improve the frequency response of CIC filter we go for two stage realization of CIC filter. At the initial stage we use CIC filter and in the last stage we use Kaiser Window and improve the characteristics of filter design. When we design a filter using multistage methodology the order of the filter as well as power also decreases. Tools used are MATLAB Simulink Model and Xilinx system generator and realization is done on Virtex V-XC5VLX110T-3ff136. In this paper the proposed two stage realization is compared with respect to two stages Kaiser window realization in the terms of number of LUT's required, slices as well as power dissipation and improvements in frequency response with respect to conventional CIC filter are compared.

Keywords: WiMax Applications, CIC Filter, FPGA, Multistage CIC

I. INTRODUCTION

In the area of Wireless applications signal processing plays a very key role. The signal processing is taken into consideration because rate of the signal changes during transmission until it reaches the reception this also technically named as multi rate signal processing. In the multi rate signal processing two blocks are taken into account they are DDC and DUC. The application of DDC or DUC is to improve Signal to noise ratio (SNR) and inter channel interference (ICI). WiMAX stands for worldwide interoperability for micro wave access. The decimation factor of WiMAX is 8, which is realized into two stages. When we introduce this concept of two stage design overall there is improvement in pass band, stop band, device usage, amount of power consumed when compared with single stage realization.

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Due to improvements in VLSI, FPGA is used in DSP applications.

The reason behind using FPGA is it can be reprogrammable; it can as well be reconfigurable and common parameters for any electronic device is it must be low cost and highly reliable. Reliability means within in a stipulated amount of time the device should work effectively. So, FPGA has all these qualities so we bring FPGA into DSP applications. Multi rate sampling means rate of the data should be changed from arbitrary sampling rate to user defined sampling rate. The best example can be taken as audio signal sampling which is 48 Khz. Audio engineering society recommended 48 Khz as major application but it gave 44.1 Khz for CD and other consumer applications. So, here rate of the signal is changing at every instant for every application so we conclude that multi rate signal processing gives us motivation to design the required application.

II. CASCADED INTEGRATOR COMB (CIC) FILTER

Cascaded integrator comb (CIC) filter was introduced in 1981 which is especially used in multirate systems practically used as large sample rate converters. It is a multiplierless architecture but the disadvantage of this filter is it has non flat response in the pass band. In our application this problem can be overcome by introducing a compensator. In our paper our assumption is in the first stage CIC is used and in the second stage for compensating it we are using Kaiser window. In the Z domain transfer function is represented as,

$$H(Z) = \frac{1}{N} \left[\frac{1 - z^{-N}}{1 - Z^{-1}} \right] \quad (1)$$

The frequency response of single stage CIC filter is given by,

$$H(e^{j\omega}) = \left[\frac{1}{M} \frac{\sin(\omega M / 2)}{\sin(\omega / 2)} e^{-j\omega(M-1)/2} \right] \quad (2)$$

The integrator portion will operate at a larger rate; It requires more chip area and consumes large power. But the differentiator portion is operated at a rate of . By introducing the concept of decimated CIC filter the device usage and consumption of power are decreased a lot. The single stage realization of this filter as shown in Fig (1).



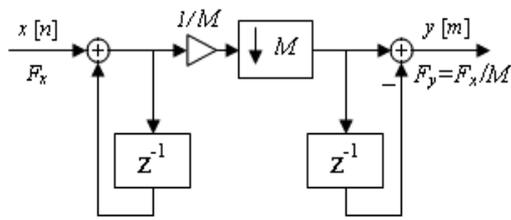


Figure 1. Single Stage realization of CIC

Saramaki T had examined a linear phase FIR filter characteristic of the proposed filter like placement of zeros, coefficient of sensitivity is contrasted with respect to former FIR stages. He has demonstrated that narrow band can be achieved when multistage decimators and interpolators are cascaded. In 1973 Parks McClellan have built up a program to achieve an ideal digital low pass filter which is linear phase in nature. This program had choices for planning typical filters like LPF, HPF, BPF, BSF. This program is likewise useful for configuring filters with respective specifications given by the clients. It was written in FORTRAN language.

Bellangar have planned a polyphase system design. This allows the utilization of feedback devices for productive sampling rate modification. On examining with respect to traditional filter design demonstrates that with a similar dynamic memory, a reduction in multiplication rate moving towards a factor of two was accomplished when modification factor increments. Gustafsson executed a FIR filter which is polyphase decomposed utilizing various strategies which uses a constant number of multiplications using least amount of hardware like adders and subtractors. When we consider interpolation with direct form sub filters which lead to less registers as the mutual design of sub filters. However, in the direct form transposed sub filters registers can't be in mutually shared format. At last comparison is done in terms of amount of space required, power consumed and operational speed for various realizations.

Ranstad TE and Sramaki have introduced about system design which is capable for actualizing for all intents and purposes any viable LPF and HPF which utilizes approximately 60 multiplications per sample. This technique is also applicable for multi rate procedures as well as complementary filters. [7] Suvarna joshi and Bharati anapure, executed fundamental FIR design with the assistance of FPGA using Xilinx System Generator (XSG). A tool called MATLAB was utilized to decide channel coefficients. Finally, structure was implemented on XC3S5004FG320 in SPARTAN 3E platform using Xilinx.[8] introduced a power efficient decimator structure ADC for biomedical applications. In [9] memory saving approach was taken into consideration using polyphase decomposition. The design was executed with the assistance of XSG.

III. CONVENTIONAL FIR FILTER

In the single stage design for a factor of M decimation factor with h(n) as impulse response. In the discrete domain it can be represented as,

$$v(n) = \sum_{k=0}^{N-1} h(k)x(n-k) \quad (3)$$

Where N=order of the filter, The realization is as illustrated in Figure 2 after down sampling by a factor of M it can be written as,

$$y(m) = \sum_{k=0}^{N-1} h(k)x(nM - k) \quad (4)$$

y(m) represents decimated signal at the output. The direct form realization is as shown in Figure 3.

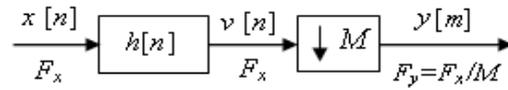


Figure 2. Decimation by a Factor of M for FIR Filter

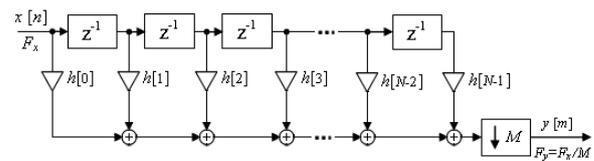


Figure 3.

Decimation by a Factor of M direct form Realization

IV. DUAL STAGE FILTER DESIGN

When we introduce the concept of multistage filter design multiplication rate of the signal is decreased. We divide M into two stages M1 and M2 where M1 is the oversampling ratio of first stage and M2 is oversampling ratio of second stage. So, when two stages are cascaded then decimation factors get multiplied i.e. M=M1*M2 as illustrated in Figure 4.



Figure 4.

Dual-stage realization by a Factor of M where M=M1xM2

The efficiency of H1(z) can be written as,

$$Rm_dec_H_1 = N_1 * F_{y1} = N_1 * \frac{F_x}{M_1} \quad (5)$$

The efficiency of H2(z) can be written as,

$$Rm_dec_H_2 = N_2 * F_{y2} \quad (6)$$

So, the cumulative multiplication rate is,

$$Rm_dec = Rm_dec_H_1 + Rm_dec_H_2$$

$$Rm_dec = N_1 * F_{y1} + N_2 * F_{y2} \quad (7)$$

Where,

N1 is the order of first stage.

N2 is the order of second stage

Rm_dec_H1 is the multiplication rate of first stage.

Rm_dec_H2 is multiplication rate of second stage

Rm_dec is the cumulative of the two stages

Figure 5 indicates the single stage equivalent of dual stage realization where second stage is represented by $H_2(Z^{M1})$. We conclude that multiplication rates of the two stages are added.

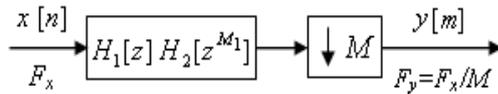


Figure 5. Single Stage equivalent of Dual stage realization

V. FPGA REALIZATION OF THE PROPOSED FILTER

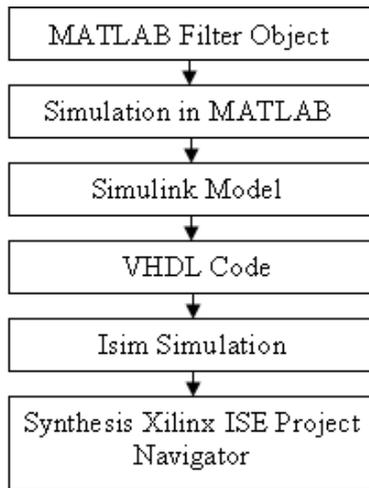


Figure 6. FPGA synthesis Flow

The ongoing headway in Very Large-Scale Integration innovation especially in FPGA as made conceivable; acknowledgement of the processed DSP set of rules in the high frequency domain with this advancement a system on chip arrangement is feasible for DSP based implementations

like ADC in the corresponding framework. Computerized usage couples with signal processing calculations which incredibly improves system performance. Power efficient Digital Signal Processing design are actualized by varying the inspecting clock for every subsystem relying on genuine requirements. The variation in rate of the signal will results in aliasing, this requires the filter utilization to overcome this problem.

In the initial stages model was designed in Simulink tool which is a package from MathWorks. Figures (9) illustrates dual stage implementation of Kaiser window-based realization for $M=8$. The Simulink model was taken as implication for synthesis of in FPGA XSG and is used to implement this model. The XSG provides Simulink block sets and then converted into VHDL for synthesis.

VI. RESULTS AND DISCUSSION

The two different combinations of two stage design are $M=2 \times 4$, $M=4 \times 2$ are compared with respect standard CIC filter of $M=8$ in terms of pass droop and alias rejection, in terms of hardware it is compared in the terms of number of registers, number of LUT's required for the desired application. By using FDA tool, we find minimum order Kaiser window response for the second stage and we compare the characteristics in both droop in pass band and alias rejection of the CIC filter design. The power consumption is also discussed with respect standard CIC filter. Magnitude response characteristics are plotted in figures 7 and 8 and improvements in pass band and stop band are discussed.

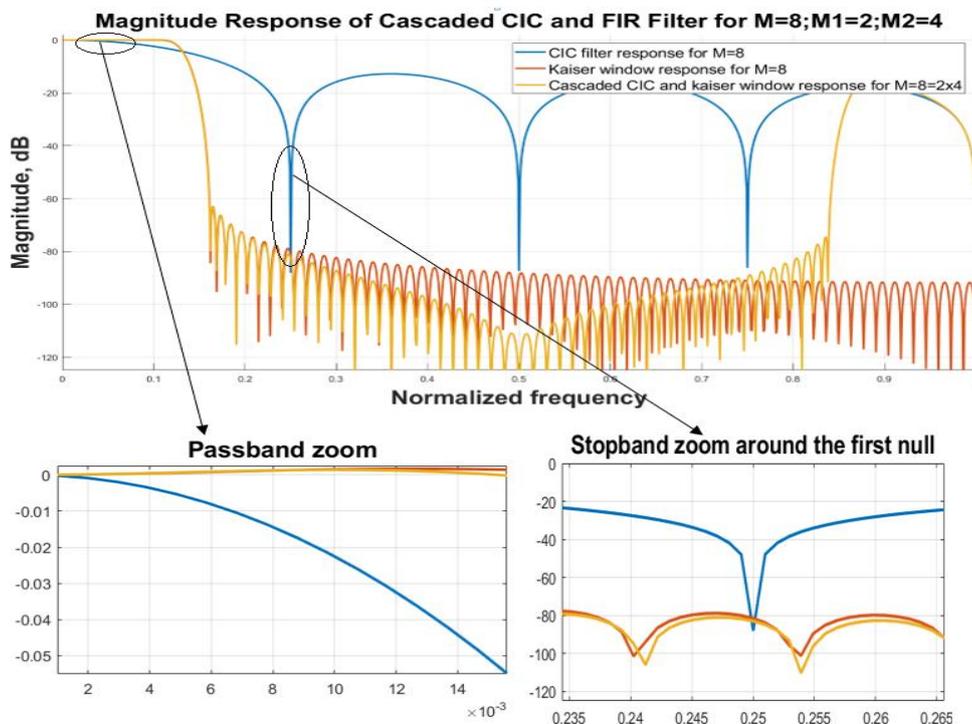


Figure 7. Frequency Response for WiMAX with $M_1=4$, $M_2=2$

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Table 1 indicates improvement in the response of the filter design in pass band and stop with respect to conventional CIC filter. The proposed filter has maximum improvement of 99.72% in the passband when $M_1=2, M_2=4$, and maximum improvement in attenuation the stop band is 71.60% when $M_1=4, M_2=2$.

Figure 9 illustrates Xilinx platform two stage realization of Kaiser Window with $M_1=4, M_2=2$ and $M_1=2, M_2=4$

respectively. Figure 10 illustrates Xilinx platform two stage realization by placing CIC in the initial stages and Kaiser window in the second stage with $M_1=4, M_2=2$ and $M_1=2, M_2=4$ respectively. Table 2 discusses device usage and percentage of power saved for realization of the proposed filter design for the combinations $M_1=4$ and $M_2=2$ and $M_1=2$ and $M_2=4$ respectively.

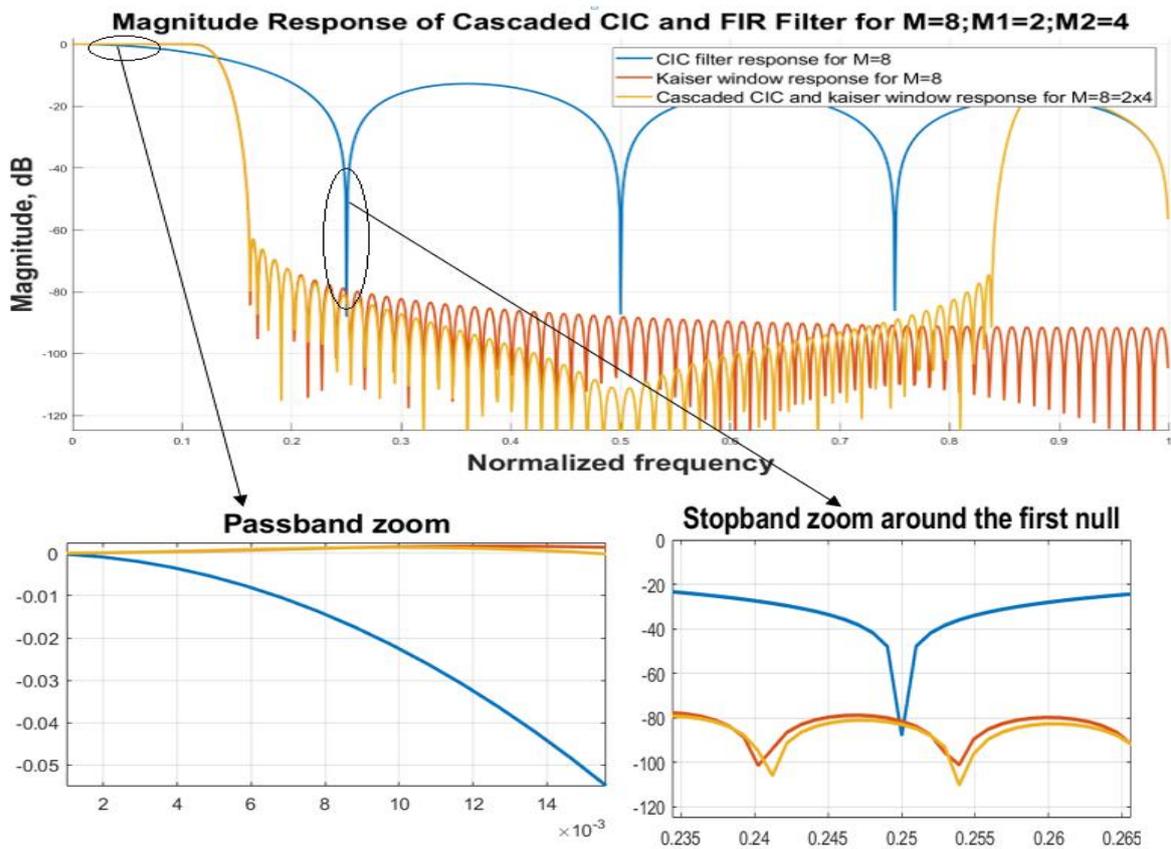
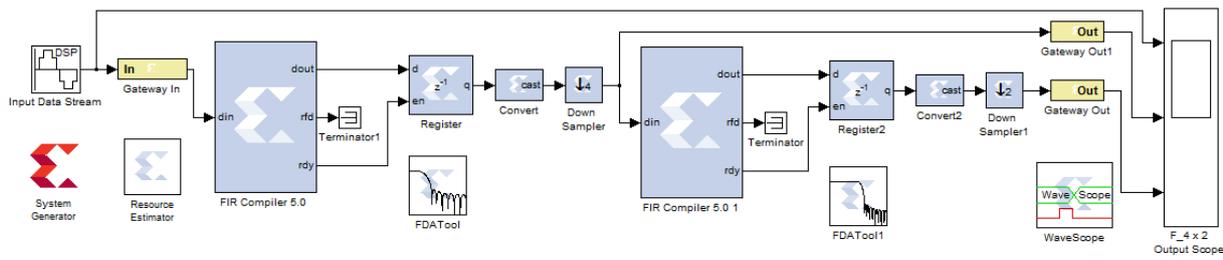


Figure 8. Frequency Response for WiMAX with $M_1=2, M_2=4$

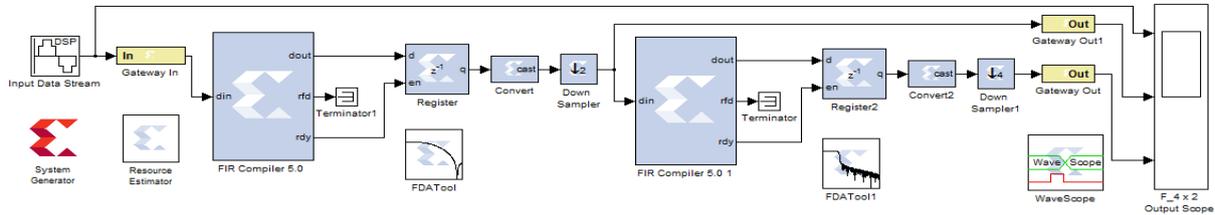
Decimation Filter Specification Characteristics of the filter Conventional CIC Proposed CIC with Kaiser window as second stage and Improvement in percentage.

Table 1 Improvement in the response of filter design with respect to Novel CIC filter

Decimation Filter Specification	Characteristics of the filter	Conventional CIC	Proposed CIC with Kaiser window as second stage	Improvement in percentage
$M=8, M_1=4, M_2=2$	Passband droop (dB)	-0.0550	-0.0104	81.09%
$M=8, M_1=4, M_2=2$	Alias Rejection (dB)	-23	-81	71.60%
$M=8, M_1=2, M_2=4$	Passband droop (dB)	-0.0550	-0.00015	99.72%
$M=8, M_1=2, M_2=4$	Alias Rejection (dB)	-23	-80	71.25%

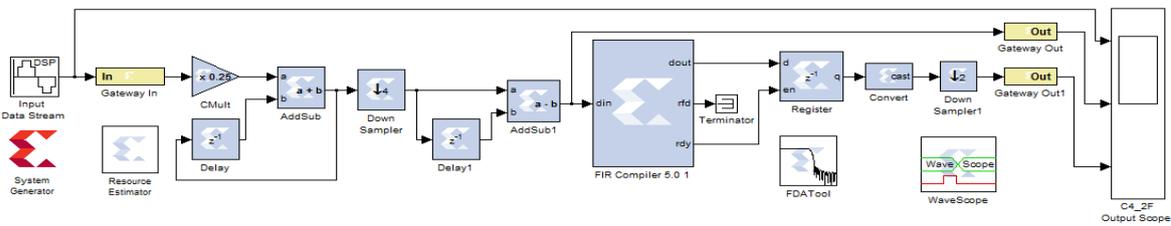


(a) Xilinx platform dual stage Kaiser window realization for WiMAX with $M1=4, M2=2$

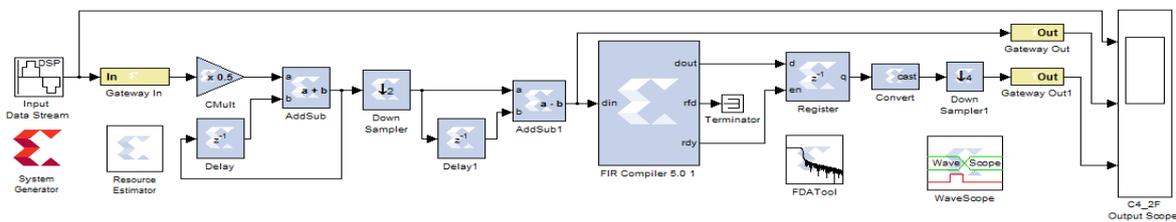


(b) Xilinx platform dual stage Kaiser window realization for WiMAX with $M1=2, M2=4$

Figure 9. Implementation structure for two stage Kaiser-window



(a) Xilinx platform dual stage realization for WiMAX with $M1=4$ for CIC, $M2=2$ for Kaiser window



(b) Xilinx platform dual stage realization for WiMAX with $M1=2$ for CIC, $M2=4$ for Kaiser window

Figure 10. Implementation structure for two stage filter design by considering first stage as CIC and second stage as Kaiser Window

Table 2 Device usage summary for Proposed Filter design for WiMAX application

M=8	CIC	Kaiser Window realization	Number of Registers	Number of LUT's	Number of LUT flip flop pairs used	Power in watts	Percentage power in Savings
Dual Stage Kaiser Window		4x2	2148	1086	2215	0.129	

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Proposed Decimation filter with conventional CIC	4	2	1271	470	1330	0.096	25.5%
Dual Stage Kaiser Window		2x4	3723	1990	9811	0.018	89.22%
Proposed Decimation filter with Conventional CIC	2	4	2826	1444	2882	0.167	

VII. CONCLUSION

The two stage Kaiser window realization is implemented on Virtex-V FPGA kit and simulation results are noted down in tabular form as shown in Table 2 and it is compared with respect to proposed CIC filter design by considering Kaiser window as second stage. Comparison is done with respect to number of registers, number of LUT's, number of LUT flip flop pairs used and power in watts. From the above table it can be concluded that with $M_1=4$, $M_2=2$ the power saved almost equal to 25% When we compare magnitude response of proposed filter with single stage realization by considering $M_1=2$, $M_2=4$ the pass band improvement was approximately equal to 99.72%, alias rejection was approximately 71.25%. so, overall CIC filter response became almost flat by introducing Kaiser window in the last stage.

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