

# Euler and RK4 Algorithms Based Implementation of Autonomous Chaotic Generator

Subodh Kumar Pandey, Alpana Pandey



**Abstract:** Chaotic systems plays a vital role in the field of security, data hiding and steganography. FPGA implementation makes more advantageous compared to analog one. Different chaotic systems like chaos generator and nondeterministic number generator used for security purpose and key generation were successfully realized in FPGA. In this paper, FPGA implementation of Pandey-Baghel-Singh chaotic system (PBSCS) using Euler and RK4 numerical algorithms is presented. Pandey-Baghel-Singh chaotic system were obtained using numerical differential solution and numerically modelled in Verilog with the environment of Xilinx Vivado 2017.3 design suite. The design is verified using experimental setup with the help of interfacing to PC and FPGA family of Artix-7 Nexys 4 DDR and Basys3. Performance of the FPGA based chaotic generator using Euler and RK4 algorithm are analyzed using 1 GB data sets with the maximum operating frequency achieved up to 359.71 MHz.

**Key Words -** Chaotic Generators, RK 4 algorithm, FPGA

## I. INTRODUCTION

Chaos generator is a fundamental block of any chaos based system. Basically chaos based system are used in secure communication and cryptography. Recently implementation of FPGA based real time chaotic systems were presented. Due to parallel processing capabilities the processing speed of FPGA is much higher. Analog based chaotic generators are sensitive to initial conditions and acquires a large chip area hence it may be interesting to see the performance of FPGA based chaotic generators to avoid these problems. Digital based design of chaotic generators using FPGA can be implemented as FPGA implementation is more flexible architecture and have low cost test cycle and found more useful in chaos based engineering applications [1-7].

In II section of the paper presented the Pandey-Baghel-Singh Chaos System (PBSCS) is described along with their x, y and z signals and their attractors [8]. In the III section the mathematical models of PBSCS is numerically obtained with Euler and RK4 algorithms and FPGA models of PBSCS is introduced. In section IV simulation results of different numerical algorithm based design has been presented and analyzed. In section V conclusion is given.

## II. INTRODUCTION TO PANDEY- BAGHEL- SINGH CHAOS SYSTEM

Pandey- Baghel-Singh Chaos System (PBSCS) is defined by the set of differential equation (1).

$$\begin{aligned} \dot{x} &= y \\ \dot{y} &= z \\ \dot{z} &= -ax - by - cz - x^2 \end{aligned} \quad (1)$$

In the system two equilibrium points as (0, 0, 0) and (-1, 0, 0) were shown for the constants  $a = 1$ ,  $b = 1.1$ , and  $c = 0.4$ . The equilibrium point (0, 0, 0) have the Eigen values - 0.745,  $0.162+j1.147$  and  $0.162-j1.147$ . For the equilibrium point (-1, 0, 0) the Eigen values shown are 0.589,  $-0.504+j1.20$ , and  $-0.504-j1.20$ . The initial condition for the system is taken for  $x = 0.1$ ,  $y = 0$  and  $z = 0$ . The time domain representation of x, y and z waveform are given in Fig.1 and attractors generated are given in Fig. 2 (a-c).

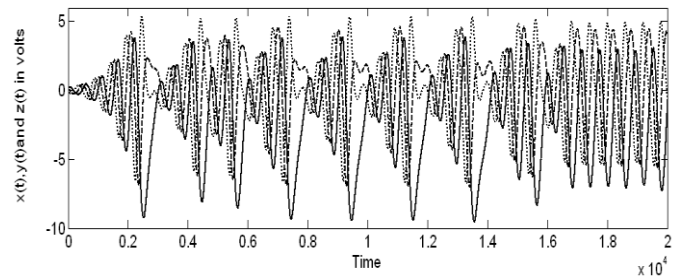


Fig 1: Time domain representation of x, y and z signals of PBSCS.

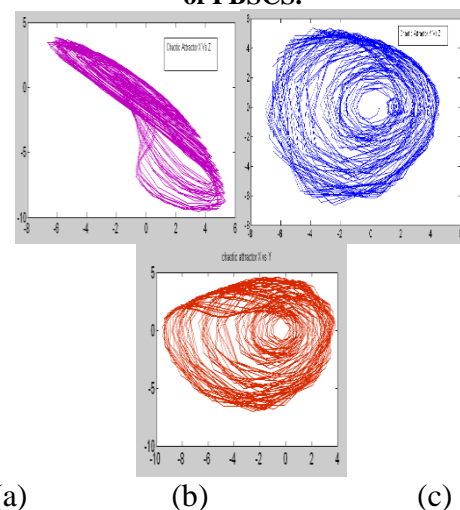


Fig 2: (a) x-y attractor, (b) y-z attractor, (c) x-z attractor

Revised Manuscript Received on October 30, 2019.

\* Correspondence Author

**Subodh Kumar Pandey\***, Directorate of Technical Education M. P. Bhopal, India. Email: subodhpandey88@gmail.com

**Alpana Pandey**, Department of Electronics and Communication Engineering, M.A.N.I.T. Bhopal, India. Email: [alpanasubodh@gmail.com](mailto:alpanasubodh@gmail.com)

© The Authors. Published by Blue Eyes Intelligence Engineering and Sciences Publication (BEIESP). This is an open access article under the CC BY-NC-ND license (<http://creativecommons.org/licenses/by-nc-nd/4.0/>)

**III. NUMERICAL MODELS OF PBSCS AND THEIR FPGA IMPLEMENTATION USING DIFFERENT NUMERICAL ALGORITHMS**

For FPGA implementation of the system the numerical model of PBSCS is obtained using Euler and RK 4 algorithm and coded in Verilog.

**A. Numerical model using Euler algorithm**

For the numerical model using Euler algorithm initial value of  $x(n)$ ,  $y(n)$  and  $z(n)$  are taken as  $x(t_0) = x(n) = 0.1$ ,  $y(t_0) = y(n) = 0$  and  $z(t_0) = z(n) = 0$ , and the mathematical model of PBS chaotic system is described by the following Equation (2).

$$\begin{aligned}
 x(n+1) &= x(n) + h \cdot y(n) \\
 y(n+1) &= y(n) + h \cdot z(n) \\
 z(n+1) &= z(n) + h \cdot \{-a \cdot x(n) - b \cdot y(n) - c \cdot z(n) - x(n)^2\}
 \end{aligned}
 \tag{2}$$

**B. Numerical model using RK4 algorithm**

To construct the mathematical model of the PBSCS using RK4 algorithm, the system equation are represented as a function of  $f, g$  and  $\delta$  as equation (4)

$$\begin{aligned}
 \dot{x} &= f(t, x, y, z) = y \\
 \dot{y} &= g(t, x, y, z) = z \\
 \dot{z} &= \delta(t, x, y, z) = -ax - by - cz - x^2
 \end{aligned}
 \tag{4}$$

With respect to above equation the mathematical model of the system using RK4 algorithm is given in equation (5). The parameter  $K, \lambda$  and  $\xi$  in equation (6) defined as the coefficients of the first, second and third equations respectively given in equation (4) and are placed in equation (5) to calculate the  $x(k+1)$ ,  $y(k+1)$  and  $z(k+1)$  which are the values of the system after  $h$  steps. The values  $x(k+1)$ ,  $y(k+1)$  and  $z(k+1)$  are the output of the system after each interval which are used as initial conditions of the algorithm to calculate the values for the next cycle.

$$\begin{aligned}
 x(n+1) &= x(n) + \frac{1}{6}h[k_1(n) + 2k_2(n) + 2k_3(n) + k_4(n)] \\
 y(n+1) &= y(n) + \frac{1}{6}h[\lambda_1(n) + 2\lambda_2(n) + 2\lambda_3(n) + \lambda_4(n)] \\
 z(n+1) &= z(n) + \frac{1}{6}h[\xi_1(n) + 2\xi_2(n) + 2\xi_3(n) + \xi_4(n)]
 \end{aligned}
 \tag{5}$$

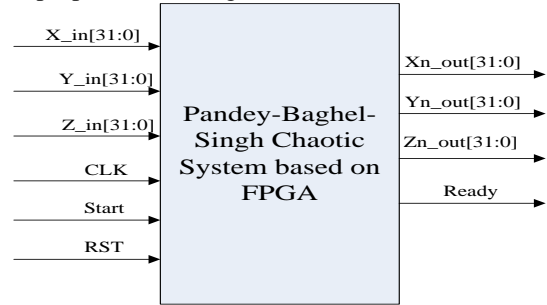
$$\begin{aligned}
 k_1 &= f[x(n), y(n), z(n)] \\
 \lambda_1 &= g[x(n), y(n), z(n)] \\
 \xi_1 &= \delta[x(n), y(n), z(n)] \\
 k_2 &= f[x(n) + \frac{1}{2}hk_1, y(n) + \frac{1}{2}h\lambda_1, z(n) + \frac{1}{2}h\xi_1] \\
 \lambda_2 &= g[x(n) + \frac{1}{2}hk_1, y(n) + \frac{1}{2}h\lambda_1, z(n) + \frac{1}{2}h\xi_1] \\
 \xi_2 &= \delta[x(n) + \frac{1}{2}hk_1, y(n) + \frac{1}{2}h\lambda_1, z(n) + \frac{1}{2}h\xi_1] \\
 k_3 &= f[x(n) + \frac{1}{2}hk_2, y(n) + \frac{1}{2}h\lambda_2, z(n) + \frac{1}{2}h\xi_2] \\
 \lambda_3 &= g[x(n) + \frac{1}{2}hk_2, y(n) + \frac{1}{2}h\lambda_2, z(n) + \frac{1}{2}h\xi_2] \\
 \xi_3 &= \delta[x(n) + \frac{1}{2}hk_2, y(n) + \frac{1}{2}h\lambda_2, z(n) + \frac{1}{2}h\xi_2]
 \end{aligned}
 \tag{6}$$

$$\begin{aligned}
 k_4 &= f[x(n) + hk_3, y(n) + h\lambda_3, z(n) + h\xi_3] \\
 \lambda_4 &= g[x(n) + hk_3, y(n) + h\lambda_3, z(n) + h\xi_3] \\
 \xi_4 &= \delta[x(n) + hk_3, y(n) + h\lambda_3, z(n) + h\xi_3]
 \end{aligned}$$

**C. FPGA Implementation of Autonomous Chaotic Generator**

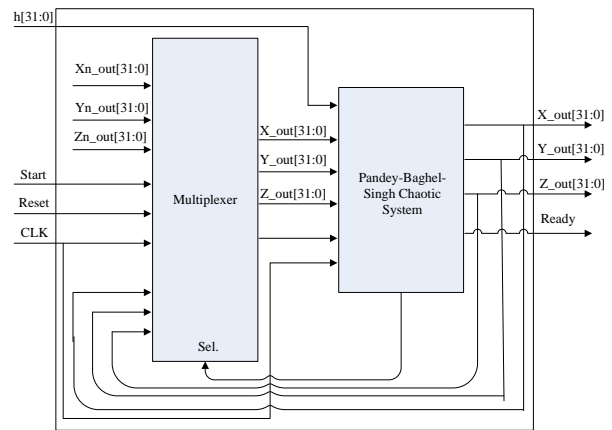
The PBSCS which have been modeled using Euler and RK 4 algorithm are implemented with 32-bit IEEE 754-1985 standard on FPGA. Mathematical modeling is done in

Verilog using Vivado design suite. The Top-level diagram is same for both the models using Euler and RK4 algorithm have been shown in Fig. 3. For the synchronization purpose one bit start, reset and clock signal is used. A 32-bit input has been used and initial conditions are set in the beginning phase. The 32-bit signal are used as input parameter. There is three 32-bit output signals ( $X_{n\_out}$ ), ( $Y_{n\_out}$ ) and ( $Z_{n\_out}$ ) and ready signal is taken as one bit control signals for the proposed chaotic generator.



**Fig.3 Top level diagram of PBSCS based on FPGA**

The second level block diagram of the chaotic generator is presented in Fig. 4 It have one multiplexer and a chaotic generator unit which is FPGA based. The multiplexer is used to provide initial condition signals. For successive operation it is provided by the output signals. When enable is at logic high, the output generates chaotic signal.



**Fig.4 second level design of PBSCS based on FPGA**

The third level block diagram of the Euler based chaotic generator is given in Fig. 5. The system consist of multiplexer, function f, multiplier, adder/Subtractor and filter. The system equations are calculated in the f unit and the output is multiplied by h in the multiplier. In the adder unit previously generated signals by the generators and the signal obtained from the multiplier are added. The filter unit eliminates the undesired signal. The system works sequentially and it generates the first value after the end of 42 clock cycles.

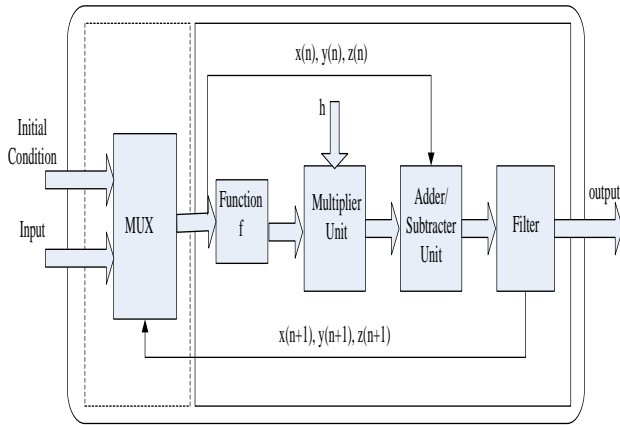


Fig. 5 Third Level design of Euler based PBSCS

The third level block diagram of the RK 4 based chaotic generator is given in Fig. 6. The proposed chaotic generator consist of multiplexer,  $K_s$  units,  $Y_s$  block and filter stage.  $K_s$  units calculate  $k_s, \lambda_s$  and  $\xi_s$  where  $s$  varies between 1 to 4. The  $x(k+1), y(k+1)$  and  $z(k+1)$  given in equation (3) are calculated at  $Y_s$  block. The first value is generated after 142 clock

Pulses and a feedback system is to be employed so that output is feedback to MUX after 142 clock pulses to generate next cycle. Filter unit stops undesired signal to reach output if generator does not generate any result.

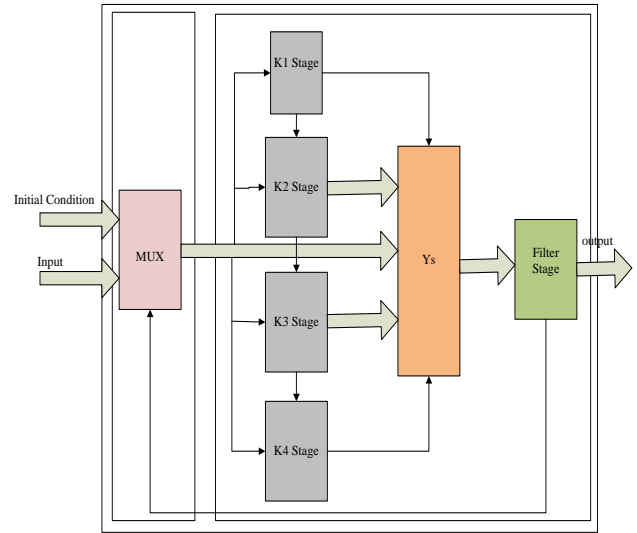


Fig. 6 Third Level diagram of RK 4 based PBSCS

#### IV. SIMULATION RESULTS OF PBS CHAOTIC GENERATOR

The numerically modelled (Euler and RK4) PBS Chaotic generator have been synthesized on Nexys-4 DDR XC7A100TCSG-1 (Artix7) and Basys-3 (Artix7) from the Xilinx vivado v.2017.3 design suite. The simulation results of numerically modelled PBSCS based on Euler and RK4 is presented in the Fig. 7 and Fig. 9 respectively. FPGA chip related Parameters and clock speed of the system for Euler and RK4 is given in fig. 8 and fig. 10 respectively. The summary of the FPGA chip speed and other statistics which are obtained for both the algorithm based system is given in table 1. Euler based chaotic generator gives optimize result with the use of 2181 LUT's and 3907 registers with set clock period 2.78 ns which corresponds to maximum frequency achieved 359.71 MHz. The attracter of the system is generated by the data set are given in fig.11 (a-c) which are similar to PBSCS designed on analog platform.

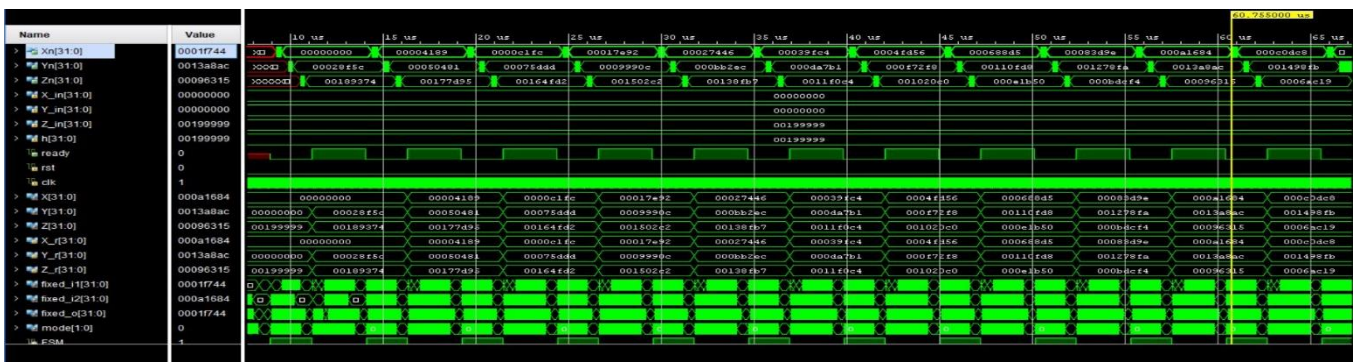


Fig. 7 The simulation results of Euler based PBSCS

# Euler and RK4 Algorithms Based Implementation of Autonomous Chaotic Generator

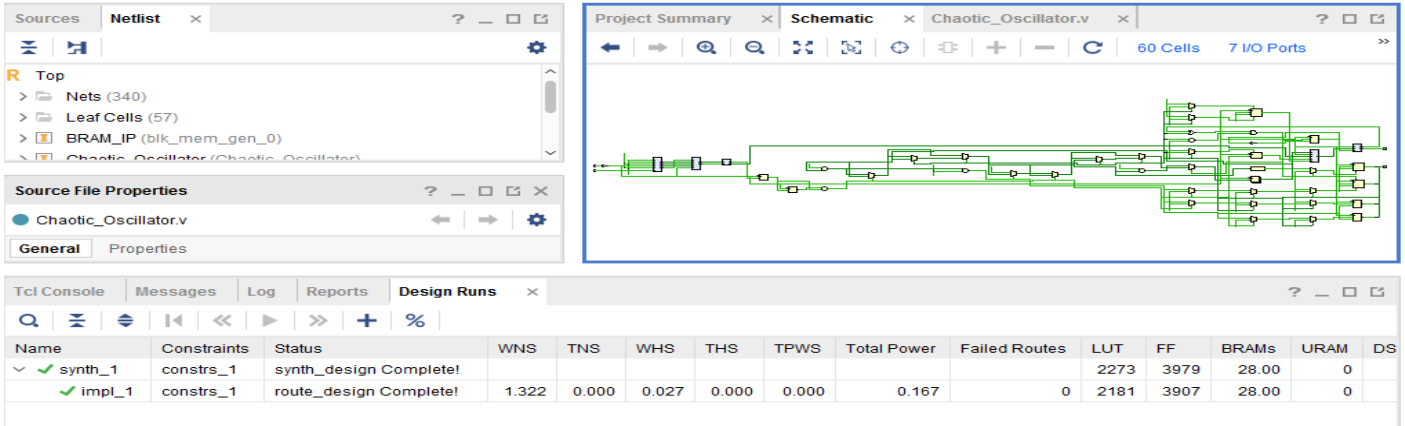


Fig.8 Simulation result of Euler based PBSCS with resource utilization on Vivado 17.3

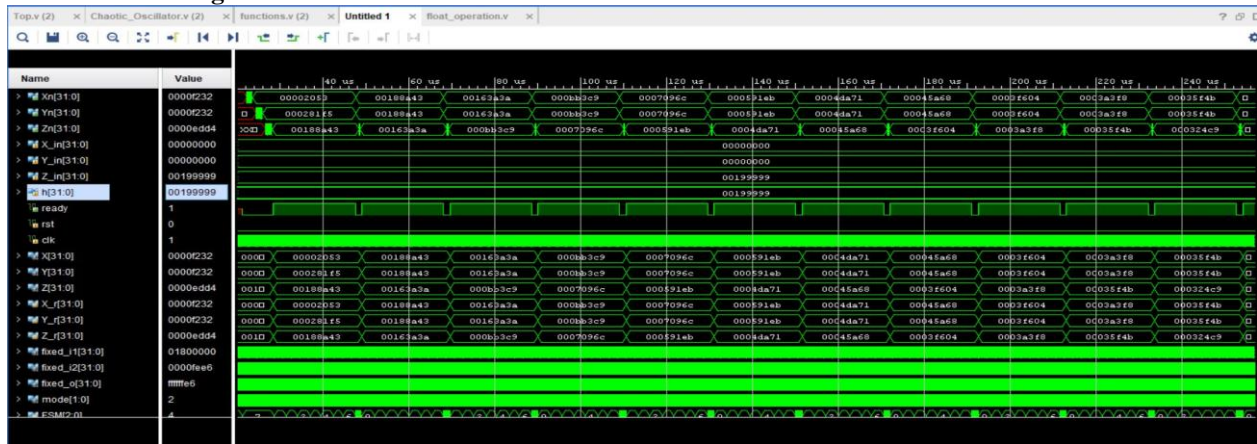


Fig. 9 The simulation results of RK4 based PBSCS

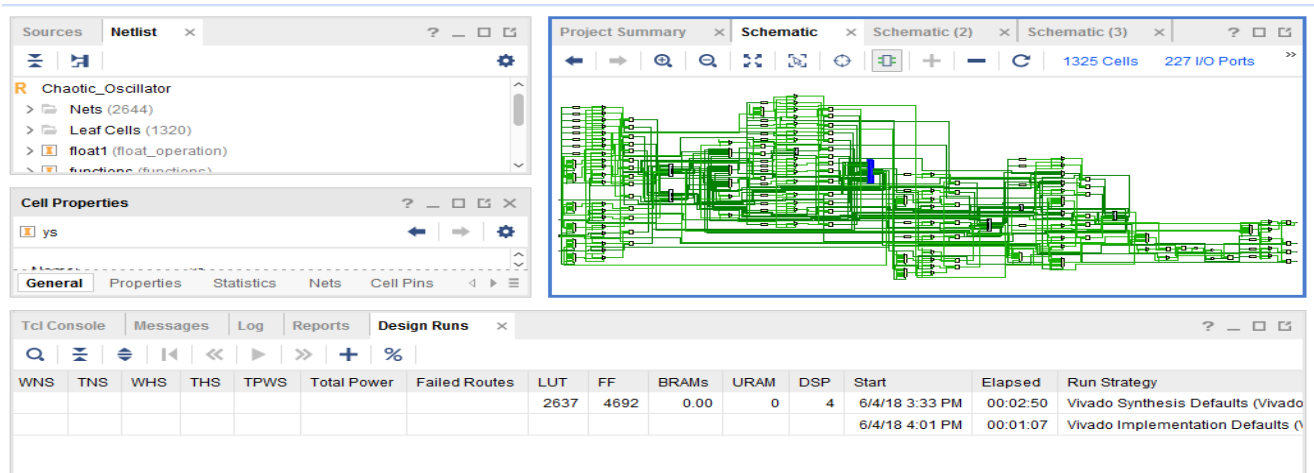


Fig.10 Simulation result of RK4 based PBSCS with resource utilization on Vivado 17.3

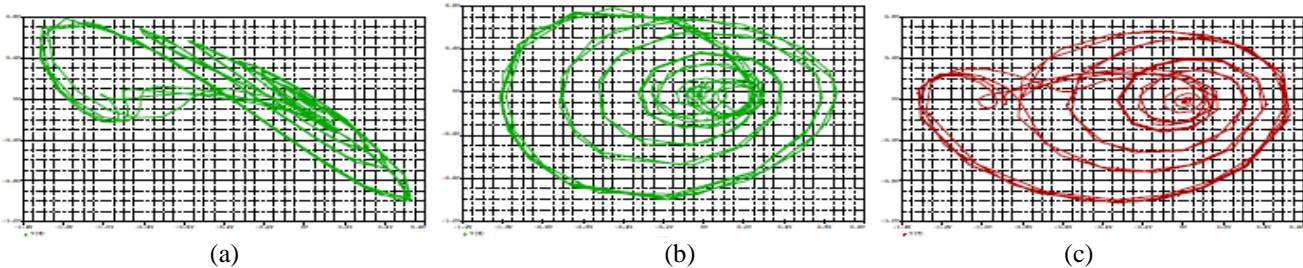


Fig. 11 (a) x-y attractor, (b) y-z attractor, (c) x-z attractor

Table 1: Final report of the resources consumption

Parameter	Euler-based	RK4-based
Maximum frequency (MHz)	359.71	359.71
No. of DSP	2	4
Number of 4 input LUTs	2181	2637
Number of bonded IOBs	32	32
Number of Slice Flip Flops	3907	4692
Total On-chip Power(W)	0.167	0.179



**Dr. Alpana Pandey** is presently working as an Assistant Professor in Department of Electronics and Communication Engineering at Maulana Azad National Institute of Technology, Bhopal, M.P., India, since 2005. She did her B.E. degree from UIT Bhopal and M.Tech and Ph.D. degree from Maulana Azad National Institute of Technology, Bhopal, M.P., India. Her area of research is Chaos communication and Analog and Digital communication including circuits. She has published number of research papers in reputed journals related to this field.

## V. CONCLUSION

The Euler and RK4 based PBS Chaotic generator have been synthesized using the Nexys 4 DDR XC7A100TCSG-1 (Artix7) and Basys3 (Artix7) from the Xilinx vivado v.2017.3 design suite. The Euler based chaotic generator gives optimize result with the use of 2181 LUT's and 3907 registers with set clock period 2.78 ns which corresponds to maximum frequency achieved 359.71 MHz. The attracter of the system is generated by the data set are given in fig. 11 (a-c) which are similar to PBSCS designed on analog platform.

## REFERENCES

1. Ismail K., A. Tuaran O, Ihsan Pehlivan, "Implementation of FPGA-based real time novel chaotic oscillator", Nonlinear dynamics (2014); pp. 49-59.
2. Murat Tunaa, Can Bülent Fidan, "Electronic circuit design, implementation and FPGA-based realization of a new 3D chaotic system with single equilibrium point", Optic Elsevier Optik (2016) pp. 11786-11799.
3. S. Banerjee, J. Kurths, "Chaos and cryptography: a new dimension in secure communications", Eur. Phys. J. Spec. Top., (2014) pp. 1441-1445.
4. I. Koyuncu, A.T. Ozcerit, I. Pehlivan, "An analog circuit design and FPGA-based implementation of the Burke-Shaw chaotic system", Optoelectron. Adv. Mater. Rapid Commun. (2013) pp. 635-638.
5. L. Merah, A. Ali-pacha, N.H. Said, "A pseudo random number generator based on the chaotic system of Chua's circuit and its real time", FPGA Implementation (2013) pp. 2719-2734.
6. S. C, ic, ek, A. Ferikog`lu, I. Pehlivan, "A new 3D chaotic system: dynamical analysis, electronic circuit design, active control synchronization and chaotic masking communication application", Optik - Int. J. Light Electron Opt. (2016) pp. 4024-4030.
7. M. Tuna, I. Koyuncu, C.B. Fidan, I. Pehlivan, "Real time implementation of a novel chaotic generator on FPGA", in: 2015 23rd Signal Processing and Communications Applications Conference (SIU), IEEE, 2015, pp. 698-701.
8. Alpana Pandey, R. K. Baghel, R.P. Singh, "Analysis and Circuit Realization of a New Autonomous Chaotic System", International Journal of Electronics and Communication Engineering. ISSN 0974-2166 Volume 5, Number 4 (2012), pp. 487-495.

## AUTHORS PROFILE



**Dr. Subodh Kumar Pandey** is presently working as Deputy Director in Directorate of Technical Education ,Madhya Pradesh at Bhopal, basically an Associate Professor in Electronics & Communication Engineering, joined teaching as lecturer in 1991 in Government Engineering College Bhopal and worked as Head of Department in UIT, RGPV, Bhopal. He did his M. Tech. in Digital Communication From MANIT, Bhopal and Ph.D. in Electronics & Communication Engineering. His area of research is Chaotic Communication and he has published number of research papers in reputed journals related to this field. He is also a life member of ISTE and IETE.

