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Alarm System based on GSM Network and FPGA using NIOS II Embedded Processor

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Abstract**: *The present work describes how to carry out a text message transmission in a communication system based on GSM network using a NIOS II processor programmed into an FPGA with the objective of controlling a system alarm remotely. A processor interconnects a bus system with electronics components, such as memories and peripherals, integrating them into a chip to demonstrate the potential applications using both wireless technology and embedded processor through a communication module deployed into an educational board for either commercial or academic uses. The implementation of the communication system proposal was through Intel Platform Designer, Intel Quartus Prime, and NIOS II.***

Keywords**: *Alarm systems, GSM, messaging systems, NIOS II.***

I. INTRODUCTION

Different applications approach electronic systems development at a scientific or technical level to enhance processes or access tools that allow improving the environment of those who use them. For example, applications such as alarm systems, necessary to control and warn about the entry of unauthorized people in a determined place, increasing the security in the home and corporate environments.

A technology that is becoming popular among system developers in the implementation of the logical design is FPGA (Field-Programmable Gate Array), which requires configuration or programming to perform a specific instruction. This paper pursues the understanding of basic concepts about GSM communication and FPGA, validating their interconnection through practical examples oriented to magnetic switches and security systems. In this proposal, a surveillance system available throughout the day is designed, allowing the user to have access control to a place by an SMS message (via remote) to take the appropriate actions. The tests shown were carried out in a laboratory environment, with a GSM module for sending SMS messages to a mobile phone along with four magnetic switches to simulate the opening control of a door.

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II. THEORETICAL FRAMEWORK

A. NIOS II Soft Processor

In the development of embedded systems through development environments, the customized configuration of the NIOS II microprocessor system is established (Fig. 1) using a synthesis tool (e.g., Intel Quartus Prime) for direct implementation on FPGA. NIOS II is a 32-bit general-purpose processor that uses separate buses for instructions and data conveying (Fig. 2).

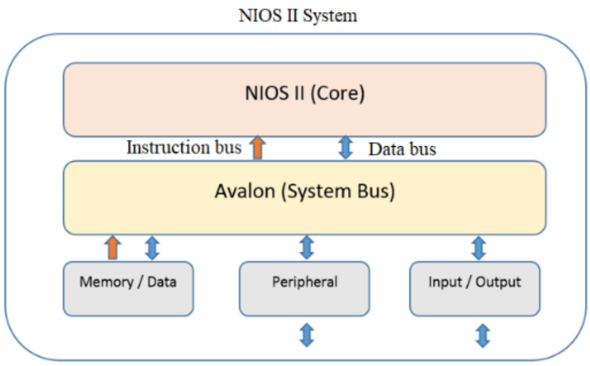


Fig. 1.Microprocessor system based on NIOS II

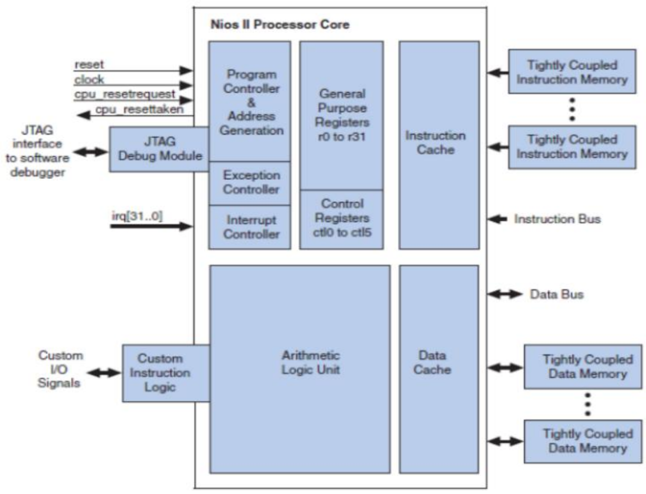


Fig. 2.NIOS II architecture block diagram

Traditionally, FPGAs systems are developed using a hardware description language such as VHDL, Verilog [1][2], or similar. For the NIOS II programming, a tool based on an integrated development environment provides support for applications developed into different languages such as C, C++, or assembler. The configurable nature of NIOS II requires a stage where is defined each one of the system peripherals, assigning a memory address as well [3].

B. GSM network

A GSM network works by digital cells for compatibility with ISDN services, integrating devices that use this technology [4]. Mobile systems operate through cell division for covering larger areas, which are sized depending on the transmission power, i.e., at low power, the higher number of frequencies for transmission. Having frequency availability makes possible conveying by a frequency without interfering to another, in order more users can handle the system.

C. SMS

Short Message Service (SMS) is a communication protocol for exchanging text messages among mobile phones. SMS originally oriented to GSM service, but nowadays is available to other mobile networks, such as 3G [5].

The maximum size of a text message in SMS format is either in 160 characters of 7 bits, 140 characters of 8 bits or 70 characters of 16 bits, the latter in languages such as Chinese, Korean, Japanese, Russian, and Arabic. A segmented SMS is a message that exceeded its maximum character capacity but is sent as chopped, achieved because each segment starts with a User Data Header (UDH) containing information of each segment and its length turning into 153 characters of 7 bits, 134 characters of 8 bits, and 67 characters of 16 bits [6]. The mobile device receives the segments and reassembles each one to show to the user as a long text message.

III. COMMUNICATION SYSTEM

The simplified block diagram of Fig. 3 depicts the interaction between the magnetic switches together with the development/educational board (DE board), in which the NIOS II processor communicates with the mobile network.

Fig. 3.Simplified block diagram

Fig. 4 shows in detail the design, whose purpose is the sending of text messages when a magnetic door-opening switch activates. For the ease of structure, a code based on C integrated the development environment, compiled and executed by NIOS II. An SDRAM memory of the DE board temporarily stores the information. The block of magnetic switches assigns to one of the forty-pin expansion headers. Then, the message for transmission is sent in AT commands through the UART serial port to the voltage converter block, to level the output voltages and be able to communicate with the SIM340CZ GSM module for the message that arrives at the mobile phone.

The software used for computer-aided design (CAD) is the Intel Platform Designer, useful for implementing SoC (System on Chip) systems based on the NIOS II processor in Intel FPGA devices [7] (Fig.5). This software is used with Intel Quartus Prime to implement easy-to-use systems.

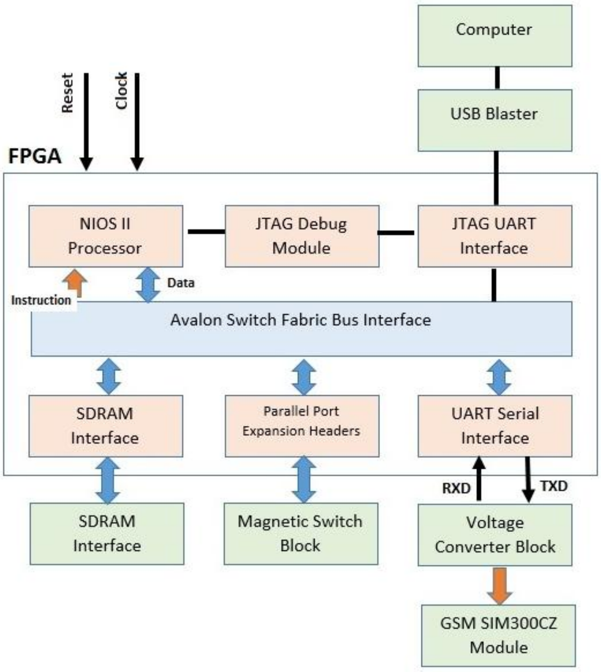


Fig. 4.General block diagram

The Intel Platform Designer has different components, highlighting a NIOS II processor that acts as a central processing unit (CPU), a parallel input/output interface (pio_0), a communication interface with the computer (JTAG UART), and a UART interface for communication with the GSM module via RS232 serial port [8][9].

The parallel input/output interface (pio_0) sets as input for the magnetic switches. Typically, the DE board comes with two 40-pin parallel interfaces, called Expansion_JP1 and Expansion_JP2. In this proposal, we worked only considering one of them, although the interface pio_0 consists of 8 pins used by the magnetic switches. Nevertheless, for simulation purposes, this work only deployed four magnetic switches that identify four pins. Table I depicts the description of the pin assignment with their respective signals.

Table I: Pin assignment description

Signal	Description	Pin location	I/O standard
GPIO_SENSOR[7]	Input	PIN_J20	3.3-V LVTTL
GPIO_SENSOR[6]	Input	PIN_J21	3.3-V LVTTL
GPIO_SENSOR[5]	Input	PIN_F23	3.3-V LVTTL
GPIO_SENSOR[4]	Input	PIN_F24	3.3-V LVTTL
GPIO_SENSOR[3]	Input	PIN_E25	3.3-V LVTTL
GPIO_SENSOR[2]	Input	PIN_E26	3.3-V LVTTL
GPIO_SENSOR[1]	Input	PIN_J22	3.3-V LVTTL
GPIO_SENSOR[0]	Input	PIN_D25	3.3-V LVTTL

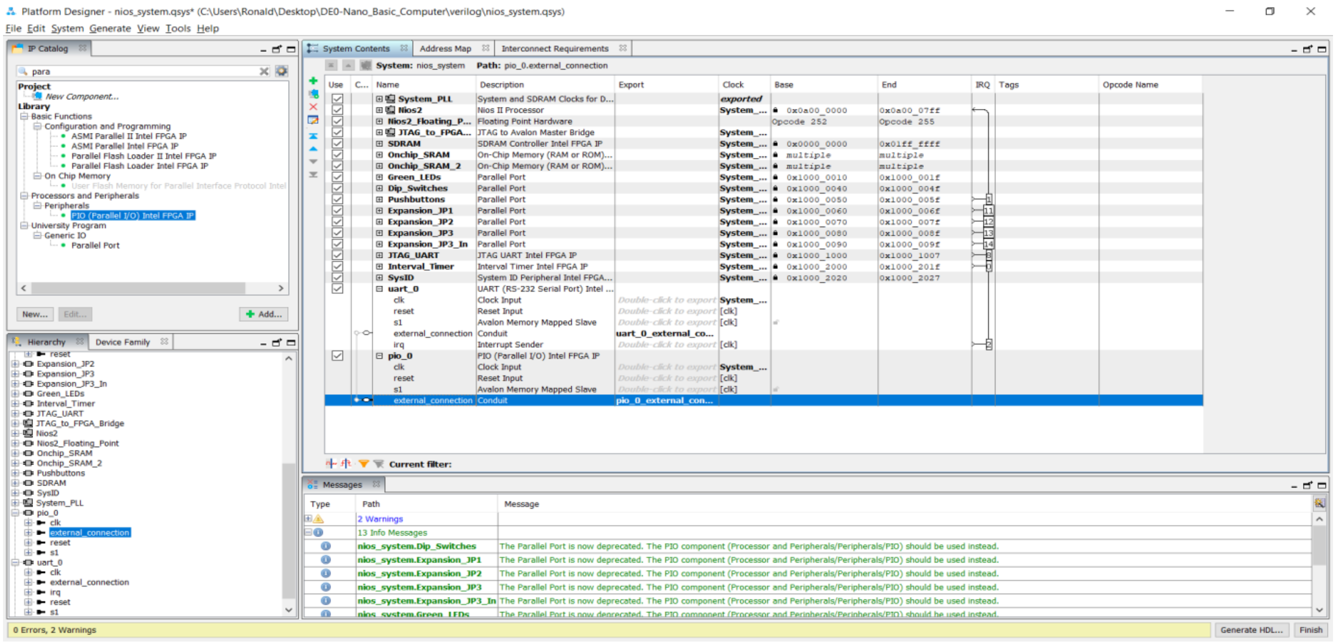


Fig. 5.System configuration by the Intel Platform Designer

The four magnetic switches were deployed into a residence. Eight bits were used, considering only the four most significant ones. A LED lights up in case a magnetic switch activates, as well as the function where the message conveys via AT commands to the mobile phone.

A. Block of magnetic switches

These sensors perform as a switch (0-1), placed in doors and windows. Their operation is similar to a keypad in negative logic: when connecting the terminal of the sensors, a short circuit sends a low voltage level, i.e., a logical zero, determining which windows and doors close. On the other hand, when the terminals of the switch are separated, the circuit sends a high-level voltage, i.e., a logical one, determining which windows and doors open and if someone gets into the place. Table II depicts the magnetic switches technical features.

Table II: Magnetic switch features

Switch	Closed (Typical values)	Open (Typical values)
With energy contact	10W	3W
Current	0.5A	0.2A
Voltage	100V	30V
Initial resistance	200Ω	-
Action distance	18-23 mm	20-25 mm

B. Voltage converter block

To perform the communication between the DE board and the SIM340CZ GSM module is necessary to work at the same voltage level and setting a DTE-DCE configuration. Thus, the use of a voltage converter allows to transform the RS-232 signal into TTL. In RS-232 a logical "1" equals to -15V and a logical "0" equals to + 15V. At the moment of working with a +5V power supply for the GSM module and the converter, this value references a positive logic level and the value of 0V represents a logical zero.

C. SIM340CZ GSM module

The SIM340CZ GSM module operates in four frequency bands (850/900/1800/1900MHz) with a performance for voice, SMS, data and fax at low power consumption [10]. Once the security compromises, this module will send text messages to the mobile phone, based on the commands executed by the NIOS II processor. The commands sent are AT type by UART communication between the processor and the module. Table III shows the pins used with their respective descriptions.

Table III: SIM340CZ GSM module pin features

PIN	I/O	Description	DC features
VBAT	-	For voltage source. Typically, a current transmission of 2A. These pins are for the input voltage	Vmax=4.5V Vmin=3.4V Vnormal
GND	-	Digital ground	-
PWRKEY	I	Input low voltage by pulse. To turn on or turn off the system. The system needs a time margin to normalize the software	VILmax=0.3*VBAT VIHmax=0.7*VBAT Vimax=VBAT
RXD	I	For data reception	-
TXD	O	For data transmission	-
DTR	I	Data Terminal Ready, for controlling RS-232 serial communications. Transmitted via DTE-DCE.	-

D. Communication process

The four magnetic switches configured in negative logic simulate a closed door. The switches communicate to the DE board through a data bus connecting to the pins (pio_0). If a magnetic switch opens, the board receives a high voltage value. Depending on which switch opens, the signal conveys to the respective pin and the board recognizes the activated pin. In this proposal, the board is programmed to light up the LEDs after identifying which sensor activates, e.g., if switch 1 activates, the board turns on the LEDs representing the number one in binary. Fig. 6 depicts the proposal connection scheme.

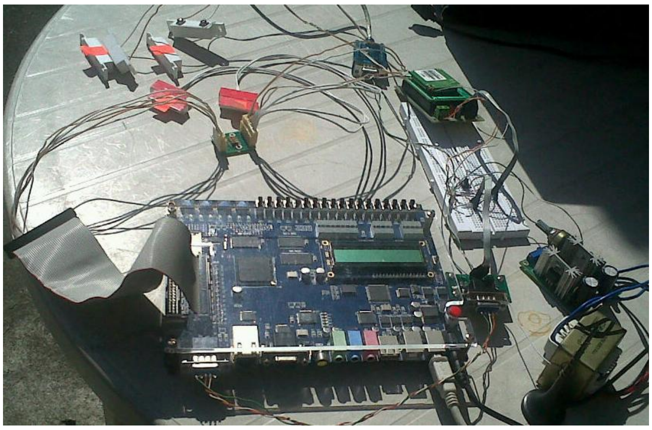
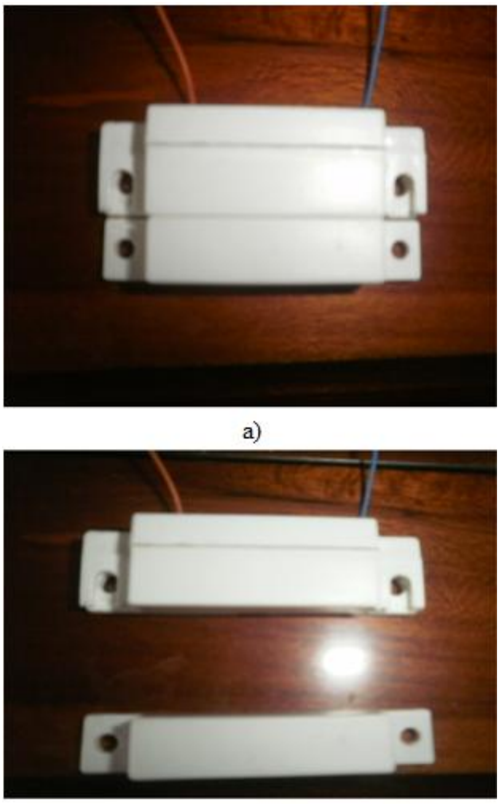


Fig. 6.Proposal schema



a)

b)

Fig. 7.Magnetic switch position

IV. TESTS AND RESULTS

This section shows the tests performed, which include the presentation on the computer screen through the access port, observing the communication between the DE board and the GSM module, with commands sent to the GSM module for the sending of the text messages to the mobile phone.

For the transmission of the text message to a mobile phone is important to consider the optimum signal level for the communication process. To attain it, the AT + CSQ command runs for reporting the signal quality, returning the received signal strength indicator (RSSUI) and the bit error rate (BER) from the mobile device. Table IV shows the parameter values.

Table IV: AT+CSQ result parameters

Parameters	Values	Description
RSSI	0	-113 dBm or less (min)
	1	-111 dBm
	2 to 30	-109 to -53 dBm
	31	-51 dBm (max)
	99	No detectable (no signal)
BER	0 to 7	RXQUAL values
	99	No detectable (no signal)

For the tests, each of the four doors has a magnetic switch. If the magnetic switch closes as in the inactive state (Fig. 7a), the DE board will not receive any signal. At the moment the first door is opened, the magnetic switch separates (Fig. 7b). The DE board shows on the LEDs the binary 1, assuring the respective magnetic switch turns on (Fig. 8), recognizing the activated switch and sending the respective AT command to the module through the RS-232 serial port, connected between the DE board and the module. The communication between the board and the GSM module can be seen on the computer screen by the access port (Fig. 9). When the door opens, the user receives a message in his/her mobile phone (Fig. 10).

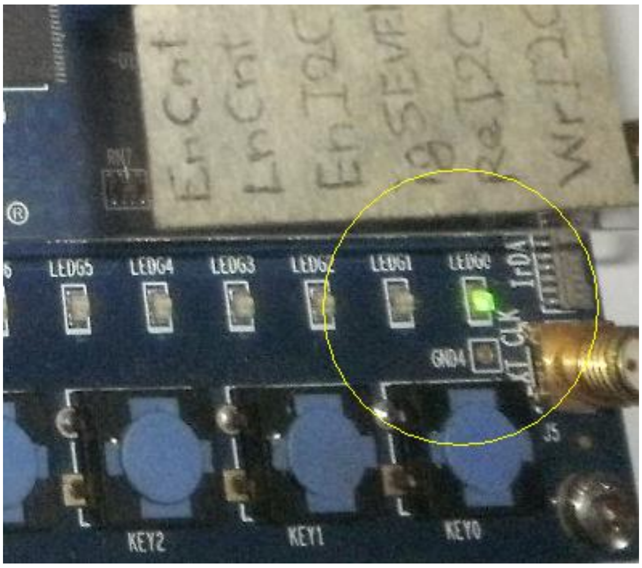


Fig. 8. LED depiction of a opened magnetic switch

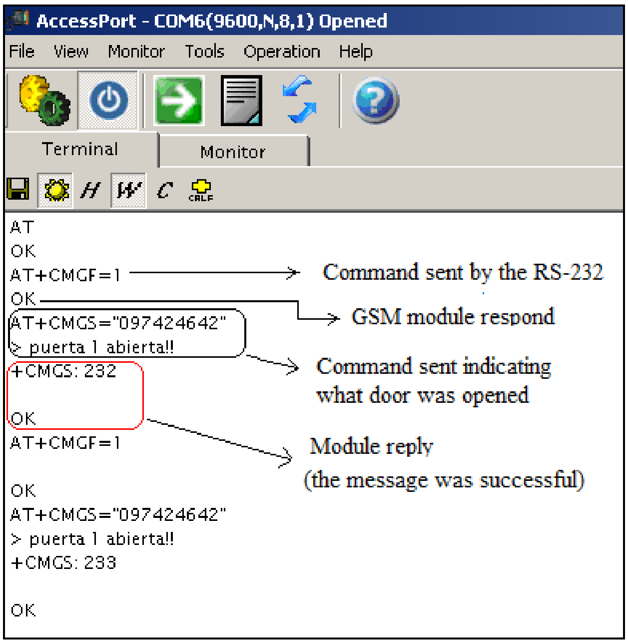


Fig. 9. Access port results

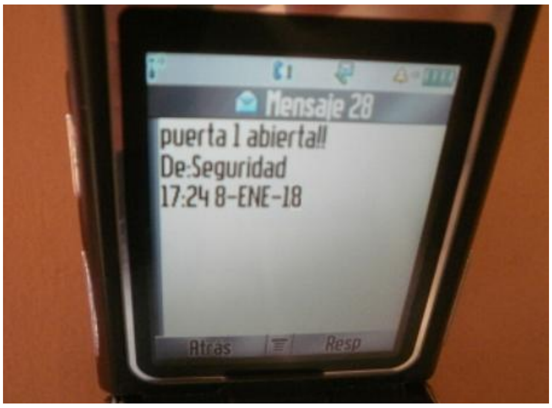


Fig. 10. SMS for alerting a door opening

V. CONCLUSIONS

This paper shows one of the several applications in which wireless technology works together with FPGA, through a module that communicates with a DE board. The ease of understanding and development is an advantage when using C programming language, verifying that a high-level language is useful for hardware level implementations.

Although the door opening magnetic switches were useful throughout the development of the project, other external sensors can detect either motion, heat or sound, since the DE board only needs a voltage level (high or low) turned into a logical signal for responding to changes in the system. Moreover, several devices can connect to an FPGA by multiple memory stacked, providing higher memory bandwidth, better internal memory controller, and enhanced multiple links. FPGA can work interfacing real scenarios providing a variety of benefits, such as low power consumption and low latency. We realized that the GSM network was reliable for the transmission of several applications at security level by a GSM module that received specific AT commands through the DE board that performs as a controller system.

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