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Improvement of Power Factor by Input Filter and Ripple Reduction using Cuk Converter in Continuous Conduction Mode

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Abstract*: *The basic Converters like buck, boost and buckboost provide pulsed ripple currents either on input or output sides. A Cuk Converter has inductors on both input and output sides, thus produces continuous currents with reduced ripple. By extending the Cuk Converter to AC side with the support of additional rectifier circuit the power factor can be assessed. The significant concerns when utilizing DC-DC converters with AC source is large Total Harmonic Distortion (THD) and low power factor. A properly designed filter circuit on AC side reduces THD and improves the power factor. In this paper a Cuk Converter (CC) topology with rectifier and inductive. capacitive. inductive (LCL) filter is proposed to reduce THD and improve the power factor. The CC circuit is designed and analyzed to reduce ripple content of currents. The reduction in ripple on DC side in turn improves the sinusoidal shape of current on AC source side. The closed loop simulation of the proposed circuit is carried out using a systematically derived type III compensator. The proposed circuit is practically validated in closed loop using FPGA controller to confirm the simulated waveforms. The results substantiate the fact that the proposed circuit shrinks ripple on DC source side and reduces harmonics of AC source current. The reduction in harmonics decreases THD to a large extent and improves distortion factor, which enhances the power factor. Also the reduction in ripple trims down losses in the circuit and improves the output power, thus suitable for DC to DC conversions in power supplies for viz. electric vehicles, computers, battery chargers and televisions. The improvement in power factor reduces the power drawn from the source and hence the efficiency of the system is improved.

***Keywords* : *Cuk Converter, Filter circuit, Harmonic distortion, Power factor* improvement, *Reduced ripple* .**

I. INTRODUCTION

Ripple current generated by basic DC-DC converters causes for harmonics and it increases Total Harmonic Distortion (THD) on AC side. The large amount of ripple on DC source current distorts the shape of AC source current and affects the quality of power adversely. Low ripple on source current has been an adequate requirement when these converters are largely utilized for various applications.

The buck converter is added with two winding transformer circuit and power conditioning circuit [1], [2] to reduce ripple on output voltage. The series connected capacitor decreases the ripple contents to zero. The cascaded SEPIC-buck converter [3] consists of two power conversion stages, which not only improves the voltage gain and but also reduces ripple content of source and output currents. A zero voltage switching with phase shift control technique [4] is used to reduce circulation current and the reduction in switching losses improves the efficiency. In these circuits the analysis and troubleshooting become complex due to versatile circuit with number of energy storage elements and switches. The high gain soft switching circuit [5] and multiplier circuit [6] are used with step-up converter to improve output voltage. The switches are operated by resonant zero voltage to trim-down the switching losses. The boost converter with parallel circuit [7] produces dual output voltages and reduces ripple content of the source current. The output losses are reduced in these circuits but challenging transient characteristics are instigated by switched capacitors. The LCL filter used in bidirectional DC-DC converter [8] reduces the current harmonics and controls soft switching of the devices.

The buckboost converter with switched capacitor logic [9] circuit trims down source current ripple irrespective of duty ratio for wide range of operations. The addition of complex capacitor - inductor circuit [10], [11] in buckboost converter, achieves high voltage gain compared to all basic converters. The continuous source current developed along with high voltage gain in buckboost –SEPIC circuit [12] eliminates large filtering requirement on Source AC side. Though the PWM switching scheme is easy in these circuits but the modelling and systematic analysis become complex. Cuk design with moving filter circuit in digital control law [13], bridgeless current sharing circuit [14], [15] is used to improve power factor to unity. The current control circuit smoothens the shape of input current. The gain of the Cuk design is increased by inserting additional boost circuit [16] as an interleaved inductor structure. The THD of the circuit is decreased by inserting diodes with Cuk design [17] in continuous mode, thus the power factor is improved. The even harmonics are addressed with the LCL filter circuit used with grid connected inverter [18] for renewable energy applications. The weight of the core is reduced in the design with delta connected yoke in three phase grid connected inverter [19] circuit using LCL filter.

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The harmonics in source current is reduced by controlled rectifier circuit [20] - [22] with help of LCL filter design. The complexity in the supplementary control and power circuit is increased, which leads to additional cost.

A Cuk converter consists of inductors on both input and output sides, which generate continuous current.

The reduced ripple current decreases the size of filtering requirement when the converter circuit extended to AC side. A Cuk Converter with LCL filter and rectifier circuit in closed loop along with type III compensator is proposed in this paper to reduce ripple on DC side and hence to enhance power factor on AC side.

II. CUK CONVERTER (CC) TOPOLOGY

The circuit of CC transfers DC input voltage to another DC with opposite polarity. The circuit diagram of practical CC is shown in Fig. 1. The energy transfer is based on storage of power in intermediate capacitor C1. The duty ratio of the switch S1 is varied to produce buck and boost output voltage. The circuit consists of inductors on both input and output sides, which reduces ripple content on DC source and output currents compared to all basic buck, boost and buck boost topologies. Reduction in ripple decreases associated conduction losses in the circuit and increases the output power. The CC topology produces negative output voltage and current, thus the output power is positive and hence the converter works in third quadrant.

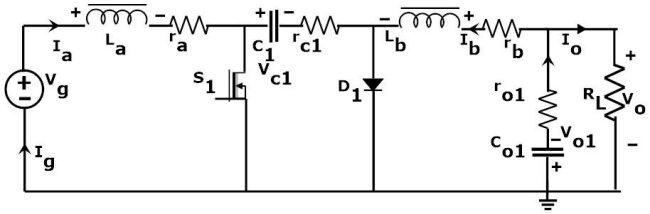

Fig.1: Practical CC topology

III. PROPOSED CUK CONVERTER CIRCUIT WITH LCL FILTER AND RECTIFIER

The circuit of CC is extended AC side by adding rectifier and LCL filter to make analysis of THD and power factor. The proposed circuit of CC with LCL filter and rectifier is shown in Fig.2. The circuit is operated to develop constant output voltage against input line voltage and output load current variations using a designed type III compensator. The transfer function of the compensator is modelled in MATLAB for simulation and emulated in FPGA controller for hardware to provide constant output voltage in closed loop.

The continuous conduction mode of operation of the CC topology develops DC source current with low ripple which smoothens its shape. A symmetrical current is obtained on the AC side without filter circuit. The even harmonics are eliminated in the source current by the definition of Fourier analysis for symmetrical shape. The designed LCL filter inserted in the circuit improves the shape of AC source current more sinusoidal. The LCL filter is utilized also to reduce amplitude of odd harmonics and the THD, which improves distortion factor and hence the power factor.

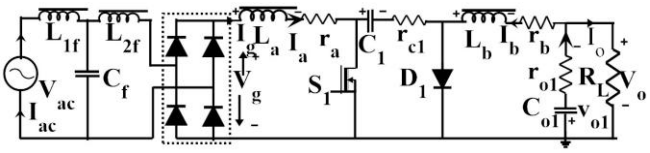

Fig.2: Proposed diagram of CC with LCL filter and rectifier

The improvement in power factor decreases the power drawn from the AC source. Hence the rise in output power (explained in section II) and diminution in input power improves the efficiency to high.

A. *Principle of Operation*

The AC power is applied to the rectifier circuit through a LCL filter circuit. The rectified DC is connected to the input of the CC circuit. The converter circuit produces higher or lower output voltage compared to its input according to duty ratio in opposite polarity. The operation of CC circuit is explained in two intervals.

B. *Interval 1: Switch S_1 - ON Position*

The circuit diagram in Fig.3 shows the CC with switch in ON position and diode in reverse bias. As the switch is closed the inductors L_a and L_b are charged and Capacitors C_1 and C_{o1} are discharged. The stored energy in capacitor C_1 is transferred to load through the discharging path S_1 and R_L. The ripple current through the DC source current is evaluated as follows.

From Fig. 3, assuming linear rise of inductor current, the ripple current through inductor L_a for the switching period T_S is given by (1),

$$\Delta_{ia1} = \frac{2 \times \sqrt{2} V_{ac} \times d \times T_s}{L_a \pi} \qquad (1)$$

where V_{ac} and d respectively are input AC RMS voltage and duty ratio of switch. The ripple current can be controlled by varying ON time against constant input voltage.

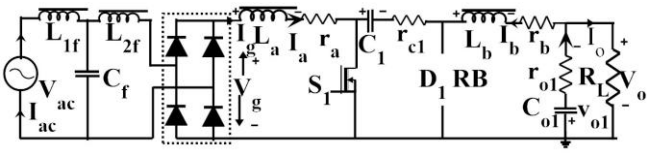

Fig. 3: Proposed diagram of CC with LCL and rectifier when switch in ON position (D_1 RB : Diode reverse biased)

C. *Interval 2: Switch S_1 - OFF Position*

The circuit diagram in Fig.4 shows the CC with switch in OFF position. In this interval switch is opened, the inductors L_a and L_b are discharging and Capacitors C_1 and C_{o1} are charging. The stored energy in the inductor L_a is transferred to energy storage capacitor C_1 and hence it is charging. The capacitor C_1 is charging through the diode.

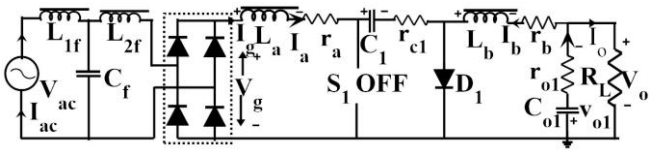

Fig. 4: Proposed diagram of CC with LCL and rectifier when switch in OFF position

From Fig. 4, assuming linear fall of current, the ripple current through inductor L_a is given by (2),

$$\Delta_{ia2} = \frac{\left(2\times\sqrt{2}V_{ac} - V_{c1}\times\pi\right)\times(1-d)\times T_s}{L_a\pi} \qquad (2)$$

where V_{c1} is voltage across capacitor C_1. The ripple current depends on difference in voltage and OFF time of the switch.

D. *Output* Voltage Equation

The output voltage equation of practical circuit of CC with rectifier can be derived by applying volt-second balance to energy storage inductors.

Applying volt-second balance to inductor L_a in Fig.3, Fig.4 and the V_{C1} is given by (3)

$$V_{c1} = \frac{2\times\sqrt{2}V_{ac}}{\pi} - I_a r_a - I_a r_{c1}(1-d) \qquad (3)$$

Also applying volt-second balance to inductor L_b in Fig.3, Fig.4 and the V_o is given by (4)

$$V_o = -V_{c1}d + I_b r_b + I_b r_{c1} d \qquad (4)$$

Substituting (3) in (4) and the output voltage is given by (5),

$$V_o = -\left[\left(\frac{d}{1-d}\right)\left(V_g - I_a r_a\right) - \left(I_a + I_b\right) r_{c1} d - I_b r_b\right] \qquad (5)$$

Thus it turns out that the output voltage can be varied by changing duty ratio of switch, by keeping input voltage constant.

IV. DESIGN OF COMPENSATOR

The stability of the closed loop system is verified by voltage mode control by designing a type III compensator. To design a compensator a state space averaged model [23] is constructed as given below,

$A = A_1 * d + A_2 * (1-d)$
$B = B_1 * d + B_2 * (1-d)$
$C = C_1 * d + C_2 * (1-d)$

where A_1, B_1, and C_1 are state matrices when the switch S_1 is in ON position in Fig.3. Similarly, A_2, B_2 and C_2 are also state matrices when the switch S_1 is in OFF position as in Fig.4. The matrices A, B and C are the averaged state space matrices. Applying small perturbations [24] bound to the steady state duty ratio d and the perturbed output voltage is given by (6),

$$v_o(s) = C\left(sI - A\right)^{-1}\left[A_1 - A_2\right) X\, d(s) \qquad (6)$$

where $v_o^{\wedge}(s)$ and $d^{\wedge}(s)$ are small ac variations of output voltage and duty ratio. The CC is designed [25] for 100W to realize practically and the component and parameter values are tabulated in Table I.

Table I: Designed component and parameter values for CC topology for an output power of 100W with resistive load

Component	L_a	L_b	C_1	C_{o1}
Values	0.75mH	0.5mH	10 µF	10 µF
parameter	V_g	V_o	f_s	I_o
Values	20V	-50V	25kHz	-2A

The designed values of Table 1 are substituted in state matrices and they are further inserted in (6) to form the small signal transfer function for the converter. The plant transfer function for the 100W output, multiplied with the gain of the FPGA modulator, is given by (7),

$$G_p(s) = \frac{18.2s^3 + 1.82*10^8 s^2 - 3.5*10^{11} s + 6.3*10^{15}}{s^4 + 430s^3 + 3.2*10^7 s^2 + 1.1*10^{10} s} \qquad (7)$$

The bode plot of the transfer function investigated to check the stability of the plant, which is shown in Fig. 5. The phase margin of the plant CC is very low and gain margin is negative. So in order to make the closed loop system stable, suitably investigated different type of compensators. Finally, a type III compensator is designed and tested in frequency domain. The compensator transfer function is converted to discrete z-domain with a sampling time of 20 nano seconds to use with digital controllers. The converted transfer function in z-domain is given by (8).

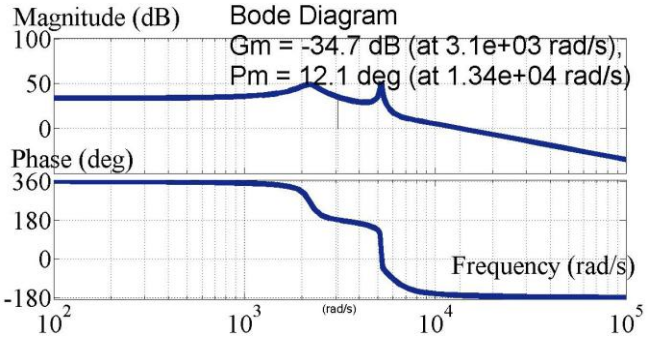

Fig. 5: Bode plot of the plant, phase margin =12.1°

$$G_c(z) = \frac{0.004z^2 - 0.008z + 0.004}{z^3 - 3z^2 + 3z + 1} \qquad (8)$$

The convolution plant and compensator transfer function, both in z-domain yields compensated overall transfer function. The bode plot of the overall transfer function in closed loop system is plotted and shown in Fig.6.

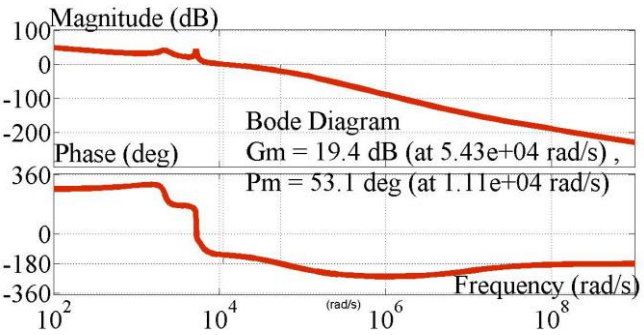

Fig. 6: Bode plot of the compensated system, phase margin = 53.1º.

From the bode plot it has observed that the phase margin of the compensated overall system is 53.1º. and the gain margin is 19.4 dB, thus the closed loop system is stable.

V. POWER FACTOR CORRECTION

The power factor of the CC with rectifier is improved by designing a LCL filter on the AC source side. The filter capacitor C_f must be designed first to optimize the size of filter inductors. The capacitance C_f is evaluated [22] by (9),

$$C_f \le 0.01\frac{P}{2\pi f * V_{ac}^{\ 2}} \qquad (9)$$

The designed maximum value of capacitance is 10µF, for the following values, Power P = 150W, V_{ac} =22V, and f= 50Hz. Also the filter inductors are selected [22] according to (10).

$$f_c = \frac{1}{2\pi}\sqrt{\frac{L_{1f}+L_{2f}}{L_{1f}L_{2f}C_f}} \qquad (10)$$

where the corner frequency f_c is assumed as 1.25kHz for a switching frequency of 25kHz, filter inductors L_{1f} and L_{2f} are assumed equal. So the inductors are selected as L_{1f} =L_{2f} = 3.3mH according to (10). The power factor of the entire system is given by,

$$pf = \cos\phi\frac{I_{ac1}}{I_{ac}} \qquad (11)$$

where pf be the power factor, I_{ac1}, I_{ac} and cosϕ respectively are the line frequency (50Hz) component of AC input current, the RMS value of AC input current and the displacement factor. The THD of the AC input current is given by (12),

$$THD(\%) = \sqrt{\frac{I_{ac}^{\ 2} - I_{ac1}^{\ 2}}{I_{ac1}}} * 100 \qquad (12)$$

The power factor of the entire circuit CC with LCL filter can be improved by the reduction of THD. The capacitor C_f play major role in the reduction of THD. Hence it is taken as designed maximum value.

VI. SIMULATON RESULTS

The simulation of the circuit of CC with rectifier and LCL filter in closed loop is carried out with the designed filter values and the values of components as in Table 1. The simulation has carried out to produce a DC output of 100W with an AC input voltage of 22V. The output voltage is compared with the reference value and error is processed in type III compensator to generate DC control signal. The PWM is produced by comparing control signal with triangular carrier signal and the switch S_1 is triggered.

The Fig. 7 shows DC output voltage and its derived DC input voltage waveform. The output voltage observed as -50V

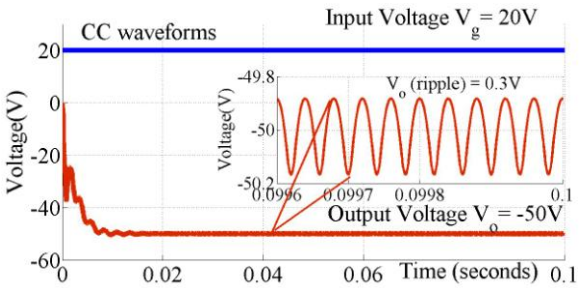

Fig. 7: Output voltage V_o =--50V, Input V_g=20V, Output voltage ripple $V_{(o\ rip)}$=0.3V

for a DC input of 20V which is derived from AC source of 22V. The output voltage has a ripple of 0.3V, which is 0.6% only. Also the output current has the same amount of ripple only.

The DC source and output current waveforms are shown in Fig. 8. The DC current drawn from the AC source is 5.4V at

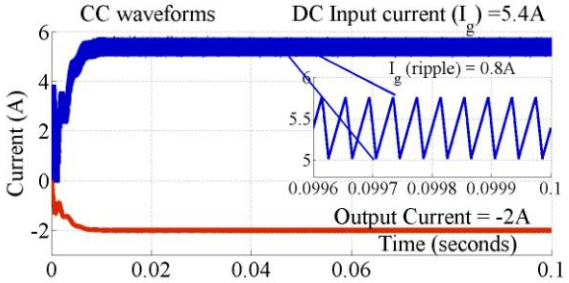

Fig.8: DC input and output current waveforms, I_g=5.4A, I_o = -2A, $I_{(g\ rip)}$ = 0.8A.

at 20V DC input to produce an output voltage of -50V at -2A. The efficiency at rated load is evaluated as 93%. The DC input current ripple is 0.8A which is 15% of the input current. The selection of inductor L_a controls the ripple content on source current. The ripple content on source current is less compared to basic converter topologies.

The closed loop operation of the converter provide constant output response irrespective line and load transients, as the converter is regulating output voltage. The line transient is shown in Fig. 9.

An input Dc voltage variation from 16V to 24V is applied at 50ms. The output voltage changes in response to changes of input. The error is processed in type III compensator and it produces control voltage to regulate output to -50V. The output voltage settles before 60ms with a settling time less than 10 ms.

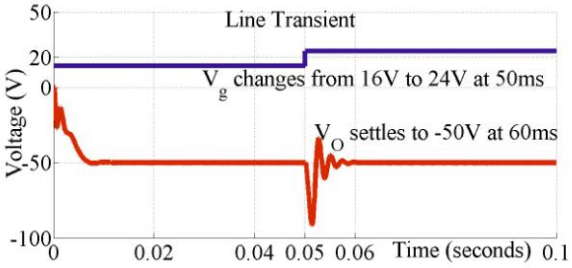

Fig. 9: Transient waveform: Output voltage is controlled back to -50V with a settling time of 10ms after the line transient.

Similarly load current change is applied to observe the output voltage variations and Fig. 10 shows load transient waveform. The load current is varied from -1A to -2A at 50ms

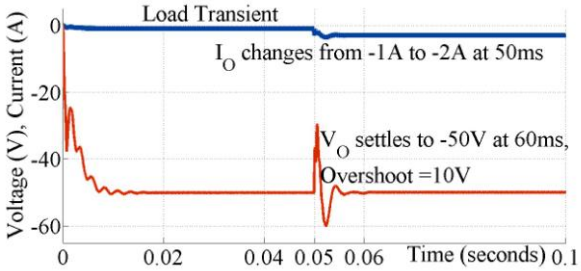

Fig. 10: Load transient: Output voltage settles to -50V after the transient current change from -1A to -2A.

The output voltage responds to the change; the feedback system works abruptly. The voltage settles to -50V after a small dip and rise with a settling time less than 10 ms.

The power factor is measured by observing AC source current and voltage waveforms. The Ac source voltage, AC source current, power factor and THD are plotted in Fig. 11. The input AC side voltage and current are measured for a rated load current of -2A at the output in continuous conduction mode of inductor current, which is shown in Fig. 11 (a). The line voltage and line current coincides at zero crossing and the also the line current is symmetrical about time axis. So the even harmonics are absent by the definition of Fourier analysis. Only odd harmonics are present, which are eliminated by LCL filter circuit. The THD of the line current is 3% as shown in Fig. 11(b). The THD measured is very low, the line current is sinusoidal, thus the distortion factor and displacement power factor are high. Hence the power factor measured is high, which is equal to 0.98. The input power factor is high and hence the power drawn from the source is low.

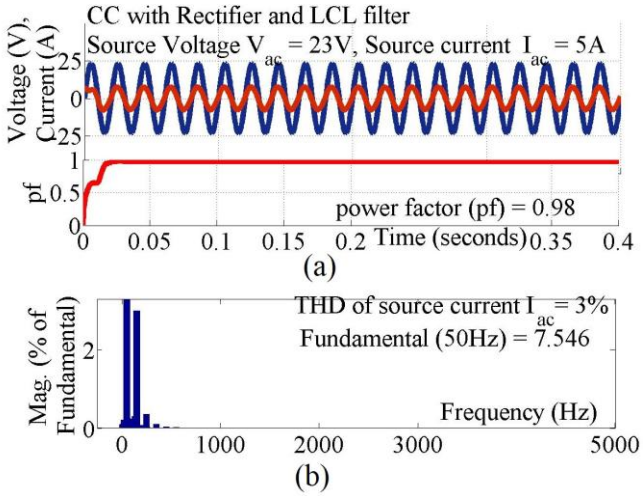

Fig. 11: (a) AC source voltage (blue color), AC source current (red color) and power factor (b) THD of source current is 3%.

VII. EXPERIMENTAL VALIDATION

The closed loop block diagram for practical validation is shown in Fig. 12. The output voltage is scaled down by potential divider circuit and applied to ADC of FPGA controller. The digital response is compared with reference value and error is processed in the type III compensator, which is emulated in XILINX tool of FPGA controller. The compensator output is compared with modelled triangular

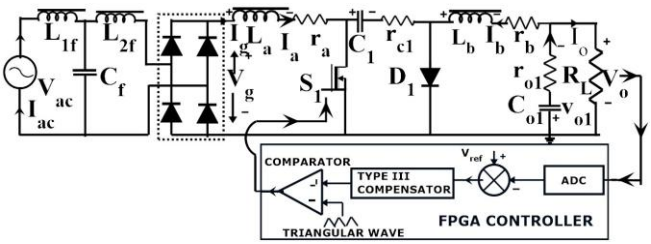

Fig. 12: Practical Circuit of CC with LCL filter and rectifier in closed loop.

repetitive signal and the PWM is generated with the controlled duty ratio.

The photo of hardware implementation is shown in Fig. 13. The source, CC board, LA55P current sensor board, XILINX Spartan – 3AN FPGA Altium Nano Board, DSO, meters etc. are shown in the Fig. 13.

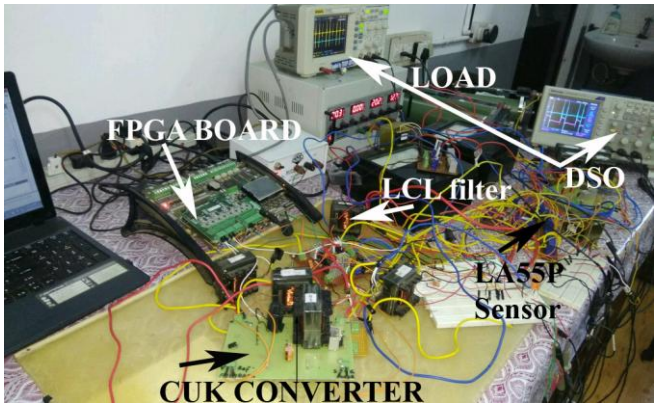

Fig.13: Photograph of CC circuit with LCL filter

The output voltage and input voltage are measured using 100 MHz DSO and is shown in Fig. 14. A DC voltage of 20V is

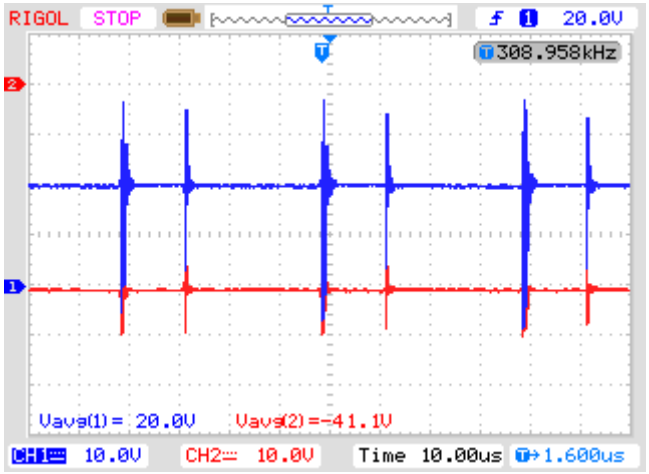

Fig. 14 : DC Input (blue) and output (red) voltage of CC

applied to CC and the output voltage is measured in closed loop is -41V. The ripple on output voltage is very low and is 1V

The DC source current and output current are shown in Fig.15. The source current of 4.62A is measured on DC side

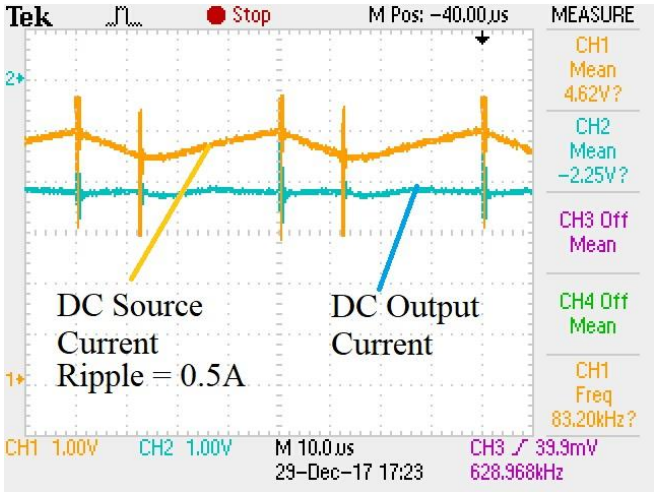

Fig. 15: DC side source current =4.62A and load current = -2.25A. (Sensor Scale 1V =1A)

for an output load current set to -2.25A. A LA55P current sensor is used to measure the current and it is scaled as 1V = 1A. The output voltage is set to -40V. The ripple on DC side source current is measured as 0.5A which is 11% of DC source current. Hence the CC circuit produces less amount of ripple compared to other basic DC-DC converters, the conduction losses are reduced. Hence the output power is increased.

The sinusoidal AC side voltage of 22V is applied through the LCL filter and source AC current is measured. The source voltage and current are shown respectively in Fig. 16. and Fig. 17.

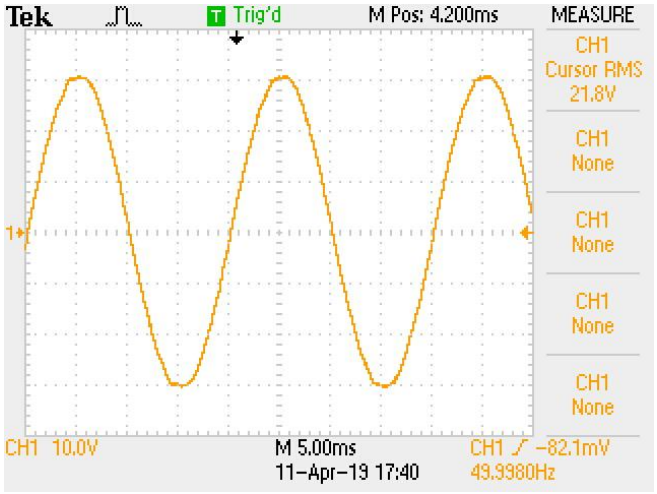

Fig.16: Source voltage = 22 V RMS

The AC source current measured using power quality analyzer against an input source voltage of 22V RMS. The load current measured is -1.3A, at -41V and the source current is observed as RMS value of 2.73A. The AC source current is symmetrical about independent axis.

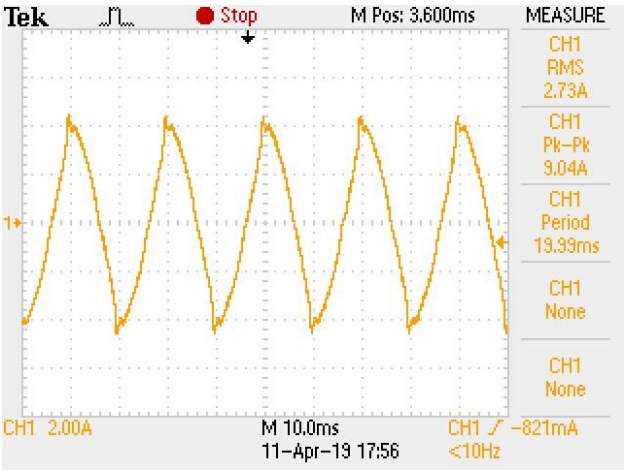

Fig. 17: The AC source current measured is 2.73A

The THD of the source current is shown in Fig. 18. It can be observed that all even harmonics are absent due to symmetry of the waveform., which corroborate with mathematical Fourier analysis. Hence the symmetrical source current has only odd harmonics and the THD is measured as 6.1%. Low value of THD indicates that the power factor is high, which reduces the power drawn AC source.

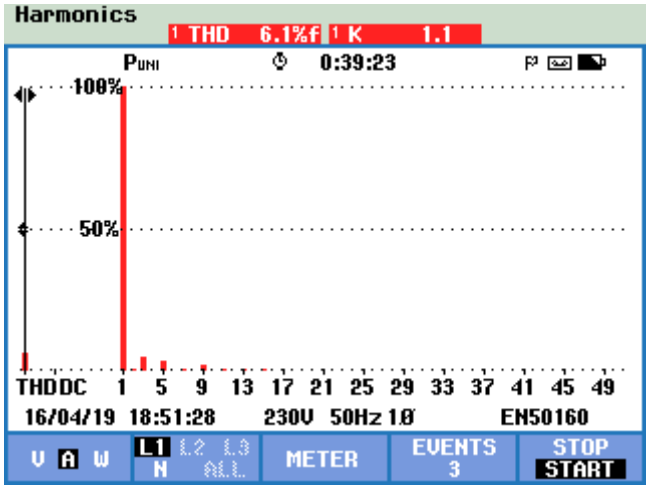

Fig.18: THD of the source current is 6.1%

The results observed from practical validation are tabulated in Table 2. It has observed that the proposed circuit of CC with LCL filter and rectifier reduces THD considerably and smoothens the shape of AC side source current. Thus the circuit is suitable for the applications like power supplies for viz. electric vehicles, TV and computers.

Table II. Experimental results of CC with LCL filter and rectifier

Parameter	Values
AC Input Voltage	22V
DC Output Voltage	-41 V
AC Source current and DC load current	2.73A and -1.3A
THD	6.1%

VIII. CONCLUSION

The Cuk Converter (CC) circuit consists inductors on both input and output sides, which reduces ripple current on both sides. The converter with reduced ripple current is a real candidate for power supply applications. The CC circuit is connected to rectifier board to extend the measurements to AC side. The uncontrolled rectifier with CC design provide low power factor, hence a LCL filter is designed in the proposed circuit for power factor correction. A Cuk Converter with LCL filter and rectifier circuit is proposed in this paper to improve the power factor. The reduction in ripple current decreases the conduction losses in the circuit, hence the output power is increased. The low ripple current in CC topology improves the shape of DC side source current, which in turn shapes the AC source current more sinusoidal. The symmetrical current on source side is having only odd harmonics, which are eliminated in the circuit by the accurate design of LCL filter. The reduction of harmonics reduces THD and hence improves the power factor. The power drawn from the source is decreased by the improvement of power factor, which enhances efficiency. The CC topology with LCL filter and rectifier is simulated to confirm the analytical outcomes. Also the circuit is validated practically using FPGA controller to confirm the simulated results.

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