International Journal of Engineering and Advanced Technology (IJEAT)
ISSN: 2249-8958 (Online), Volume-8 Issue-6, August, 2019

Noise Immune Pseudo-Stacked-wide keeper Domino technique for Ultra Deep Submicron Technology

Sapna Rani Ghimiray, Preetisudha Meher, Pranab Kishore Dutta

Abstract*: The demand of high performance with low leakage has extensively exploited domino logics for high speed computing and microprocessor systems. But this benefit gets compromised with scaling of technology leading to increase in sub-threshold leakage and reduced noise immunity. This paper presents a new performance oriented circuit technique for higher noise immunity with ultra-low leakage and better speed design. The proposed circuit technique employs pseudo buffer along with stacking effect to reduce leakage and power dissipation. The modified keeper transistor in the proposed circuit helps to reduce circuit delay and also improve noise sensitivity. The simulation has been carried out using Cadence spectre 90nm technology with results indicating 57% to 68% less leakage and 77% less power dissipation. The Energy-Delay-Product for the proposed circuit is the lowest in comparison to other existing techniques. The high values of Average Noise Threshold Energy, Unity Noise gain and Energy Normalized Average Noise Threshold Energy proves the improvement in Noise robustness over the previous techniques.

***Keywords* : ANTE, Domino, EDP, Power, Pseudo, Stacked.**

I. INTRODUCTION

Increased demand for energy-efficient, fast and non-interference battery-operated portable devices and wireless systems including personal digital assistants, notebooks and mobile phones requires VLSI designs with least power and delay characteristics [1][2]. To achieve this, vigorous scaling of technology and supply voltage is exploited. The supply voltage scaling for reducing the dynamic power leads to reduction of threshold voltage. This leads to exponential increase in sub-threshold leakage in short channel devices [3][4]. Thus, improving noise immunity with reduction in leakage current is of major concern in recent technology era involving high- performance and robust designs.

Due to their low power consumption and fast operation along with low transistor count, domino circuits are one of the better contender over static CMOS logic in the field of signal processing, computing and microprocessor systems [5,6]. However, the major drawback associated with domino circuit is its noise sensitivity proving it to be less robust then static CMOS logics [4][7][8]. So, high performance characteristics of domino technique is related to their low noise immunity [9]. Therefore, the trade-off between the reliability and performance needs to be at an optimized value [5].

A typical domino logic as in [10], suffers from charge sharing due to increased contention between evaluation network and dynamic node, and charge leakage resulting from leaky parallel legs in the evaluation network. So, traditional domino technique employs a weak PMOS keeper transistor to overcome these issues. Fig 1. shows traditional standard footed domino with and without keeper. The upsizing of this keeper transistor improves noise robustness with performance degradation due to relatively increased power consumption, and vice-versa. Thus, making the choice of keeper size hideous work. The measure which helps designer in this case is keeper ratio (K), defined as the ratio of current drivability of PMOS keeper transistor to PDN transistors. It is given by,

$$K = \frac{\mu_p (W/L)_{keeper\_transistor}}{\mu_n (W/L)_{PDN\_transistor}} \quad (1)$$

where, μ_n and μ_p are mobility's of electron and holes for a given technology, respectively. And, (W/L) is the aspect ratio of the device.

Several techniques has been introduced to overcome the leakage, power dissipation along with improvement in noise sensitivity over the years. This paper introduces a new circuit technique based on remodelling of keeper structure and footer transistor, to overcome the trade-off between performance and circuit robustness. The use of static inverter is replaced by using pseudo buffer as in [11], to reduce switching across the NMOS of inverter and reduction in power consumption. The idea behind the design is,

- Use of two keeper transistors in an arrangement providing lesser delay due to decreased feedback loop gain between the output and keeper, while increasing the threshold for second keeper leading to reduction in leakage across it caused by stacking effect.

Revised Manuscript Received on October 30, 2019.
* Correspondence Author
Sapna Rani Ghimiray*, Department of Electronics and Communication Engineering, NERIST, NIRJULI, INDIA. Email: sapna2203.sanu@gmail.com.
Preetisudha Meher, Department of Electronics and Communication Engineering, NIT Arunachal Pradesh, YUPIA, INDIA. Email: preetisudha1@gmail.com.
Pranab Kishore Dutta, Department of Electronics and Communication Engineering, NERIST, NIRJULI, INDIA. Email: pkdutta07@gmail.com.

- Use of stacking effect by footer transistors, reducing overall power consumption, and
- Connecting the source of NMOS device of output inverter to source of evaluation network transistors to eliminate switching current, helping in restoring the noise robustness with lesser power consumption.

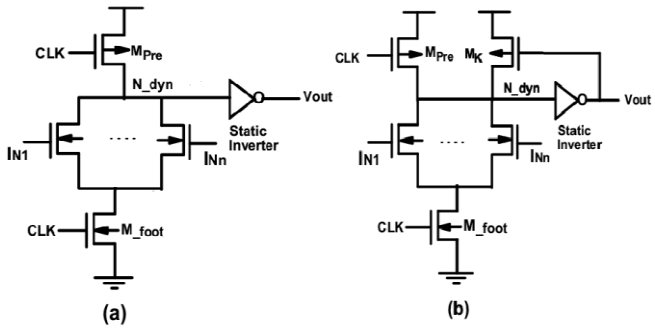


Fig. 1. Schematic of Traditional Standard Footed domino logic (a) without Keeper; (b) with Keeper

Adder being the crucial element in wide arithmetic and computing applications such as addition, multiplication, division, etc. finds immense interest by researchers [12][13]. 1-bit Adder unit has been designed and validated to further prove the effectiveness of the proposed domino design.

The rest of the paper is organized as: Section II describes the proposed domino logic technique for 2-input OR gate and 1-bit adder unit, with Section III illustrating the performance and noise margin metrics for the proposed circuit along with simulation framework. Section IV holds the simulation results and comparison of this results with traditional footed domino and pseudo-buffer domino technique for 2-input OR gate, along with results comparison for adder cell with few existing techniques. And, Section V consists of conclusion.

II. PROPOSED CIRCUIT DESIGN

A. Pseudo Stacked-Wide Keeper Domino Logic

Conventionally, the dynamic node capacitance is large in case of OR gate and if the fan-in increases, the capacitance also increases, resulting in dramatic speed reduction. Compared to AND gates, the wide fan-in OR gates are more prone to low noise robustness because of more number of parallel leaky paths. Hence, improvement in noise immunity is possible by upsizing keeper transistor at the expense of increased power consumption and delay. This issue can be solved by employing the same upsized keeper in the form of two series connected keepers creating stacking effect at the drain terminal of all evaluation transistors. By doing so, the threshold of the second keeper is increased, resulting in reduced leakage through it to the evaluation transistors. Also, as the variation of aspect ratio of keeper transistor and pre-charge transistor does not contribute significantly in the delay of the circuit. So, we focused on reducing the effect of feedback loop between the output and keeper transistor to reduce the overall delay of the circuit while attaining maximum immunity. The use of pseudo-buffer helps in restricting the pre-charge pulse from penetrating to the output. Thus, helping in reducing the switching of the input leading to saving power consumed by the buffer. Finally, the footer transistor section below the pull down network (PDN) networks helps in reducing the gate-to-source voltage of all evaluation transistors. It is achieved by increasing the threshold voltage of footer transistors. Thus, resulting in lesser leakage power, more noise robustness for the proposed circuit.

The Fig 2 illustrates the 2-input OR gate based on proposed domino circuit technique. It consists of four sections, transistor M_{pre}, M_{k1} and M_{k2} of pre-charge section, PDN network in evaluation section, transistors $M_{\_foot}$, M2 and M3 in footer section with pseudo buffer transistors M_{p1} and M_{n1} in output section. Transistor M_{pre}, precharges the dynamic node to V_{DD} and restrains the dynamic node voltage from discharging due to charge sharing or charge leakage caused by evaluation network transistors. The $M_{\_foot}$ transistor, changes the new gate switching threshold voltage (V_{th}) to twice the original V_{th} of the NMOS devices by increasing the V_{th} of the evaluation transistor. This further helps in reducing the leakage while improving noise immunity with relatively degraded performance.

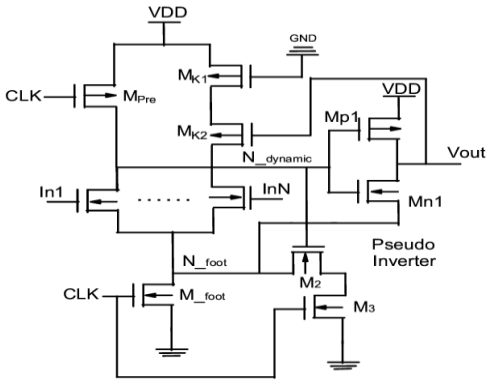


Fig. 2. Schematic of 2-input OR gate based on proposed domino technique

This performance issue is resolved with the help of transistor M_2 and M_3. The source of M_2 is connected to source of NMOS device, M_{n1}, and drain is connected to the transistor M_3. The gate of M_2 is connected to dynamic node, whereas the gate of M_3 is connected to clock. The performance of the circuit is increases by increasing total evaluation current. Therefore, transistor $M_{\_foot}$ and M_3 are made equally wider. Resulting in increased total evaluation current as the sum of current through the PDN plus current through M_3. Transistor M_2 on the other hand helps in discharging of dynamic node and maintaining the output logic during evaluation phase.

The positive feedback loop between output and keeper transistor M_{k2}, helps in eliminating evaluation phase short circuit current, hence, helping in reducing power consumption. Keeper transistor M_{k1} and M_{k2} are series connected, with gate of M_{k1} grounded which increases the threshold voltage (V_{tp}), of the M_{k2} keeper, resulting in lower leakage and delay. The aspect ratio of M_{k1} and M_{k2} are manages in such a way that, the dc current following through them equals the direct current (DC) following through the single upsized keeper with $(W/L)_K$ aspect ratio.

The circuit technique illustrated in Fig 2 operates in two phases.

Pre-charge Phase: In pre-charge phase, the clock is low and transistor M_{pre}, and M_2 are ON,

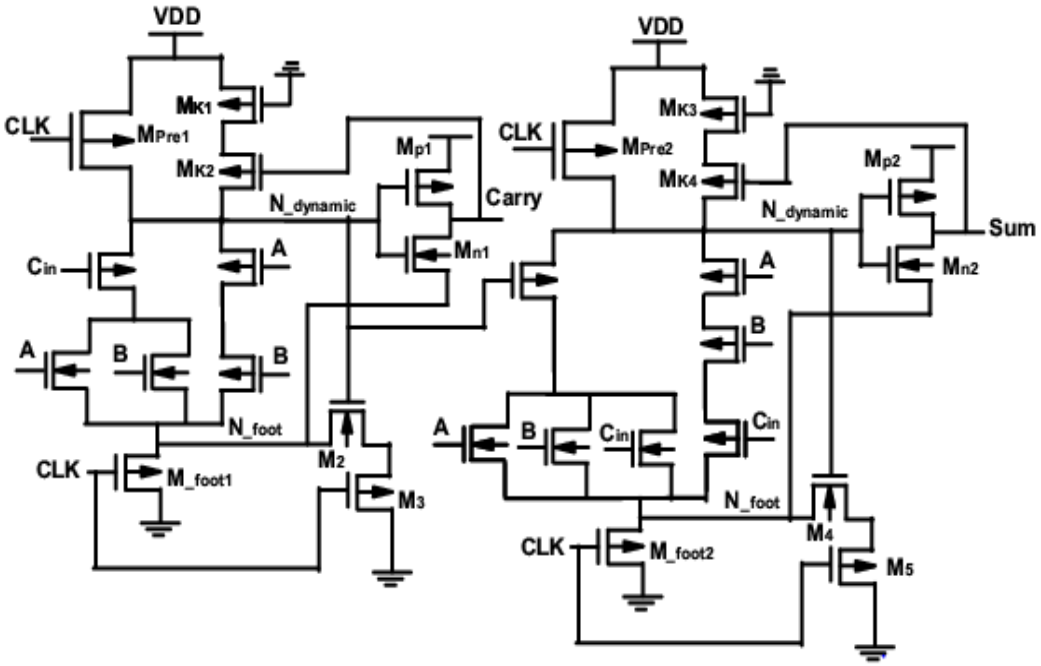


Fig. 3. Schematic of 1-bit Full Adder based on proposed domino technique

whereas transistors $M_{\_foot}$, M_{k1}, M_{k2} and M_3 are OFF. The Precharge transistor M_{pre} holds dynamic node to V_{DD} irrespective of the applied input. Since dynamic node is at V_{DD} and gate of M_2 is connected to it, M_2 is ON while ensuring N_foot to be nearly equal to N_dynamic. Therefore, the gate voltage of M_{n1} becomes $V_{GS} - V_S < V_{th}$; keeping the NMOS M_{n1} in OFF condition. Hence, maintaining the output node at completely low level (i.e., 0) through the output buffer NMOS being equal to N_foot.

Evaluation Phase: In evaluation phase, CLK is high and transistor $M_{\_foot}$, M_2, M_3 and M_{k2} along with PDN are ON. The turning ON of $M_{\_foot}$ discharges N_foot node to 0. This leads to voltage drop across it, which results in reduced switching V_{th} for the evaluation transistor. This voltage drop also leads to leaking of transistor M_2, which is compensated by employing transistor M_3. M_3 reduces current through M_2 using stacking effect making the $M_{\_foot}$ transistor less conducting and reducing overall leakage in footer section. Also, discharging of dynamic node makes the gate-to-source voltage of transistor M_{n1} '0', turning it OFF and charging of output node depends on transistor M_{p1}.

B. Pseudo Stacked-Wide Keeper Adder

The schematic of proposed adder cell is illustrated in Fig 3. The circuit consists of two pre-charge transistors, M_{pre1} and M_{pre2}, each for evaluation of carry and sum, respectively, four keeper transistors M_{k1}, M_{k2}, M_{k3} and M_{k4} in a pair of two, along with evaluation network for carry and sum generation, six transistors in footer section in a group of three, with two pseudo-buffers.

During pre-charge, CLK is low and M_{pre1}, Mp_{re2} are ON and dynamic nodes are pre-charged to V_{DD}. Evaluation transistors are OFF, so, in carry and sum generation the N_foot nodes are at slightly greater than '0' level, making the source of pseudo buffer transistors M_{n1} and M_{n2} almost zero, while the gate connected to dynamic _node, turns ON these transistors and output follows the N_foot.

During evaluation phase, CLK goes high and $M_{\_foot1}$, $M_{\_foot2}$ are ON, making the N_foot node discharge to zero. Also, the N_dynamic node discharges to zero depending upon ON evaluation transistors, leading to zero V_{GS} voltage for M_{n1} and M_{n2}, turning them OFF. Since, the NMOS in the buffer section are OFF, output follows transistors M_{p1} and M_{p2} completely. Therefore, depending upon the inputs applied i.e., if any one of the input is high, discharging of dynamic node and change in output node occurs. Whereas, if all the input are low, the dynamic node remains intact to V_{DD} with help of keeper transistors which eliminates charge sharing and charge leakage possibilities. The adder cell proposed in Fig 3 has three inputs A, B , Cin and two outputs as carry and sum , expressed as,

$$Carry = Cin \times (A + B) + A \times B$$
$$Sum = Carry \times (A + B + Cin) + A \times B \times Cin \quad (2)$$

III. PERFORMANCE AND NOISE MARGIN METRICS

A. Power Analysis Metric

The amount of total power consumption in generic is defined for three parameters [14][15][16].

Stand-by power: It indicates the power leaked within the circuit by OFF transistors.

$$P_{stand\_by} = V_{DD}.I_{OFF} \quad (3.1)$$

where, V_{DD} represents supply voltage and I_{OFF} is the leakage current, respectively.

Dynamic power: it depicts the amount of power consumed due to switching activity of transistors within the circuit leading to charging, discharging of load capacitance.

$$P_{dynamic} = V_{DD}^2.f_{CLK}.C_{load}.\alpha_i \quad (3.2)$$

where, C_{load} is the load capacitance with α_i being the switching activity factor and f_{CLK} is operating clock frequency, respectively.

Short-circuit power: it indicates the amount of power dissipated during input signal transitioning,
which results in creating direct path between supply and ground.

$$P_{short\_circuit} = V_{DD}.I_{SC}.f_{CLK}.t_{SC} \quad (3.3)$$

where, I_{SC} is the short-circuit current and t_{SC} is the time for which all devices were conducting.

Therefore, the total power dissipation is expressed as,

$$P_{Total} = V_{DD}.I_{OFF} + V_{DD}^2.f_{CLK}.C_{load}.\alpha_i + V_{DD}.I_{SC}.f_{CLK}.t_{SC} \quad (4)$$

The three main elements contributing OFF state leakage are gate induced drain leakage (I_{GIDL}), reverse biased junction leakage (I_{Rev}) and subthreshold leakage (I_{Sub}). Among the three, subthreshold leakage is dominating component as per in [13] and is given by,

$$I_{Sub} = (\frac{W}{L}).\mu.VT^2.C_s.e^{\frac{V_{GS}-V_{th}+\eta V_{DS}}{n.VT}}(1-e^{\frac{-V_{DS}}{VT}}) \quad (5)$$

where, (W/L) is the aspect ratio, μ is the carrier mobility, C_s is the summation of depletion region capacitance and interface trap capacitance, η is the drain-induced barrier lowering (DIBL) coefficient with n as slop factor and VT is the thermal voltage at temperature T.

B. Propagation Delay Metric

Propagation delay of the proposed circuit is evaluated with 50% duty cycle time difference between falling and rising edge presuming that, prior to the controlling signal's rising edge input has been considerably set. The average propagation delay is the average of rising and falling propagation delay, respectively.

C. Noise Metrics

Robustness of the circuit can be evaluated with the help of three noise margin metrics [17][18].

- *Unity Noise Gain (UNG):* It is defined as the amount of input noise amplitude that results in noise with same amplitude at the output [16][17] [19][24]. It is expressed as,

$$UNG = \{V_{in\_noise}; V_{in\_noise} = V_{out\_noise}\} \quad (6)$$

The UNG is obtained by applying an input noise pulse with varying amplitude and constant duration to the gate under test with worst case scenario leading to only one input as 1, while all others are 0.

- *Average Noise Threshold Energy (ANTE):* The tolerable average input noise energy of the circuit is defined as ANTE metric [18][19]. It is expressed as,

$$ANTE = E(V_{in\_noise}^2.T_{in\_noise}) \quad (7)$$

where, V_{in_noise} and T_{in_noise} are the input noise pulse amplitude and width, respectively with $E(\_)$ being the average, giving the expression for Metric as,

$$ANTE = \frac{(V_{in\_noise1}^2.T_{in\_noise1} + V_{in\_noise2}^2.T_{in\_noise2} + \ldots + V_{in\_noiseK}^2.T_{in\_noiseK})}{K} \quad (8)$$

where, K indicates the Noise Immunity Curve defining points. The higher value of ANTE relates the fact of lower chances of symbolic failure due to higher energy required for discharging dynamic node.

- *Energy Normalized Ante (NANTE):* This metric is used to indicate the associated energy (i.e., power and speed) penalty involved in the proposed circuit, and is expressed by [18][19],

$$NANTE = \frac{ANTE}{E} \quad (9)$$

where, E is a measure of energy penalty involved in improving noise immunity of the circuit, and is known as energy dissipated by the circuit per cycle, inclusive of capacitance, standby power dissipation, etc.

Higher the value of UNG, ANTE and NANTE, better is the noise immunity or circuit robustness. To compare the performance and energy metrics of proposed domino OR-gate and proposed Adder with traditional and previous domino techniques, a three-stage chain of 2-input OR gates and adder circuit is implemented.

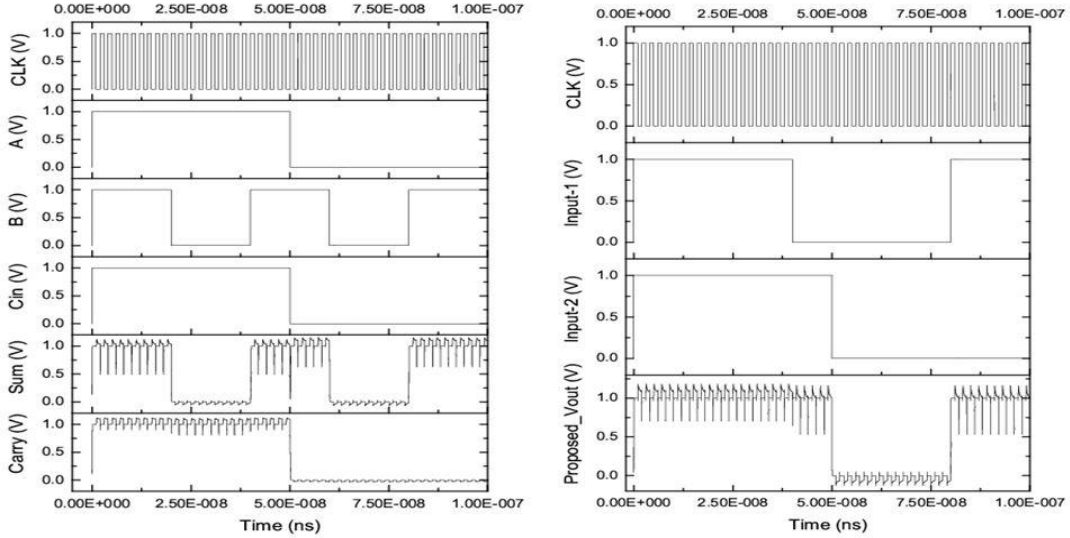
IV. RESULTS AND ANALYSIS

The proposed circuit along with traditional footed domino [10] logic circuit and pseudo buffer domino [11] logic 2-input OR gate were simulated using Cadence Spectre in 90nm technology model at 27^0 C temperature with supply voltage of 1V. The 2-input OR gate circuit operating at 500 MHz clock is used as benchmark. The output capacitance load for the worst case scenario is set as 5 Ff [5]. In order to understand application prospective of proposed domino technique, Full Adder cell is designed and simulated at 1V power supply, 110^0 C temperature with load capacitance as 10 Ff [15]. The results are then compared with conventional static logic adder [1][21], complementary pass transistor logic adder [22], hybrid adder as in [13], and pseudo-buffer domino based adder as in [11]. All the adder circuits used for comparison were simulated in same environment as of proposed adder.

The output waveform for the proposed domino based 2-input OR gate and 1-bit adder unit is illustrates in Fig 4(a) and Fig 4(b), respectively.

For all evaluation network transistors, the width is set to $W_{min} = 3L_{min}$, i.e., the minimum width where $L_{min} = 90nm$.

The transistors M_{pre}, $M_{\_foot}$ and M_3 are also set to minimum width, size with length equal to 90nm for obtaining lesser delay. The width of PMOS to NMOS transistors of the pseudo buffer is set to 3. The transistor M_2 is kept wider than $M_{\_foot}$ and M_3 to help in reducing leakage current. The keeper size is set assuming two keepers to be originally providing same dc current as single keeper. Further to reduce the delay, these



a b

Fig. 4. Output of proposed domino technique based (a) 2-input OR gate; and (b) 1-Bit Full Adder cell

Table-I: Size of transistors for the designed 2-input domino OR gates at 50ps iso-delay condition

Circuits	$(W/L)_{Keeper1}$	W_{Pre}	$(W/L)_{Keeper2}$	$(Wp/Wn)_{inv}$	W_{Foot}	W_2	W_3
Traditional domino	3 L_{min}/1 L_{min}	3 L_{min}	-NA-	6 L_{min}/3 L_{min}	-NA-	-NA-	-NA-
Pseudo-Buffer domino	3 L_{min}/1 L_{min}	3 L_{min}	-NA-	6 L_{min}/3 L_{min}	3 L_{min}	-NA-	-NA-
Proposed domino	3 L_{min}/1 L_{min}	3 L_{min}	3 L_{min}/1 L_{min}	9 L_{min}/3 L_{min}	3 L_{min}	4 L_{min}	3 L_{min}

Table-II: Leakage current involving all input states for different 2-input OR gates at same delay

Inputs		Leakage current for K=0.5 (nA)			Leakage current for K=1 (nA)		
A	B	*Traditional domino*	*Pseudo-buffer domino*	*Proposed domino*	*Traditional Domino*	*Pseudo-buffer domino*	*Proposed domino*
0	0	6.46	4.68	2.75	6.13	4.36	1.96
0	1	59.6	57.7	32.7	55.7	53.8	31.8
1	0	59.6	57.7	32.7	55.7	53.8	31.8
1	1	63.5	61.7	34.8	59.1	57.7	33.6

transistors aspect ratio is given as, $(L/W)_K = (L/W)_{K1} + (L/W)_{K2}$, which reduce the loop gain between output and keeper transistor M_{k2} [23]. Since, driving capability of keeper is lower, its width is set to minimum, whereas the length is set as equal to twice the minimum length. So, the width for keepers are $W_K = W_{K1} = W_{K2}$, while length is set as $L_K = L_{K1} + L_{K2}$. The same sizing constraints has been followed for the adder too. The proposed 2-input domino OR gate circuit is implemented and simulated for two different keeper ratios, i.e., K=0.5 and K=1. Table I illustrates the transistor sizing for the proposed 2-input OR gate.

Table II illustrates the leakage/ stand-by current variation in the proposed circuit and other reference circuit w.r.t. changing input. The careful sizing of transistors M_foot and M3 helps in decreasing its 'ON' time voltage drop. This reduction in voltage drop is further accompanied by increased Vth for PDN transistors caused by body effect. This body effect also influences the logic gate's supply voltage positively, helping to achieve lesser leakage. The data indicates minimum leakage for OFF state of both PDN transistors, while maximum leakage current with both transistors ON. The data further proved the proposed circuit to be least leaky compared to reference circuits.

The relationship between the leakage current and temperature is further examined and illustrated in Fig 5. It shows that, the increase in temperature attributes proportional increase in leakage, as the leakage for 100 ^{0}C temperature is almost 5 times greater than leakage at 27 ^{0}C.

Further, to acknowledge the effect of supply voltage on the power dissipation by the proposed OR gate, circuit has been simulated with different power supply. The lowest supply voltage used is V_{DD}=0.7 V with no symbolic failure, gives the least power dissipation. The variation in supply voltage is done in a step of 0.2 V. For V_{DD}=1.2 V and below, increase in power dissipation is considerably low compared to V_{DD}=1.5 V and V_{DD}=1.8V. The abrupt increase in the power consumption is resulted from increased leakage along with switching current. Fig 6 illustrates the relationship between variable supply voltage and power dissipation.

The noise robustness and circuit performance trade-off is clear from the simulation indicating slightly higher power dissipation, delay and hence lesser performance for proposed circuit with K=0.5 compared to K=1. Table III and Table IV illustrates the performance comparison for the proposed 2-input OR gate and performance comparison for Proposed adder cell, respectively. Both tables (Table III and Table IV) attributes to the fact of better performance for proposed circuit with K=1.

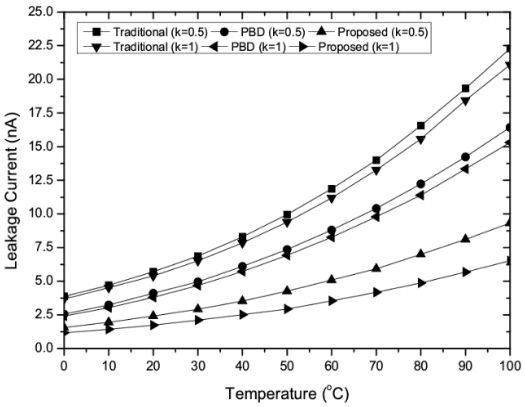


Fig. 5. Leakage current versus Temperature curve for 2-input domino OR gate.

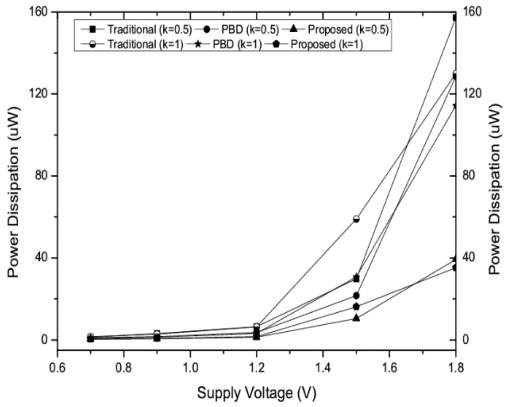


Fig. 6. Relationship between power dissipation and variable supply voltage for domino OR gate

Table-III: Power, EDP comparison for different 2-input OR gates (at VDD=1V and 50ps delay)

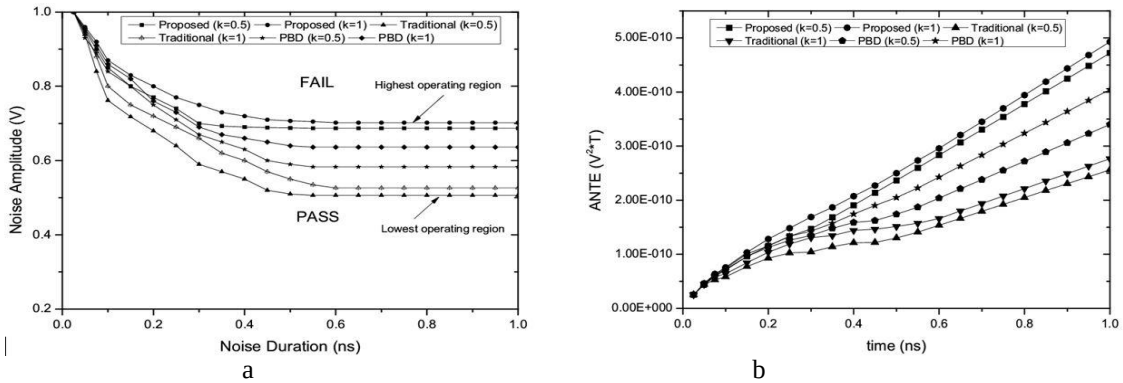
Keeper Ratio	Parameters	Circuit Techniques		
		Traditional domino	*Pseudo-buffer domino*	*Proposed domino*
K=0.5	Power, µW	3.89	1.97	0.89
	EDP, J^2	$9.72x10^{-27}$	$4.92x10^{-27}$	$2.22x10^{-27}$
K=1	Power, µW	3.59	1.61	0.87
	EDP, J^2	$8.97x10^{-27}$	$4.02x10^{-27}$	$2.17x10^{-27}$

Table-IV: Power and EDP comparison for different Full Adder cell at Supply Voltage= 1V.

Parameters	Circuit Techniques				
	CMOS Adder	*CPL Adder*	*Hybrid Adder*	*PBD based Adder*	*Proposed Adder*
Power, µW	18.32	14.65	12.16	4.53	2.11
EDP, J^2	$4.58x10^{-26}$	$3.66x10^{-26}$	$3.04x10^{-26}$	$1.13x10^{-26}$	$0.52x10^{-26}$
References	[1][19]	[20]	[11]	[9]	[Present]

Table-V: Normalized UNG comparison for 2-input OR gate under iso- delay

Circuit Techniques	Keeper Ratio, K=0.5		Keeper Ratio, K=0.5	
	UNG, mV	*Normalized UNG*	*UNG, mV*	*Normalized UNG*
Traditional Domino	506	1	526	1
Pseudo- Buffer Domino	583	1.15	636	1.20
Proposed Domino	687	1.36	702	1.34



a b

Fig. 7. Noise Margin Metric analysis results (a) NIC curve for 2-input OR gate; and (b) ANTE Curve for 2-input OR gates

The UNG of the proposed OR gate with K=1 and adder cell are found to be 702 mV and 734 mV which are highest compared to their respective reference circuits. The UNG comparison for 2-input OR gate normalized with respect to traditional domino OR gate is given in Table V.

The UNG evaluation only speaks about the amount of noise acceptable at output rather than detailing about the possible range of symbolic failure or pass region. Therefore, to understand the region of operation of our circuit ANTE is evaluated. Before

Table- VI: Comparison of ANTE and NANTE for all 2-input OR gates

Circuit	ANTE, (Pico Joule)		NANTE, (Kilo)	
	k=0.5	k=1	k=0.5	k=1
Proposed domino	235	248	5280.8	5701.1
Pseudo-Buffer Domino	179	207	4022.4	4758.6
Traditional Domino	138	152	3101.1	3494.2

Table-VII: Comparison of ANTE and NANTE for all Full Adder Cell

Circuit	ANTE, (Pico Joule)	NANTE (Kilo)	References
CSL Adder	142	1345.9	[1][19]
CPL Adder	149	1412.3	[20]
Hybrid Adder	206	1952.6	[11]
PBD based Adder	214	2028.4	[9]
Proposed Adder	270	2559.2	[Present]

evaluating ANTE, plotting NIC curve is desirable depending upon the noise pulses amplitude and duration variation. The Fig 7(a), Fig 7(b) illustrates NIC curve and ANTE curve for the proposed and reference techniques OR gate. The Table VI and Table VII illustrates the evaluated data for the ANTE and NANTE Metrics for the proposed domino OR gate and proposed domino Adder cell, respectively.

The high value of ANTE and NANTE for proposed OR gate and adder gives the possibility of almost no symbolic failure and high region of operation with better noise immunity for the proposed technique.

Figure of Merit (FOM), being the measure of comparison for existing circuit techniques, account for the power, delay, area along with Noise robustness [16][17][20][24], expressed by,

$$FOM = \frac{UNG_{Norm}}{P_{total} X t^2_{pdelay} X \sigma_{delay\_norm} X Area_{norm}} \quad (9)$$

where, $P_{total} X t^2_{pdelay}$ is one of the critical parameter of circuit, named as Energy-Delay-Product used for defining the energy efficiency of the circuit. For making FOM more realistic all the circuits to be compared to have same delay i.e., 50ps. Also, σ_{delay_norm} , UNG_{Norm} , and $Area_{norm}$ are the standard deviation of delay, UNG and die area normalized with respect to traditional footed domino.

Table VIII and Table IX illustrates the Normalized FOM comparison for proposed 2-input OR gate and Normalized FOM comparison for proposed adder, respectively. In Table VIII, proposed domino suffers with high die area compared to rest technique. It is then compensated with high UNG, low power dissipation leading to higher value of FOM. The highest value of FOM confirms realistic nature of the proposed circuit. The comparison drawn in Table IX is done on AV_Extracted view of all the designed adder. Although, normalized FOM evaluated in Table IX is not completely realistic because the comparison reference circuits are not entirely domino logic based (i.e., CSL and CPL logic are static CMOS based logics) as in case of Table VIII.

To examine the effects of process, voltage and temperature (PVT), variations on the proposed OR gate, the circuit is simulated in all four process corners, three temperatures (i.e.,

Table-VIII: Normalized FOM comparison for 2-input OR gate (under iso-delay condition)

Parameters	Traditional Domino	PB-domino	Proposed Domino
No. of transistors	7	7	9
σ_{delay}, ps	28	24	25
Normalized σ_{delay}	1	0.86	0.89
Power, µW	3.59	1.61	0.87
Normalized_Power	1	0.45	0.24
Normalized_Delay	1	1	1
Area, pm^2	292	323	396
Normalized_Area	1	1.11	1.36
UNG, mV	526	636	702
Normalized_UNG	1	1.20	1.34
FOM	1	2.8	4.6

Table-IX: Comparison of FOM normalized under same delay for all Full Adder cell

Parameters	CSL	CPL	HYBRID	PBD	Proposed Adder
No. of transistors	28	32	16	24	28
Power, µW	20.82	18.53	16.33	6.83	4.88
Normalized_Power	1	0.89	0.81	0.33	0.23
Normalized_Delay	1	1	1	1	1
Area, μm^2	240	287	186	218	265.12
Normalized_Area	1	1.20	0.78	0.91	1.10
Normalized σ_{delay}	1	1.10	0.72	1.36	1.38
UNG, mV	486	505	635	654	734
Normalized_UNG	1	1.04	1.31	1.35	1.51
FOM	1	0.88	2.91	3.29	4.31

-40 ^{0}C, 27 ^{0}C and 110 ^{0}C) using technology model of 90 nm at variable V_{DD} (i.e., 0.9 V to 1.8 V). The results of simulation for the normalized delay are shown in Fig 8(a) and Fig 8(b). Fig 8(a) refers to the temperature and process variation effects with three different temperature and all four corners on the Normalized delay at supply voltage of 1V, and Fig 8(b) refers to variable V_{DD} effect on the Normalized delay for typical process at 27 ^{0}C and is varied from 0.9 V to 1.8 V. The delay in both the cases has been normalized with respect to traditional footed domino delay at 1V and proposed circuit delay at 1V, respectively. The simulation reflects that the variation in V_{DD} from 0.1 to 0.3 results in normalized delay to be varied from 0.1 to 0.2 for the proposed circuit, which are lesser and within tolerable range. Thus, ensuring the proposed circuits functionality with PVT Variation. Also, the layout of the proposed adder is illustrated in Fig 9. Here, the area is obtained to be 12.26 µm X 21.625 µm, i.e. 265.12 μm^2 with *pcap* and *pres* as 1288 and 344, respectively.

V. CONCLUSION

In this paper, a new pseudo stacked-wider keeper domino circuit approach is proposed. The circuit topology helps in saving the power consumption up to 77%, with lowest leakage, better speed. It is obtained by reducing the circuit delay considerably, by employing stack transistor and wider keeper which attribute to higher performance. Also, the circuit achieve high values of noise margin metric compared to reference circuit from literature. While the UNG increases by 1.34 times with highest value of ANTE being 248 pico-joule and NANTE being 82.4 Mega, the approach is suitable for an optimized value of performance and robustness trade-off with minimum energy dissipation. The implementation of adder circuit at 1 V with 500MHz frequency, leads to leakage of 19 nA at 110 ^{0}C temperature, with power consumption 2.11 μW and lowest delay, making the adder efficient for all arithmetic and computing devices. The UNG of the adder is found to be improved by a factor of 1.51 times compared to conventional static logic adder.

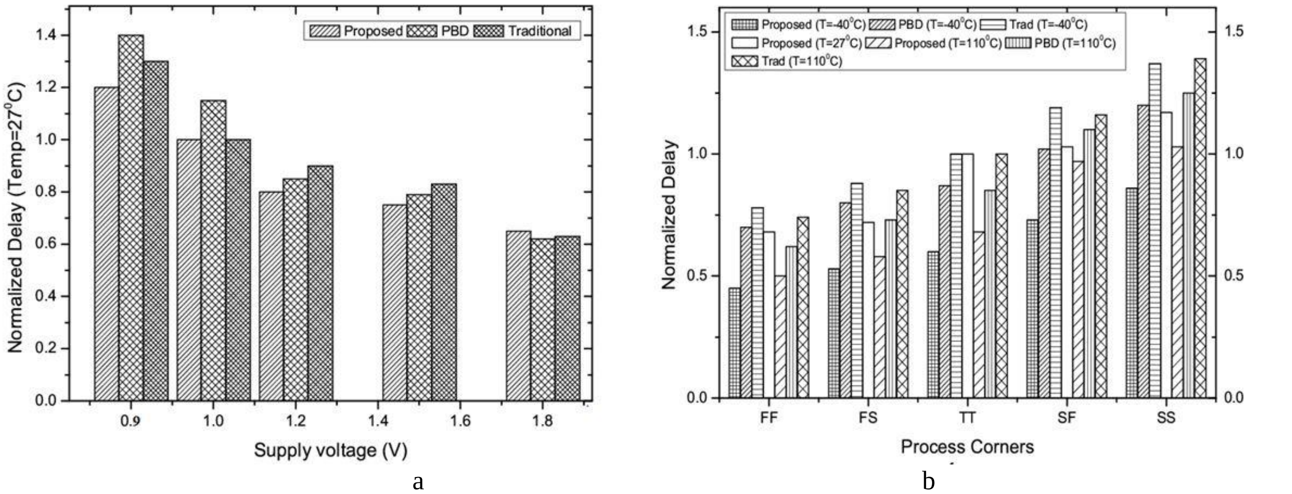


Fig. 8. PVT variation effects on proposed domino OR gate (a) Temperature and Process variation effects for different temperature and corners on Normalized delay, at supply voltage of 1V; and (b) variable VDD effect on Normalized delay for VDD variation from 0.9 V to 1.8 V.

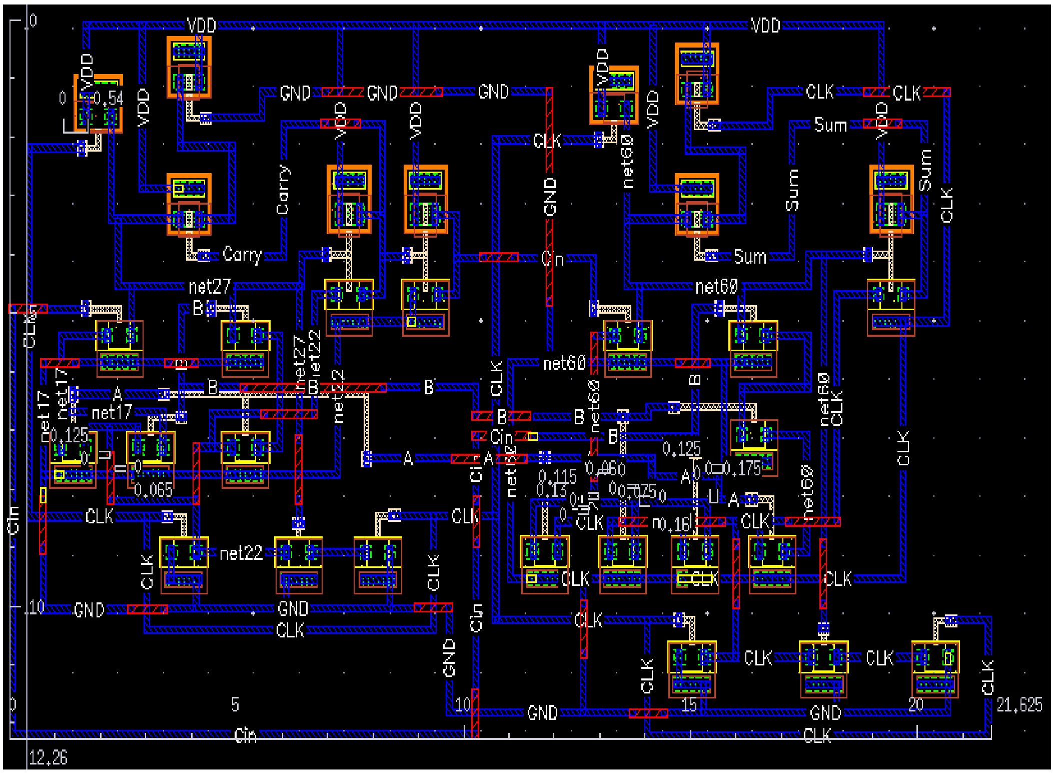


Fig. 9. Layout of the proposed pseudo stacked-wide keeper adder

ACKNOWLEDGMENT

The Authors extend their acknowledgement for the financial support provided by MHRD, Government of India for completing this research.

REFERENCES

1. J. M. Rabaey, A. Chandrakasan, and B. Nicolic," Digital Integrated Circuits: A Design Perspective," *Upper Saddle River,* NJ, Prentice-Hall, 2nd ed. 2003
2. Neil H.E. Weste, david Harris, "Principles of CMOS VLSI Design: A System Perspective," *Addison-Wesley*, 3rd ed. 2004
3. K. S. Yeo and K. Roy, "Low-voltage low-power voltage subsystems," *Tata Mc-Graw Hill edition*, 2009
4. S. H. Choi , Bipul C. Paul, K. Roy, "Dynamic Noise Analysis with Capacitive and Inductive Coupling," *in: Proc. of ASP-DAC,* January 2002, pp. 65-70.
5. Moradi Farshad, Tuan-Vu Cao, et al., "Domino logic designs for high-performance and leakage-tolerant application," *Integration the VLSI journal*, **46**, 2013, pp. 247-254.
6. M. Nasserian, M. Kafi- kangi, M. M. Nejad, "A low-power fast tag comparator by modifying charging scheme of wide fan-in dynamic OR gates," *Integration, the VLSI J*., vol. **52**, 2016, pp. 129-141.
7. Y. Sun, W. He, Z. Mao and V. Kursun, "Variable strength keeper for high-speed and low-leakage carbon nanotube domino logic," *Elsevier Microelectronics Journal*, **62**, 2017, pp. 12–20.
8. L. Ding, P. Mazumder, "On circuit techniques to improve noise immunity of CMOS dynamic logic," *IEEE Transactions on Very Largr Scale Integration (VLSI) Systems*, **12**,2004, pp. 910-925.
9. H. F. Dadgour and K. Banerjee, A novel variation-tolerant keeper architecture for high-performance low-power wide fan-in dynamic or gates, IEEE Trans. Very Large Scale (VLSI) Syst., 18 (2010) 1567–1577
10. R. H. Krambeck, C. M. Lee, H. F. S. Law, "High-speed compact circuits with CMOS," *IEEE Journal of Solid State Circuits*, **17,** 1982, pp. 614–619.
11. Fang Tang, Amine Bermak , Zhouye Gu, "Low Power dynamic logic circuit design using pseudo dynamic buffer," *Integration, the VLSI Journal*, **45**, 2012, pp. 395-404.
12. M. J. Zavarei, M. R. Baghbanmanesh, E. Kargaran, H. Nabovati, et al, "Design of new full adder cell using hybrid-CMOS logic style," *in: Proc. of 18th IEEE Int. Conf. Electron., Circuits Syst. (ICECS),* Dec. 2011, pp. 451–454.
13. P. Bhattacharya, B. Kundu, et al, "Performance analysis of a Low-power high-speed Hybrid 1-bit Full Adder circuit," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **23**, 2015, pp. 2001-2008.
14. K. Navi, V. Foroutan, M. Rahimi Azghadi, et al, "A Novel low power full-adder cell with new technique in designing logical gates based on static CMOS Inverter," *ELSEVIER Microelectronics Journal*, **40**, 2009, pp. 1441-1448.
15. F. Fallah, M. Pedram, "Standby and active leakage current control and minimization in CMOS VLSI circuits," *IEICE Trans. Electron (Special Section on Low-Power LSI and Low-Power IP),* E88-C, 2005, pp. 509-519.
16. Asyaei, Mohammad, "A new leakage-tolerant domino circuit using voltage-comparison for wide fan-in gates in deep sub-micron technology," *Integration, the VLSI Journal*, **51**, 2015, pp. 61-71.
17. H.Mahmoodi, K.Roy," Diode Footed Domino: A Leakage tolerant high fan-in dynamic circuit design style," *IEEE Trans, VLSI Syst.*, **14**, 2006, pp. 646-649.
18. L. Wang, N. R. Shanbhag, "An energy-efficient noise tolerant dynamic circuit technique," *IEEE Transaction on Circuits Systems - II*, **47**, 2000, pp. 1300–1306.
19. G. Balamurugan, N. R. Shanbhag, "Energy-efficient dynamic circuit design in the presence of crosstalk noise*," in: Proc. of Int. Symp. on Low Power Electronics and Design,* 1999, pp. 221–225.
20. A. Peiravi, M. Asyaei, "Robust low leakage controlled keeper by current-comparison domino for wide fan-in gates," *Integration, the VLSI J.*, **45**, 2012, pp. 22–32.
21. D. Radhakrishnan, "Low-voltage low-power CMOS full adder, " *IEE Proc.-Circuits Devices Syst*., 148, 2001, pp. 19–24.
22. R. Zimmermann and W. Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic", *IEEE J. Solid-State Circuits,* **32**,1997, pp. 1079–1097.
23. G. Palumbo, M. pennisi, M. Alioto, "A Simple approach to reduce delay variations in domino logic gates," *IEEE Trans. On Circuits and Systems – I: Regular Papers,* **59**, 2012, pp. 2292-2300.
24. Ali Peiravi, Mohammad Asyaei, "Current-Comparision-Based Domino: New Low-Leakage High-Speed Domino Circuit for Wide FanIn Gates," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst*., **21**, 2013, pp. 934–943.

AUTHORS PROFILE

Sapna Rani Ghimiray received the B.Tech degree in Electronics and Communication Engineering from the North Eastern Regional Institute of Science and Technology, Arunachal Pradesh, India, in 2012 and the M.Tech degree in VLSI Design from Manipal University, India, in 2014. She is currently working towards the Ph.D. degree in the Department of Electronics and Communication Engineering from the North Eastern Regional Institute of Science and Technology, Arunachal Pradesh, India. Her current research interests include leakage-tolerant circuit design and low-power VLSI design.

Dr. Preetisudha Meher is now working as an assistant professor at National Institute of Technology, Arunachal Pradesh, India. She has done Ph.D from National Institute of Technology, Rourkela, India. Her area of interest is VLSI and Embedded systems. She had passed her M.Tech from National Institute of Science and Technology, India in the year 2008. She had done her B. Tech from Biju Pattnaik University of Technology, India. She is a researcher having many IEEE and other journal and conference papers.

Dr. Pranab Kishore Dutta is currently working as an Assistant Professor at NERIST, Arunachal Pradesh, India. He has done Ph.D from Jadavpur University, India. His area of interest are Semiconductor devices and VLSI, Digital Design. He had completed his M.Tech from Tejpur University, India in the year 2000.