International Journal of Engineering and Advanced Technology (IJEAT)
ISSN: 2249-8958 (Online), Volume-8 Issue-6, August, 2019

Clock Tree Optimization for Multi-Corner Multi-Mode Timing Closure with Different Design Flows

Kasi Annapurna.Nalluri, G. R. L.V. N. Srinivasa Raju

Abstract*: Clock Tree Optimization for Multi Corner Multi Mode Timing closure is done with Integrated Clock Gating cells. It is power efficient clock tree technique because, it will reduce the switching power usage of clock. It is implemented using integrated clock Gating cells for reducing the switching power caused by clock propagation in the design during Clock Tree Synthesis. The multi mode and multi corner uses integrated clock gating cells to achieve timing and these cells will reduce dynamic power .This technique can be applied to industrial Digital Intellectual Property(DIP). The cells used in the design are fabricated by using 22nm FDSOI process and these cells used as clock pins by Automatic Root Clock Pin (ARCP) in Clock Specification file during clock tree synthesis along with proposed flows for reducing buffer count. The result shows that the number of buffers added in the each stage is reduced by the proposed flow and also we achieve the timing, power and area. In this paper, by using clock tree optimization technique the clock power dissipation in the chip is reduced by Integrated clock gating cells.

Keywords*: ARCP (*Automatic Root Clock Pin*) ,*Clock Gating (CG)*, Clock *Tree synthesis, ECO (Engineering Change Order), FDSOI (Fully Depleted Silicon On Insulator) , Macro Model, MCMM (Multi Corner and Multi Mode).

I. INTRODUCTION

Today's mobile market demands the low power system on chips (SoC's) for portable devices, where the main energy source is battery. The major portion of the power is consumed in the SoC is the clock power, as it operates at very high frequency and also the generation of such a high frequency requires more number of flip flops and buffers tends to more complex SoC. In earlier technologies, the area and timing are the two important parameters in the design of an integrated circuit. Now a day's most sophisticated tools came into the market which drastically reduces the area and timing constraints, at the same time the present IC industry demands low power devices with negligible leakage currents at low clock frequencies, but the device densities and operating clock frequencies have increased rapidly in CMOS devices, which leads to the increase in the power consumption drastically.

At the same time, supply voltages of the transistors and threshold voltages of the transistors have been reduced, because the leakage current becomes a significant and major problem. As a result, power has

become as important as timing or area. In order to meet the requirements, the clock buffers and normal buffers are increased by its count.Most of the commercial tools in the market are tried to avoid the setup and hold violations but it will add more buffers as a result of increased power consumption in the block level or chip level.The MBFFs was first proposed in [1], which has four stages in the design flow such as logic synthesis, pre-placement, in placement and post placements, but it is having a disadvantage of grouping single bit inputs before the floor planning stage. In [2, 3] cell libraries are Created and can be utilized during logic synthesis but suffers from worst timing and delay. To avoid the timing and delay budgets MBFFs are generated after the post-placement stage [4-7] and in [8] MBFFs are created in placement iteration rather than at the post-placement stage. The above approach does not consider clock tree topologies during flip-flop merging, which may result in longer latency/delay of the clock network [9]. Clock tree latency is an important factor in addition to other metrics [10-11]. The clock tree latency is especially important as the technology scales down to nanometers. Different works are proposed in the recent past to minimize the latency of clock network and power consumption [12, 13] and in [14], five different clock tree flows are proposed. It requires more number of buffers to avoid the timing violations which leads to the power consumption and also the density in the design is also more.

II. FDSOI (FULLY DEPLETED SILICON ON INSULATOR)

Over the past few decades, the transistor size has shrunk below a few tens of nano meters (nm), the effort has increased the challenges for every new generation of technology. This significant change in transistor size causes leakage current, which increases the power consumption in a proportionate manner in standard bulk CMOS process. In order to deliver higher performance keeping the leakages under control, a Fully Depleted Silicon On Insulator (FD-SOI) technology was proposed by Global Foundries. FDSOI is a planar process with reduced silicon geometries compared to CMOS process.

Revised Manuscript Received on October 30, 2019.
* Correspondence Author
Kasi Annapurna.Nalluri, Physical Design Engineer in a reputed company on lower node technologies from APR (Automatic Place and Route) to Sign-Off (GDSOUT).
G. R. L.V. N. Srinivasa Raju, Professor and HOD in the Department of ECE, Shri Vishnu Engineering College for Women, Bhimavaram
© The Authors. Published by Blue Eyes Intelligence Engineering and Sciences Publication (BEIESP). This is an open access article under the CC BY-NC-ND license (http://creativecommons.org/licenses/by-nc-nd/4.0/)

This technology based upon two ultra thin buried oxide, which is positioned on a thin silicon substrate. Due to the thin film silicon structure, there is no need to dope the channel, thus making the transistor “fully depleted". In the Fig.1 (a) the conventional CMOS device and in the Fig.1 (b) the fully depleted (FD) 2D SOI wafer is shown. In this paper, clock tree optimization technique is implemented in 22nm FDSOI technology, as it is having an advantage of low leakage currents.

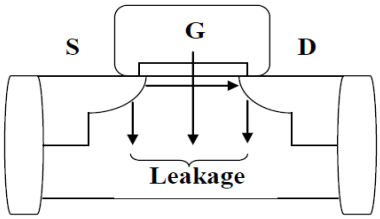

Fig.1(a) conventional CMOS

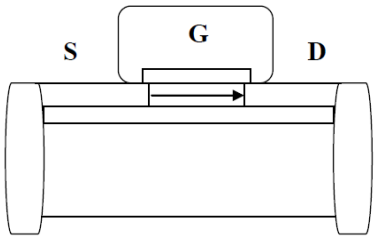

Fig:1(b) FDSOI device

III. CLOCK TREE SYNTHESIS

Clock tree synthesis plays a major role in physical design. Once the placement is done, the clock tree is propagated in entire layout based on SDC (Synopsis Design Constraints). To perform the clock tree synthesis placement database and clock tree specification file is very much essential in SDC. The specification file contains the clock information, excluded and global excluded pins. It also contains clock tree information like clock routing layers and Non Default Rules (NDR). The clock is very sensitive in nature, and it will continuously change its states so the cross talk may come into picture. In order to avoid these violations, NDR for these clock routings should be the double width and double spacing.The conventional flow of design approach is followed as shown in Fig.2, which will add more number of buffers to avoid the timing violations which lead to the more power consumption and density in the design. In block level, setup and hold timing in both modes i.e., functional mode and scan mode are achieved [14]. The density must be under control, because at block level the timing violations may not present but, when it comes to the chip level there is a less chance of timing clean in all corners. So, to meet the timing clean at the chip level, the top level timing ECO's are implemented. For implementing top level ECO's buffers are inserted or resizing or adding of delay cells based on the slack. The suggested modifications must be incorporated in the block level database and again rerouting is done. In the proposed design, all the design rule violations parameters such as Max transition, Max capacitance and Max fan-out are checked at all corners like, slow-slow(ss), typical–typical(tt) and fast-fast(ff) corners with 0.72V, 0.8V and 0.88V respectively. Even after implementing these modifications, if the timing requirements are not met for achieving the required constraints a modified is suggested as shown in Fig.3.

In ***conventional Flow (FLOW1)***, it will add buffers during optimizations of APR Flow like Place, CTS and Route Optimization to meet the timing. (i.e., setup time and hold time in all scenarios). Scenario is combination of Multi Mode and Multi corner.

While coming to, lower node (i.e., lower nano meter technologies) the main aspects like Area, power and time will play a major role. We can clean the timing with FLOW1, but it won’t reduce Power and Area.

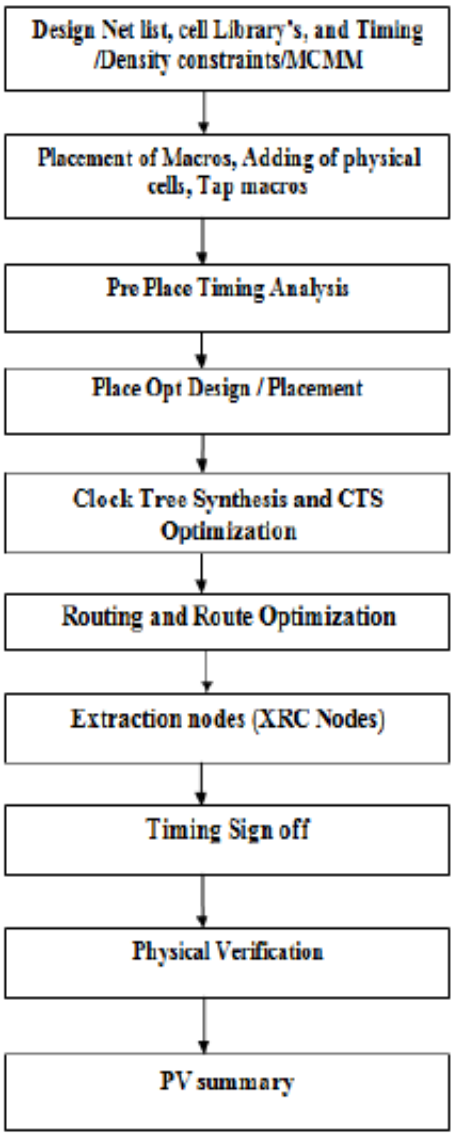

Fig.2 Conventional Flow (FLOW1)

In order to reduce Power and Area occupied by the standard cells in the design, we need to implement optimization techniques like FLOW2, FLOW3, FLOW4 and FLOW5 (Proposed Flow). By these flows, we can reduce the buffer count indirectly which helps to reduce power and Area Consumption in the design.These flows help to achieve better optimization in lower node technologies, mainly for Timing, Power and Area of the Chip.

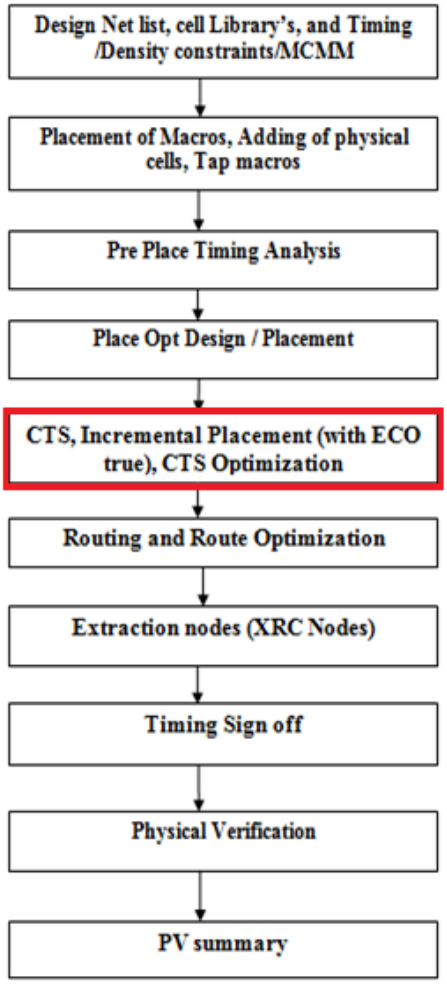

Fig.3 Design flow is updated with Incremental Placement (FLOW2)

Clock Gating: Clock gating shown in Fig. 4 uses data path signals to inhibit or permit clock edges to propagate from a clock source to clock sinks. The clock arrival time at a clock gating cell is unknown prior to CTS and this arrival time determines the required time for the data path control signal to reach the clock gating cell enable input. Therefore, the setup slack at a clock gating enable input is hard to predict pre CTS. In addition, clock gating cells have an earlier clock arrival time than regular sinks. Therefore, often timing is critical. Typically, the fan-in registers controlling clock gating may need to have an earlier clock arrival time than regular sinks in order to avoid a clock gating slack violation –which means the fan-in registers need to be skewed early.

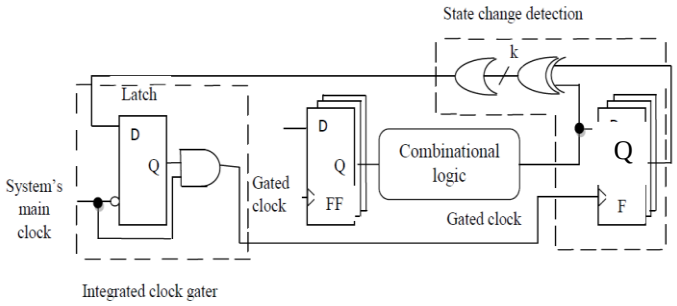

Fig. 4 Clock Gating Cell

IV. BLOCK DIAGRAM OF ALWAYS ON (AON)

Always-on domain shown in Fig.5, enriched with an analog comparator to generate wake-up events from an analog signal, 2KB SRAM in retention at 0.6V(lowest retention voltage). This Always-on power domain has an independent supply from the rest of SoC with its dedicated LDO. The memory has two possible supply sources depending on its power mode. Low drop out regulators (LDOs) are a simple inexpensive way to regulate an output voltage that is powered from a higher voltage input. Retention registers or memories are used to hold data or register states before a power down. Retention registers are always on, even in the power down mode.

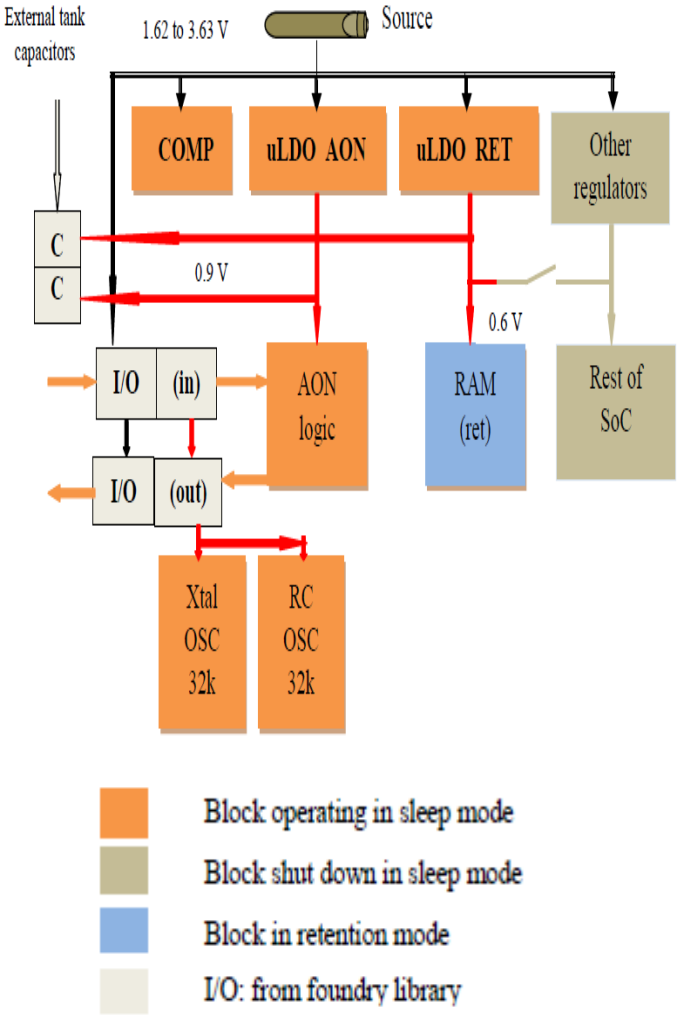

Fig. 5 Block Diagram of Always in Block (AON)

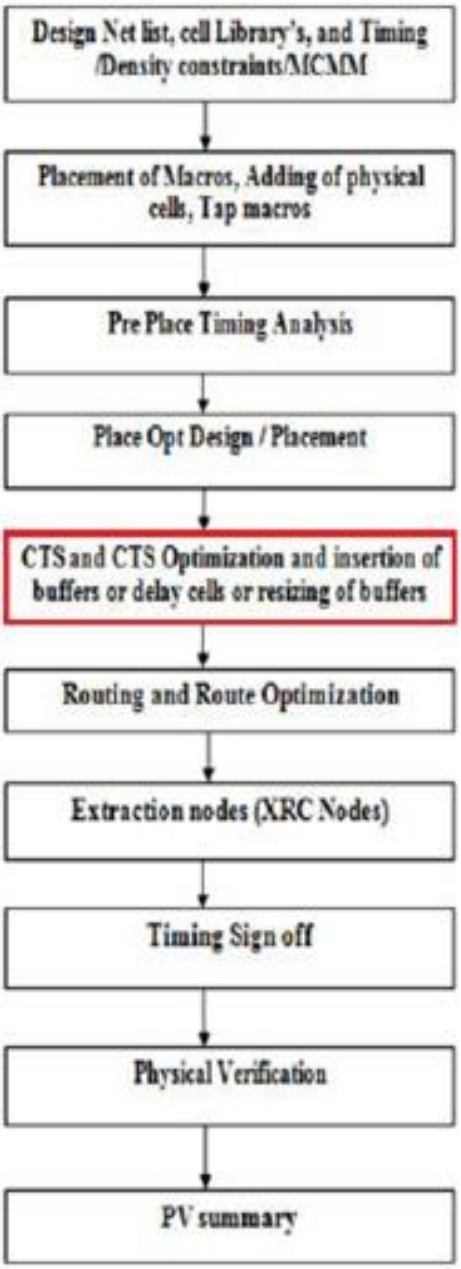

Fig.6 Flow is updated with buffer insertion in CTS stage (FLOW3)

In Fig. 7, a macro model is a block that has been clock tree synthesized, so that the delays are identified. All macro model statements must be specified in the top lines of the clock tree specification file. The experimental results are shown in Table. I to III. There are two ways to set the Macro Model pin properties inside Encounter.

(1) Cell/Port delay specification that has all the instantiations of cells have the same pin delay. The syntax of the macro model is "*Macro Model port cell Name/port Name max Rise Delay min Rise Delay max Fall Delay min Fall Delay input Cap"*, Eg. Macro Model port spram288x65/clk -5ns -4.5ns -5ns -4.5ns 10ff.

V. MACRO MODEL

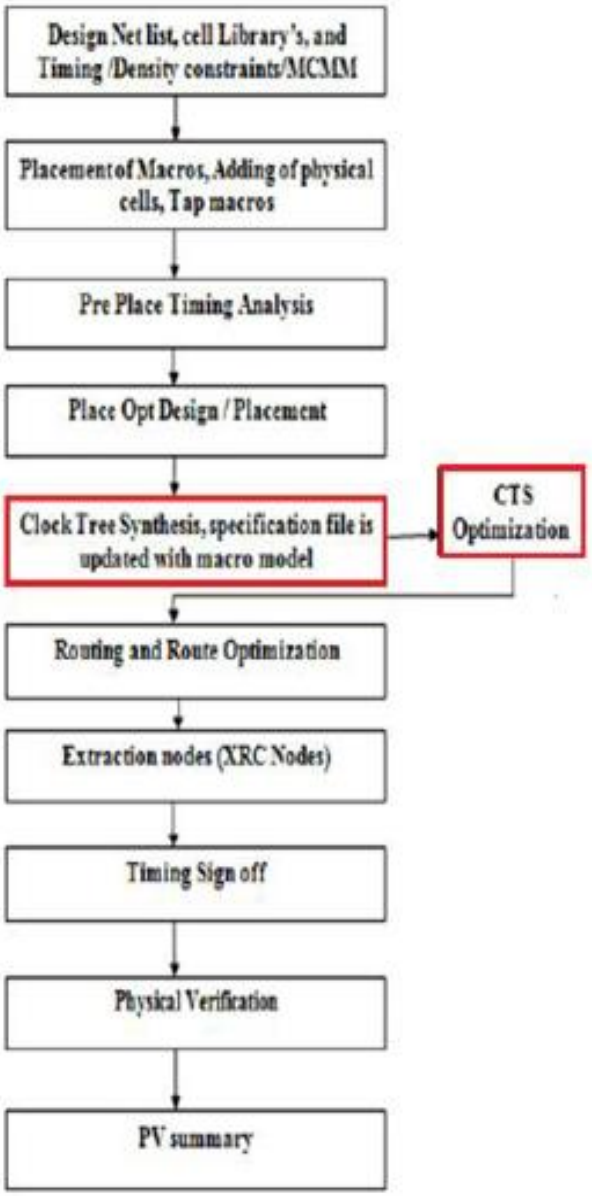

Fig.7 Flow is updated with Macro model in specification file in CTS stage (FLOW4)

(2) Pin instance delay specification that can supersede a Cell/Port delay, the syntax of the macro model is "*Macro Model pin leaf Pin Name max Rise Delay min Rise Delay max Fall Delay min Fall Delay input Cap"*, Eg. Macro Model pin mem_core/clk 20ps 18ps 20ps 18ps 28ff.

VI. PROPOSED METHOD

The experiments are performed to get timing clean in all corners in functional and scan mode with density under control and buffers added in each stage are reduced. The Fig.3 to Fig. 8, are different experiments implemented on Always on Block.

Fig .5 shown above tells us, in each and every flow the number of buffers added in the design is gradually decreased, along with timing clean in all corners. In each stage there is a need to check the power bump. If it is more, then it is checked, whether it is expected are not and then only it will move into further stages. Power dissipation of each cell will accumulate and especially, the number of clock buffers added in the design is also an important factor, because compared to normal buffer the clock buffer will exhibits more power and those are added in CTS stage. So, it is made sure that the count of clock buffers is controllable and acceptable.The CTS Stage, Plays a major role in the PnR (Place and Route) flow, the clock power will leads to major power consumption in the design. The frequent switching of the clock will cause the power consumption, so the clock buffer exhibits the more drop compare to normal buffers. The *duty cycle of the clock buffers will be 50%.The ON and OFF times of clock buffers will be same. These are specially designed for the CTS stage. Compare to normal flip flop the Clock Buffers offer more delay.

VII. ENGINEERING CHANGE ORDER (ECO)

Engineering Change Order (ECO) [8] is the process of changing the PNR net list, in order to meet the timing requirements. (i.e. setup time, hold time, data transition, clock transition and max capacitance) For e.g. if there is a setup violation in the design, it implies that a combinational path has large delay than required. In this case, you need to reduce the delay by upsizing cell, which reduces resistance, in turn, reduces RC [9] delay of the path.

Setup Time = (T_clk + T_cap – T_setup – T_uncertainty) – (T_launch + T_cq + T _combi)

Hold Time= (T_launch + T _cq + T _combi) – (T _cap +T_ hold + T _uncertainty)

T_clk→ Clock Period
T_cap→ Capture Time
T_setup → Setup Time
T_Hold→ Hold Time
T_uncertainty → Uncertainty Value
T_Launch → Launch Time
T_cq →Clock to Q Delay
T_combi → Combination Delay or Data path Delay
In other words,
Setup time = RT-AT
Hold time = AT-RT
AT→ Arrival Time
RT→Required Time

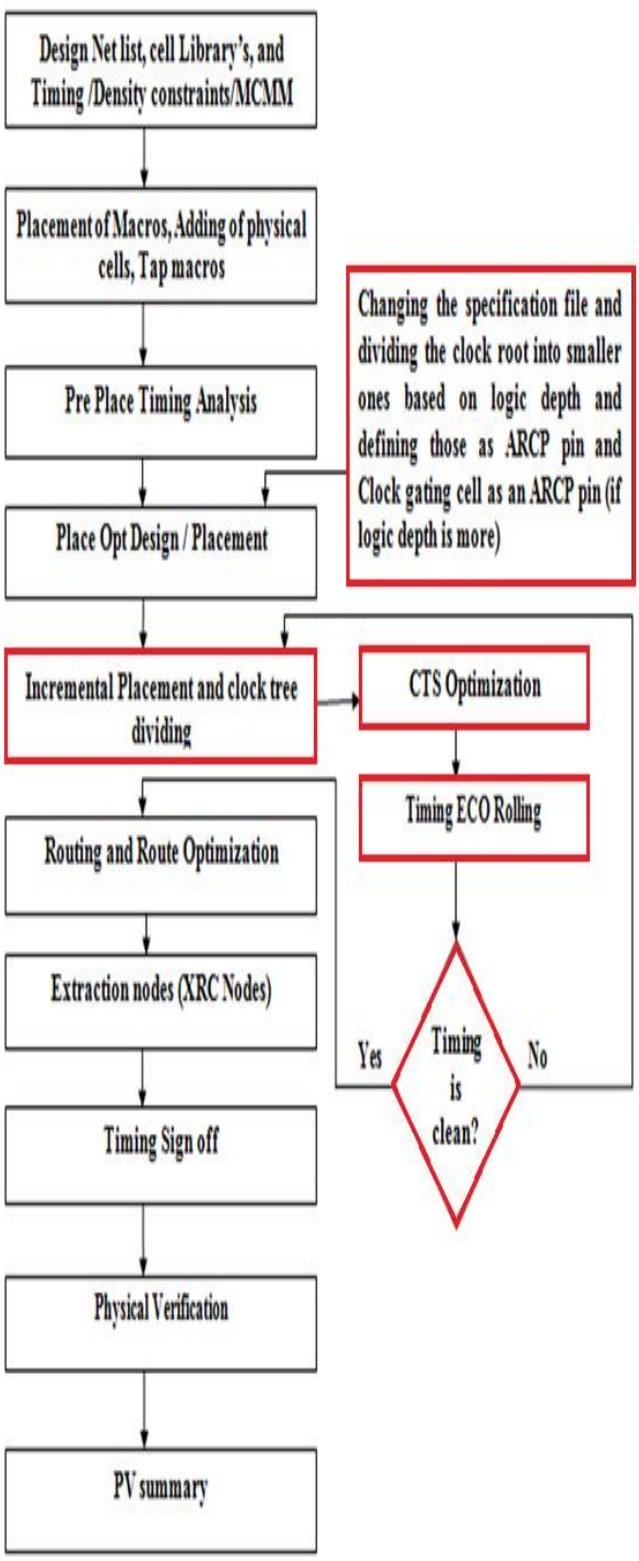

Fig. 8 Clock tree is dividing based on logic depth and makes it as ARCP (Automatic Root Clock Pin) and these are updated in clock specification file (FLOW5)

VIII. TIMING ANALYSIS IN THE DESIGN

Ideally timing clean means setup and hold values in all modes should become zero. It is achieved by,

1. **Fixing setup**: We have two chances, increasing the clock path delay or reducing the data path delay, without increasing the clock period to zero along with fixing hold by adding buffers to the data path or adding clock buffers to the launch path in clock to make it zero. If it is not fixed then, we will increase clock period which lowers the frequency to fix setup which ideally gives margin to hold. Mostly, we will not prefer to use this method, but it is the last option for timing clean. Timing clean is setup and hold. In DRV clock transitions, data transitions, SI glitch and pulse width all should be zero.

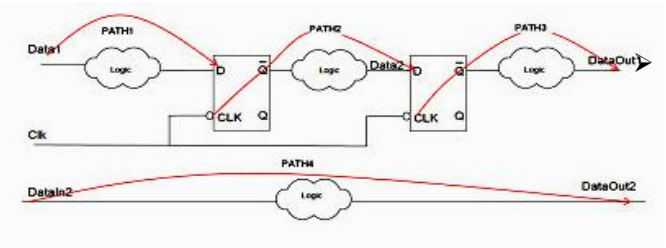

Fig. 9 Timing Paths In Design

- Path 1:Input pin or Input port to Register (flip-flop) ,
- Path 2 : Register to Register
- Path 3 : Register to output Pin/output Port
- Path 4 : Input Pin/Input Port to output Pin /output Port

While fixing any setup/hold/DRV (Design Rule Violations), which has worst slack (highest Negative slack), is called **Worst Negative Slack (WNS)**. Summation of all negative slacks while fixing setup /hold is called as **Total Negative Slack (TNS).**

Design Rule Violations max capacitance, clock transitions, data transitions, SI glitch, pulse width and fan out should be optimal with the desired design requirements.

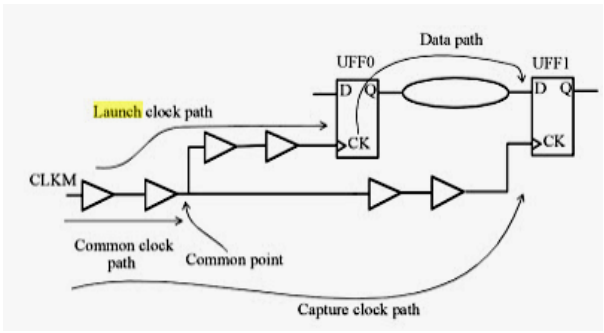

Fig. 10 Timing path for Register to Register

Here,

- UFF0 → Launch path Flip Flop
- UFF1→ capture path Flip Flop
- Data path → combination delay between UFF0 and UFF1.
- Start point for this data path is UFF0/CK and end point is UFF1/D.

- All should be cleaned/ optimized with respect to AOCV (Advanced On chip Variations) libraries before it is OCV (On Chip Variations) libraries in STA. Variation of fabrication parameters used in applying an integrated circuit design to a semiconductor wafer. These corners are dependent on FEOL (Front End of Line), BEOL (Back End OF Line) and FEOL can be achieved by the processes TT (Typical-Typical), FF (Fast-Fast) and SS (Slow-slow) and FS (Fast-Slow) & SF (Slow-Fast), but we don't consider these two because of skewed. BEOL are due to on chip variations and we will fix the timing in these corners, RCBEST and RCWORST.

  Advantages are dependent on customer requirements, right now functional modes are used for better performance, power and optimization. Scan modes are used to check the register working by testing with lower frequencies

  We will mainly focus in Register to Register timing paths in our design like Input pin to output pin, Input Port to Register, and Register to output port depending on the design requirements. These paths have the flexibility, we can fix these paths in top level or flattened level, but Register to Register need to fix in all corners for setup and hold in Scan mode and Functional mode.

- Register to register path, Worst Negative Slack (**WNS**) and Total Negative Slacks (**TNS**) in functional and scan modes for setup and hold is updated in below tables. Refer Table 1 for setup time values and DRV's and Table 2 for Hold time values.

IX. EXPERIMENTAL RESULTS

In the experimental results, mainly five flows are compared in functional mode and scan mode and WNS, TNS and violating paths in each stage is mentioned in the below tables.

TABLE I represents the setup time values and DRVs in each flow and it is observed that the proposed flow (FLOW 5) gives the better values.

Flow 1: Conventional Flow

Flow 2: Design flow is updated with Incremental Placement

Flow 3: Flow is updated with buffer insertion in CTS stage

Flow 4: Flow is updated with Macro model in specification file in CTS stage

Flow 5: Clock tree is dividing based on logic depth and makes it as ARCP (Automatic Root Clock Pin) and these are updated in clock specification file.

TABLE I: comparison between Worst Negative Slack (WNS), Total Negative Slack and DRV's for five Design Flows (Setup Slack)

Stage	Design Flow	Test Mode@0.72V		FuncMode@0.72V		DRV's(Design Rule Violations)			
		WNS(ns)	TNS(ns)	WNS(ns)	TNS(ns)	max_cap	max_tra	max_fanout	max_length
	Flow1	13.5	0	9	0	50	55	5	5
Placement	Flow2	10.013	0	5.279	0	9	40	1	0
	Flow3	13.588	0	7.963	0	0	46	2	0
	Flow4	13.443	0	8.157	0	1	46	1	1
	Flow5	13.443	0	8.157	0	1	46	1	1
	Flow1	6.5	0	2.4	0	6	50	0	0
CTS Stage	Flow2	3.77	0	3.813	0	10	43	0	0
	Flow3	7.98	0	8.25	0	0	48	0	0
	Flow4	9.357	0	8.466	0	0	70	0	0
	Flow5	11.329	0	7.403	0	2	210	0	0
	Flow1	0.173	0	0.308	0	2	45	1	0
CTSOptimization	Flow2	5.974	0	5.7	0	0	46	1	1
	Flow3	7.195	0	8.122	0	0	3	2	0
	Flow4	8.177	0	8.38	0	0	43	2	0
	Flow5	9.831	0	7.398	0	1	0	2	0
	Flow1	0	0	0	0	1	43	2	0
RouteOptimization	Flow2	5.82	0	3.63	0	1	49	1	9
	Flow3	6.995	0	8.046	0	0	4	2	0
	Flow4	7.54	0	7.97	0	1	1	2	0
	Flow5	12.75	0	7.114	0	0	0	0	0

The Table III shows the different stages of physical design cycle for different flows from conventional flow (Flow1) to the proposed flow (Flow5).From the results shown in Table III, It is observed that the Proposed method having very low dynamic power of 3 mW, which shows 30% reduction.

Fig.11 shows the buffer count and DRC violations for different stages of physical design cycle. From the figure, it is observed that Flow 5 having 47% reduction in buffer count in the placement stage, and In CTS stage, 38% reduction of buffer count and especially CK Buffers are reduced by 41% and at the same time, caliber DRC count is almost 43.7% reduction in DRC violations when compared to conventional flows.

TABLE II: Comparison between worst Negative Slack (WNS), Total Negative Slack for five Design Flows (Hold Slack) and VP (Number of Violating Paths)

Stage	Design	Test Mode @0.88V			Test Mode@0.72V			Test Mode @ 0.8V			Func Mode @0.88V			Func Mode@0.72V			Func Mode @ 0.8V		
	Flow	WNS(ns)	TNS(ns)	VP	WNS(ns)	TNS(ns)	VP	WNS(ns)	TNS(ns)	VP	WNS(ns)	TNS(ns)	VP	WNS(ns)	TNS(ns)	VP	WNS(ns)	TNS(ns)	VP
	Flow1	-1.613	-323	261	-6.785	-1012	244	-2.6	-432	328	-0.149	-1.731	29	-0.919	-0.919	1	-0.299	-0.849	15
CTS Stage	Flow2	-1.008	-29.861	289	-3.06	-23.73	80	-1.269	-23.399	91	-0.183	-2.125	136	-0.243	-0.643	4	-0.183	-0.683	4
	Flow3	-1.436	-3.695	130	-4.6	-9.6	3	-1.837	-3.919	3	-0.177	-0.498	23	-0.289	-0.289	2	-0.216	-0.357	2
	Flow4	-1.06	-6.097	358	-3.39	-6.98	3	-1.43	-5.69	192	-0.239	-0.822	30	0.791	-0.956	2	-0.382	-1.007	22
	Flow5	-0.517	-3.429	221	-1.408	-3.282	3	-0.739	-2.799	74	-0.755	-1.016	6	-2.15	-2.775	2	-1.017	-1.722	12
	Flow1	-1.9	2.2	2	-6.7	7	2	-2.6	-3.12	2	-0.032	-0.032	1	-0.225	-0.225	1	-0.085	-0.121	2
CTSOptimization	Flow2	-0.829	-2.719	4	-2.48	-7.439	4	-1.05	-3.36	4	0.002	0	0	0.148	0	0	0.093	0	0
	Flow3	-1.585	-3.169	2	-5.352	-10.7	2	-2.064	-4.129	2	-0.032	-0.063	2	0.163	0	0	0.063	0	0
	Flow4	-1.307	-4.36	173	-4.38	-8.73	2	-1.79	-4.92	125	-0.025	-0.081	4	0.069	0	0	-0.022	-0.049	3
	Flow5	0.03	0	0	0.179	0	0	0.067	0	0	0.03	0	0	0.103	0	0	0.033	0	0
	Flow1	-1.82	-1.82	1	-6.46	-6.46	1	-2.5	2.55	2	-0.03	-0.03	1	0.046	0	0	-0.036	-0.036	1
RouteOptimization	Flow2	-0.668	-2.219	5	-1.92	-5.76	4	-0.855	-2.806	4	-0.018	0	0	0.105	0	0	0.055	0	0
	Flow3	-1.57	-3.14	2	-5.32	-10.64	2	-2.07	-4.14	2	-0.04	-0.079	2	0.48	0	0	0.044	0	0
	Flow4	-1.259	-2.519	3	-4.34	-8.69	2	-1.74	-3.53	3	0.036	0	0	0.646	0	0	0.079	0	0
	Flow5	0.035	0	0	0.034	0	0	0.033	0	0	0.002	0	0	0.15	0	0	0.034	0	0

TABLE III: Buffer count in each stage in five Design flows

Design Flow	Placement	CTS Optimization	Route Optimization	CKBuffers	Delay cells	DRC count	Calibre DRC	Power Numbers				Dynamic Power (mw)
								IP(mw)	SP(mw)	LP(mw)	TP(mw)	
Flow1	2727	1888	180	185	669	555	8k	0.09	0.8	7.46	8.3646	10.5
Flow2	1702	767	38	154	584	560	6k	0.06241	0.194	7.46	7.725	8.8
Flow3	1659	1911	494	188	367	585	6k	0.5167	0.5199	0.00223	0.5398	4
Flow4	1376	1314	19	125	353	380	5.8k	0.0225	0.552	0.002	0.5766	3.8
Flow5	1284	720	13	76	320	130	3.5k	0.04861	0.1535	0.0021	0.1741	3

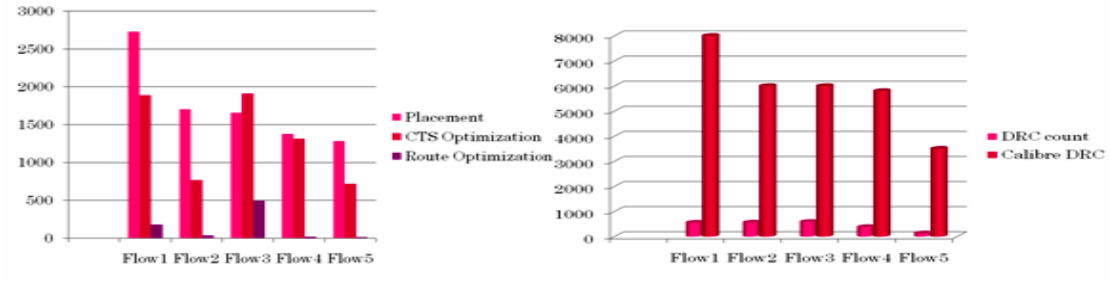

Fig. 11.Buffer and DRC Count in each stage with 5 design Flows

X. CONCLUSION

In this Paper, the clock network optimization is done by the Integrated clock gating cells and clock tree optimization through ARCP and Flows. These methods significantly reduces the buffer count in each stage along with Signal Net Routes.The proposed method is very efficent in reducing Power,Area and Timng.It is efficient in reduction of Dynamic Power and helps to reduce the timing ECO's [Engineering Change Order] for timing closure.The design is signoff in all scenarios, which are required for the better implementation of the design. Design is closed in block level as well as chip level.

ACKNOWLEDGMENT

We express our profound gratitude to K.V. Vishnu Raju, Chairman, Shri Vishnu Educational Society (SVES) and **G.Srinivasa Rao,** Principal, Shri Vishnu Engineering College for Women, Bhimavaram for providing us the Cadence tools during our project work. I express my heartfelt thanks for their extended support in providing the internship opportunity at Siliconus Technologies, Bangalore. I would like to express my sincere thanks to Mr. U.J. Mark, Mr. A. Anil Kumar, and Mr. B. Teja, Senior Physical Design Engineers, Siliconus Technologies, Bangalore, for their extraordinary conceptual guidance along with constant encouragement throughout the work. I am indebted to the faculty of Department of ECE for their valuable suggestions, which helped us during the completion of the work. Praises and thanks to the Almighty for his showers of blessings all throughout the work. Special thanks to my parents, sister, brother and my friends for the support and trust in me.

REFERENCES

1. R. Pokala, R. Feretich, and R. McGuffin, "Physical synthesis for performance optimization," Proceedings of IEEE International ASIC Conference and Exhibit, pp. 34–37, Sep. 1992.
2. C.-C. Hsu, Y.-C. Chen, and M. P.-H. Lin, "In-placement clock-tree aware multi-bit flip-flop generation for power optimization," in Proceedings of IEEE/ACM International Conference on Computer-Aided Design, 2013, pp. 592–598
3. J. G. Xi and W. W.-M. Dai, "Buffer insertion and sizing under process variations for low power clock distribution," in Proceedings of ACM/IEEE Design Automation Conference, 1995, pp. 491–496.
4. L. Chen, A. Hung, H.-M. Chen, E. Tsai, S.-H. Chen, M.-H. Ku, and C.-C. Chen, "using multi-bit flip-flop for clock power saving by design compiler," Proceedings of Synopsys users Group, 2010.
5. Z.-W. Chen and J.-T. Yan, "Routability-constrained multi-bit flip-flop construction for clock power reduction," Integration, the VLSI Journal, 2012.
6. M. P.-H. Lin, C.-C. Hsu, and Y.-T. Chang, "Post-placement power optimization with multi- bit flip-flops," IEEE Trans. Computer-Aided Design, vol. 30, no. 12, pp. 1870–1882, 2011.
7. S.-H. Wang, Y.-Y. Liang, T.-Y. Kuo, and W.-K. Mak, "Power-driven flip-flop merging and relocation," IEEE Trans. Computer-Aided Design, vol. 31, no. 2, pp. 180–191, 2012.
8. Y.-T. Shyu, J.-M. Lin, C.-P. Huang, C.-W. Lin, Y.-Z. Lin, and S.-J. Chang, "Effective and efficient approach for power reduction by using multi-bit flip-flops," IEEE Trans. VLSI Syst., vol. 21, pp. 624–635, 2013.
9. S. Roy, P. Matthaiakis, Pavlos, L. Masse-Navette, and D. Z. Pan, "Evolving Challenges and Techniques for Nanometer SoC Clock Network Synthesis," in IEEE Int. Conf. on Solid-State and Integrated Circuit Technology (ICSICT), Guilin, China, October, 2014, pp1-4.
10. S. Roy, P. M. Mattheakis, L. M. Navette, and D. Z. Pan, "Clock tree resynthesis for multi- corner multi-mode timing closure," IEEE Trans Comput. Aided Design Integr. Circuits Syst., vol. 34, no. 4, 2015, pp. 589602.
11. C. Chen, C. Kang, and M. Sarrafzadeh, "Activity-sensitive clock tree construction for low power," in Proceedings of Int. Symp. on Low Power Electron. Design, Aug. 2002, pp. 279– 282.
12. Y. Wang, Q. Zhou, X. Hong, and Y. Cai, "Clock-tree aware placement based on dynamic clock-tree building," in Proc. IEEE Int. Symp. Circuits Syst., New Orleans, LA, USA, 2007, pp. 2040–2043.
13. T. Lee, J. Yi, and J. Yang "Multi-bit Flip-flop Generation Considering Multi-corner Multimode Timing Constraint," in Proc. IEEE Int. Symp. Circuits Syst., May 2016.
14. Aehee Lee, David Z.pan,Joon –Sung Yang, "Clock Network Optimization with Multi –bit Flip Flop Generation Considering Multi corner Multi Mode Timing constraint,"IEEE Transactions on computer Aided Design of Integrated Circuits.,DOI 10.1109/TCAD 2017.2698025

AUTHORS PROFILE

N Kasi Annapurna M.Tech (VLSI Design). I have done this industrial project in Siliconus Technologies Private Limited in Bangalore. Got Gold Medal in my academics .Currently working as a **Physical Design Engineer** in a reputed company on lower node technologies from APR (Automatic Place and Route) to Sign-Off (**GDSOUT**).

Dr. G.R.L.V.N.Srinivasa Raju working as a Professor and HOD in the Department of ECE, **Shri Vishnu Engineering College for Women, Bhimavaram**. He has 26 years of teaching and 3 years Industrial experience. Under his guidance UG Course accredited by NBA twice in Tier-1 & Tier-2. PG course has been accredited by NBA under Tier-2. Published 10 International Journal Papers and 20 Conference papers. As a Co-PI and PI received 15.9 Lakhs under MODROBS from AICTE for 2 labs. Co-Principal Investigator for the FDP, "Challenges in FPGA Based Digital System Design", funded by A.I.C.T.E. Under his Mentorship Dr. K. Padma Vasavi implemented a project entitled "Development of a Motion Detection and Human Tracking System using a Scale Invariant Approach". This project was funded by DST under Women scientist program. Presently implementing a Tide DST project entitled "Development and Implementation of Telephony Speech Enhancement Algorithms Using Data Hiding Techniques for Hearing Impaired People" as a Co-PI.