International Journal of Engineering and Advanced Technology (IJEAT)
ISSN: 2249-8958 (Online), Volume-8 Issue-6, August 2019

BlackBox Model Based VLSI Hierarchical Floorplanning

Rajasekhara Reddy Kallam, Srinivasulu Gundala

Abstract: ***Nowadays in VLSI number of transistors integrated on a single silicon chip is increasing day by day and the complexity of the design is increases tremendously. This makes very difficult for the designer and EDA tools. As number of instances increases the run time and memory for implementing the design increases. This will make more pressure on the designer because if product is not completed within the time to market company will lost so much of money. Floorplanning is the basic building step for any hierarchical physical design flow. Floorplanning is taking more amount of time in entire design hierarchical flow. If floorplanning is not good the entire design will take more time and it will increase a greater number of iterations to complete the design. In the top-level chip planning the quality of the floorplanning depends on the proper alignment of blocks and easy to meet the timing and congestion. To reduce memory size of CPU and run time, in this project we are using a method of Backbox model based top level hierarchical floorplanning based physical design. The main aim of this project is to reduce the number of instances which are not necessary in the top level chip floor planning which reduces peak memory for the design and also reducing CPU run time for getting proper prototype design in the top level ASIC design and estimate the congestion in the design at initial stage and modify floor planning to obtain quality of prototype model in the floorplanning. This project is designed on cadence encounter tool.***

Index Terms**: Heirarchical floorplanning, Blackbox model, Instances, VLSI, Physical design.**

I. INTRODUCTION

Physical design is the process of creating the physical layout of the corresponding to the netlist. In the physical design process various stages are available. They are floorplannig, power planning, placement, clock tree design, global routing, detailed routing, timing verification for each and every stage in design and finally getting the GDSII file. As a greater number of devices integrated on the single silicon chip the complexity of the design increases day by day which is appearing in the nano scale design [2]. Floorplanning is the most important step in the PD flow. The quality of the Floorplanning is effect on further stages of placement, cts, routing [3].

Revised Manuscript Received on August 30, 2019.

* Correspondence Author

Rajasekhara Reddy Kallam*, Electronics and Communication Engineering, LakiReddy Bali Reddy College of Engineering (Autonomous), Mylavaram, Krishna Dt, Andra Prasesh INDIA

Srinivasulu Gundala, Professor, Electronics and Communication Engineering , LakiReddy Bali Reddy College of Engineering (Autonomous), Mylavaram, Krishna Dt, Andra Prasesh INDIA

If the Floorplanning is not in good manner then further stages are facing various problems like less availability of routing resources, it is difficult to meet the desire timing requirements which results in more number of iterations and takes more memory for the design and CPU runtime.

Floorplanning is initial stage of any hierarchical physical design. The main goal of the floor planning is to create a finalized prototype. prototyping involves multiple iterations with focus on the routability and timing constraints [3]. Generally, the top-level VLSI chip planning is done by using different prototypes, for each prototype estimate congestion and timing constraints based on quick placement and global routing. There are few millions of gate-level logic units, R.Otten proposed a method called “Automatic floorplan design" in the year of 1982 [4]. Many of new algorithms and methods are implemented in the Floorplanning stage, such as simulated annealing algorithm in [5] and incremental guided Floorplanning algorithm with effectively reduce the IR-drop violations with the help of B*-tree representation in [6], and P/G(power and ground) network and Floorplanning method for fast design convergence in [7]. Even though by using this algorithms and methods taking more amount of time and doing more iterations. Using a method of Flex model-based method reduces unnecessary instances which improves run time and CPU in chip planning stage [1]. However, it is also taking more iterations. To Improve more effective run time and peak memory usage we are using Blackbox model-based floor planning which will reduce runtime and CPU peak memory. This project is done on Cadence encounter tool.

II. EXISTING METHOD

Flexmodel based heirarchical Floorplanning with active logic reduction technology is one of the method in the design VLSI heirarchical floor planning. In the flexmodel based heirarchical Floorplanning uses Flexfillers for masking the unwanted instances in the design. Flexfiller is used to mask the various combinational logic levels between reg2reg logic path in whole design which results in reducing the instances during top level chip planning. If the number of instances are reducing then the EDA tool take less time to get required optimized top level floor planning.

After completing top level chip heirarchical Floorplanning with required prototype the Flexfillers are removed and remaining stages i.e. partitioning, individual block design, assemble the design, optimize the design and signoff are same as traditional hierarchical physical design flow.

Fig.1 Physical view of flexfiller

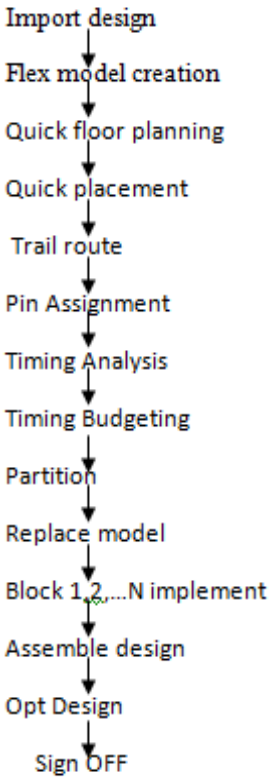

Fig.2 Flexmodel based hierarchical floorplanning Flow

III. PROPOSED METHOD

The Blackbox generally is a hard constraint. Blackbox having more advantages. Generally, Blockbox is used for defining a module which is having partial netlist, empty module in the design and used for hierarchical partitioning in the design. Blackbox can resized, reshaped and pins can also be assigned. This can also be used in the hierarchical physical design Floorplanning prototype model creation.

In the Blackbox model style floor planning each Blackbox can be created Based on analysis of the hierarchical design netlist and design constraints. After creating Blackbox the design looking like partition blocks and we assigned pins for Blackbox. For each and every module area constraints are given while Blackbox is created which is having with very less amount of time. In the top level hierarchical physical design chip planning the designer engineer not consider each individual block netlist because each individual block is designed and optimized (done PnR) by block level engineer. As top-level chip plan engineers main concentrate on critical timing path between module and making sufficient channel between modules. so, for reason we are masking the internal logic of each block by using Blackbox modeling. After top level chip Floorplanning is completed by using this Blackbox model. we got a smaller number of instances after model creation. In this way we reduced more number of instances which makes the prototype Floorplanning with less run time and CPU memory usage.

IV. BLACKBOX MODEL BASED FLOORPLANNING PROCEDURE

1.First import the design on the EDA Tool After importing the design we can get the Design Hierarchy of the imported design.
2.After that we can create Blackbox for each and every module and assigning pins to Blackbox.
3.Initial Floorplanning by using Automatic floorplan synthesis is placing the Backboxes and creating channel between Blocks.
4.Run Placement in Floorplan mode perform global placement of cells.
5.Run trail route perform global route for the design to analyze congestion and pins are assigned according to the routing, adjust the floor until meet the design with congestion free.
6.Timing analysis check the requirements of timing constraints.
7.Timing budgeting do the optimization on critical nets and gives the design requirements with good prototype floor planning.

This project is done only for Floorplanning stage, After that remaining stages are same as the flow shown in the figure [3].

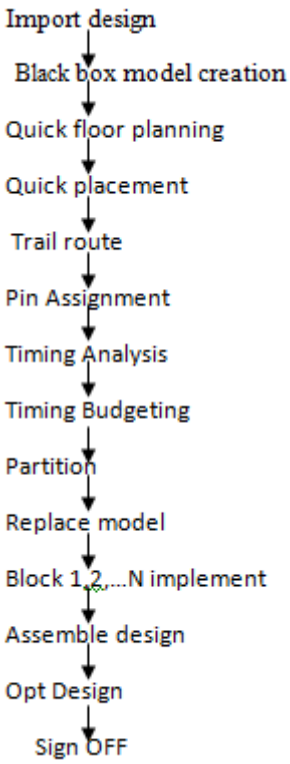

Fig.3 proposed model flow

V. RESULTS AND ANALYSIS

The main aim of this work is to reduce number of instances, CPU run time and peak memory and maintain the quality of Floorplanning in the Floorplanning stage by using black box model creation.

The number of instances before model creation is 5981 and after model creation it becomes 348 is show in figure [4,5].

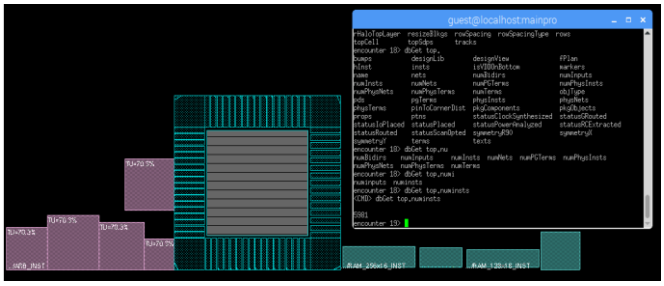

Fig.4 Instance count without model creation

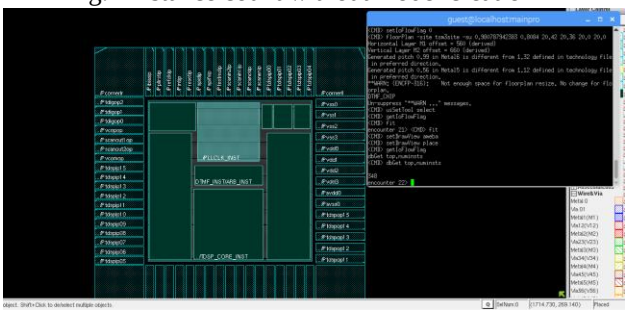

Fig.5 Instance count after model creation

BlackBox model based prototype floor plan for the design is shown in the following figure [6].

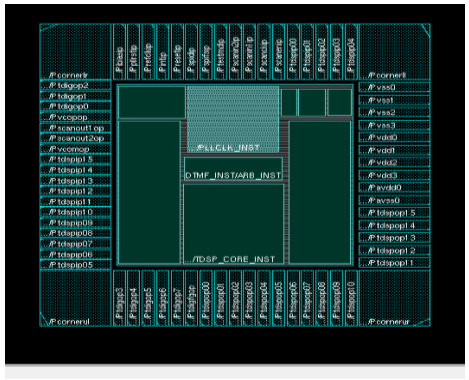

Fig.6 prototype floorplan plan design

There are various stages are there before obtaining finalized prototype of design. The following figure [7]. And also comparing the memory improvement in without model and with model shown in figure [8]. we got 0.015% vertical congestion and 0.010% horizontal congestion.

Parameters	without model	With model	CPU run time improvement
Number of instances	5981	348	N/A
Model creation	N/A	1.2min	N/A
Initial plan	12.35min	1.24min	9.95
Global place	4.35min	0.38min	11.44
Trail route	5.03min	0.58min	8.67
Pin Assignment	0.45min	0.23min	1.95
Time budgeting	10.54min	0.55min	19.16
Total Floor plan time	32.72min	4.18min	12

Fig.7 Runtime comparision of each step-in floorplan

Parameter	Without model	With model	Memory Improvement
Peak memory	997.5Mb	324.2Mb	3.07

Fig.8 memory improvement of without model and with model

Parameter	Existing method improvement	Proposed method improvement
Total run time for floorplan	5.57	12.00
Peak memory	2.22	3.07

Fig.9 comparison of existed method and proposed method

VI. CONCLUSION

Blockbox model mask the internal netlist of block logic which is not required in the Floorplanning because in the chip level Floorplanning each and every block inside logic optimization not necessary it is optimizing while individual block PD flow. As top-level chip planning main concentrate on various constraints. Blockbox model based method main advantage is it reduces more number of instances compared to flexmodel based model during the Floorplanning. As number of instances are less EDA tool is taking less CPU runtime and memory requirements which are more cost effective functions in the design. This model is very useful while dealing with bigger chips Floorplanning.

VII. FUTURE SCOPE

With the help of System architecture interface information based floor planning method with Blackbox modeling gives the best quality with less CPU runtime and memory.

REFERENCES

1. Y.Zhou,Y.Yan, and W.Yan "A method to speed up VLSI Hierarchical physical design in Floorplanning",2017 IEEE International Conference on asic. **DOI:**.10.1109/ASICON.2017.8252484.
2. S.N. Adya and I.L. Markov, "Fixed-outline Floorplanning: Enabling Hierarchical Design", *IEEE Trans. on VLSI 11(6)*, pp. 1120-1135, 2003. **DOI:**10.1109/TVLSI.2003.817546
3. Zhang K."Challenges and opportunities in nano-scale VLSI design", *IEEE VlSI-TSA International Symposium on VlSI Design, Automation and Test*, pp.6-7, 2005. **DOI:**10.1109/VDAT.2005.1500005
4. R. Otten. "Automatic floorplan design," *19th Design Automation Conference*, pp.261-267, 1982. **DOI:**10.1109/DAC.1982.1585510
5. D.F. Wong, C. Liu. "A new algorithm for floorplan design," *23th Design Automation Conference*, pp. 101-107 1986. **DOI:**10.1109/DAC1986.1586075
6. C.-W.Liuand Y.-W.Chang, "Floorplanand power/ground network cosynthesis for fast design convergence," *in Proc. of ISPD*, pp.86, 2006 **DOI:**10.1109/TCAD.2007.892336
7. Chang B, Jigang W, Srikanthan T, et al. "Fast evaluation-basedalgorithm for fixed-outline Floorplanning", *Computer Engineering and Technology (ICCET), 2010 2nd International Conference on. IEEE*, pp.V2-81-V2-85,2010.**DOI:**10.1109/ICCET.2010.5485310
8. . Innovus (Encounter) User Guide, Product Version 16.21, 2017.

AUTHORS PROFILE

Rajasekhara Reddy Reddy was graduated from Vignan's Lara Institute of Technology and Science,JNTU Kakinada. And pursuing M.Tech specialization in VLSI & Embedded Systems in Lakireddy Bali Reddy College of Engineering (Autononomous) , Mylavaram, Andrapradesh.

Srinivasulu Gundala was completed graduation in 2000, He was completed post-graduation in communication engineering in 2004,Ph.D. in VLSI Design from JNTUA, Anantapur, Andrapradesh. He has 15 Years of teaching experience.