International Journal of Engineering and Advanced Technology (IJEAT)
ISSN: 2249-8958 (Online), Volume-8 Issue-6, August, 2019

Power and Delay Estimation of universal and Exclusive gates using Static and Dynamic CMOS Design

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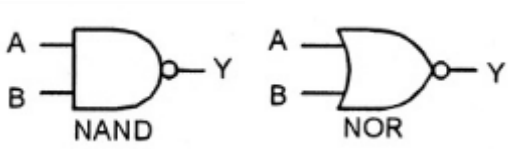
Abstract*: *In this paper, designing the universal gate and exclusive gates using static, pseudo nmos and dynamic cmos design and calculate the power and delay by using microwind simulator. We can implement any Boolean functions as well as basic gate using universal gates NAND and NOR .exclusive gate XOR and XNOR are used for error detection and correction in digital communication circuits.

Keywords* : *-NAND,NOR,XOR,XNOR,Power,Delay ,microwind

I. INTRODUCTION

A universal logic gate is a logic gate that can be used to construct all other basic logic gates. NAND and NOR is the combination of complement AND and complement OR operation. Universal gates are not associative but commutative in nature. The NAND gate operation is the inverse operation of AND gate .when both the inputs are '0', the output is '0', both the inputs are '1' the output is '0'and one of the input is '0' the output is '1'. The NOR gate operation is the inverse operation of OR gate .when both the inputs are '0', the output is '1', both the inputs are '1' the output is '0'and one of the input is '0' the output is '0'.from this , we can easily perform the basic gates operation[5]. The symbol used to represent the NAND and NOR gate as shown in the figure.



The exclusive gates are used to check or compare the inputs. The exclusives gates are otherwise known as unique gates performing true or false operation. The XOR gate operation is the true input and output operation. When both the inputs are '0', the output is '0', both the inputs are '1' the output is '0'and one of the input is '0' the output is '1'. The XNOR gate performs logical equality .when both the inputs are '0', the output is '1', both the inputs are '1' the output is '1'and one of the input is '0' the output is '0'. The symbol used to represent the XOR and XNOR gate as shown in the figure

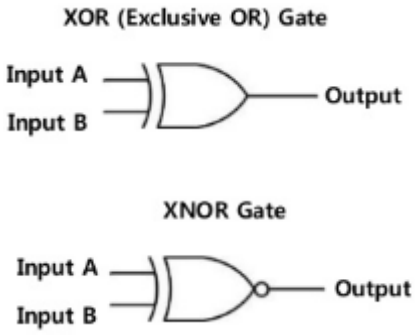


Table -1 Truth table for universal and exclusive gates

INPUTS		OUTPUTS			
A	B	NAND	NOR	XOR	XNOR
0	0	1	1	0	1
0	1	1	0	1	0
1	0	1	0	1	0
1	1	0	0	0	1

II. CMOS Design

A. Static CMOS Design

Static CMOS gates are otherwise known as conventional CMOS. It consists of PMOS network as pull up network and NMOS network as pull down network. The pull up network always pull-up the output and pull down network pull down the output. The operation of PMOS is as follows, when the input is low, the PMOS is ON state otherwise it is in OFF state. The operation of NMOS is as follows, when the input is high, the NMOS is ON state otherwise it is in OFF state. CMOS has low Static power dissipation because of leakage current[1].

B. Dynamic CMOS Design

The Dynamic CMOS design uses the clock for transition of input and output. During precharge, the clock is 0, so the clocked pMOS is ON and initializes the outputY high. During evaluation, the clock is 1 and the clocked pMOS turns OFF. It has low capacitance and no contention during switching . CMOS circuits has short circuit dissipation. The current pulse flow between supply and ground. CMOS circuits has no switching means there is no dynamic power dissipation. [3].

Revised Manuscript Received on October 30, 2019.

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C. Pseudo NMOS

In this pseudo NMOS, the PMOS is always connected to the ground and it act as load; the PMOS is always in ON state . The PMOS occupies large area and produce large capacitance; it leads to delay in producing output. If the PMOS is connected to the ground means it reduces delay. High speed and low transistor count is the main advantage of pseudo NMOS.[2]

III. CMOS CIRCUITS

A. UNIVERSAL GATE USING STATIC CMOS DESIGN

NAND:In static CMOS design, the pull up transistor is connected in parallel and pull down transistor is connected in series. When both the inputs are low, both PMOS is ON state, the output is high. When both the inputs are high , both NMOS is ON state, the output is low. When one of the input is low, one of the PMOS is in ON state, the output is high.[5]

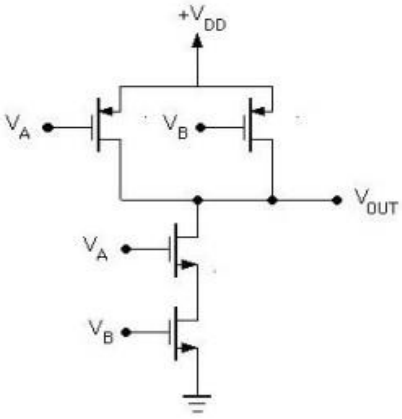

Fig. 1. CMOS NAND Using static cmos

NOR In static CMOS design, the pull up transistor is connected in series and pull down transistor is connected in parallel. When both the inputs are low, both PMOS is ON state, the output is high. When both the inputs are high, both NMOS is ON state, the output is low. When one of the input is low, one of the PMOS is in ON state, the output is low.

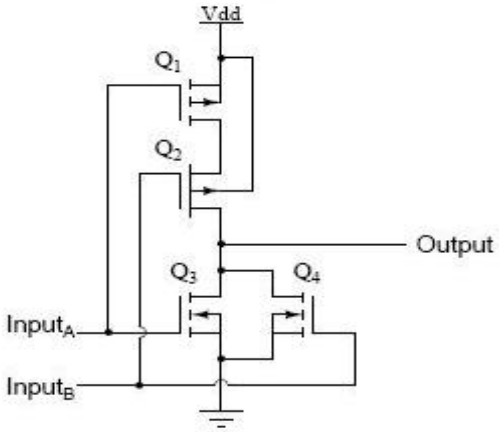

Fig. 2. CMOS NOR Using static cmos

B. UNIVERSAL GATE USING DYNAMIC CMOS DESIGN

In this footed Dynamic logic, you have only PDN network. So during precharge period (Φ=0), PDN network is idle and charging through PMOS can occur more slowly than static CMOS logic. Therefore, PMOS transistor can have small width.

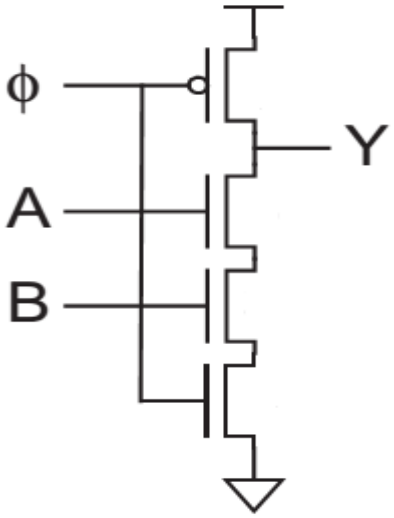

Fig. 3. CMOS NAND Using dynamtic cmos

In precharge, the clock is low, the output is always high . In evaluate, the clock is high and PMOS is in OFF state. The load capacitance first charging and then discharging at every clock cycle. The dynamic power is proportion to the clock rate. The dynamic power dissipation is minimized by the load capacitance.[4]

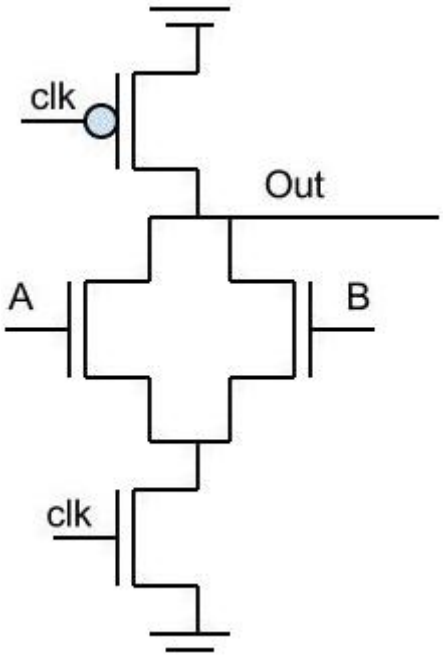

Fig. 4. CMOS NOR Using dynamtic cmos

C. EXCLUSIVE GATES USING STATIC CMOS DESIGN

In static method, the XOR and XNOR gate requires more transistors to implement[8]. The input A,ABAR,B,BBAR, it requires 8 transistor . XOR and XNOR gates has 4 Fan in and one Fan out .Static CMOS XOR and XNOR gate is shown in figure 5 and 6.

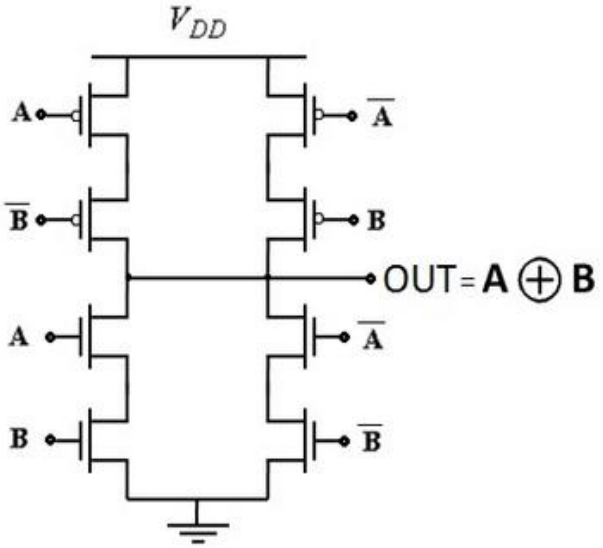

Fig. 5. CMOS XOR Using static cmos

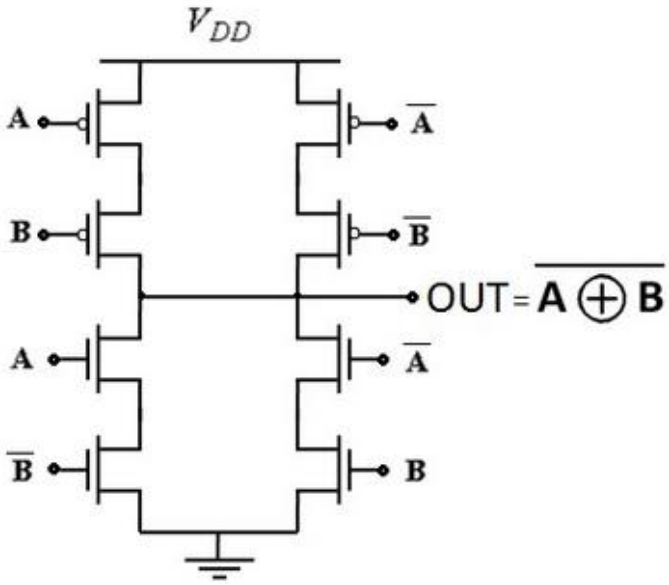

Fig. 6. CMOS XNOR Using static cmos

D. EXCLUSIVE GATES USING DYNAMIIC CMOS DESIGN

In dynamic method, the XOR and XNOR gate requires transistors less when compared to static to implement.[9]

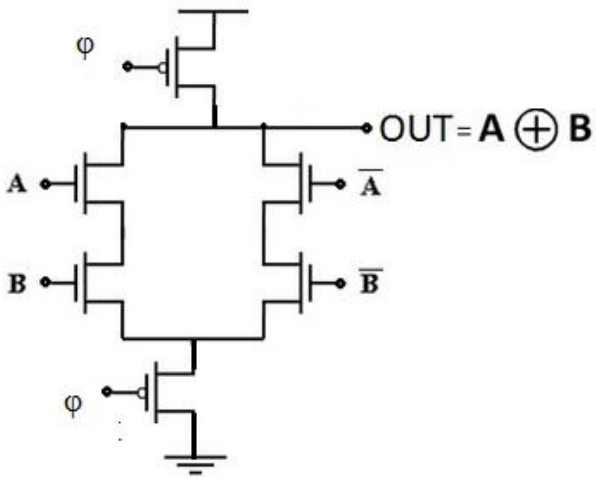

Fig. 7. CMOS XOR Using Dynamic cmos

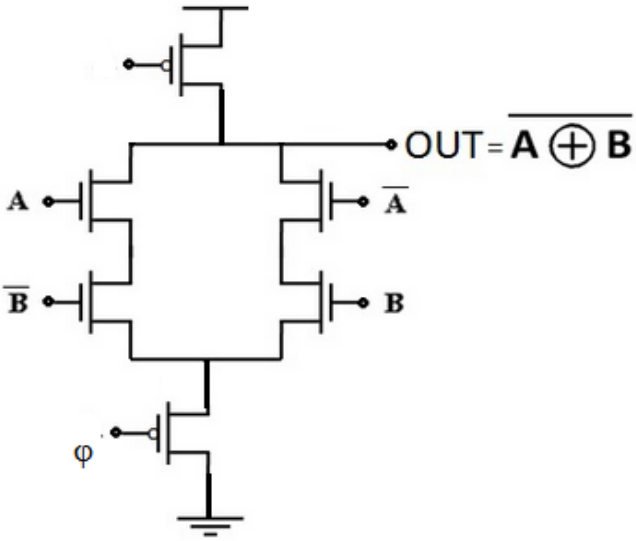

Fig. 8. CMOS XNOR Using Dynamic cmos

E. UNIVERSAL GATES USING PSEUDO NMOS

In this pseudo NMOS, the power dissipation is low compared to other techniques. The logical effort is equal to 16/9. where the output remains '1' in most of the time

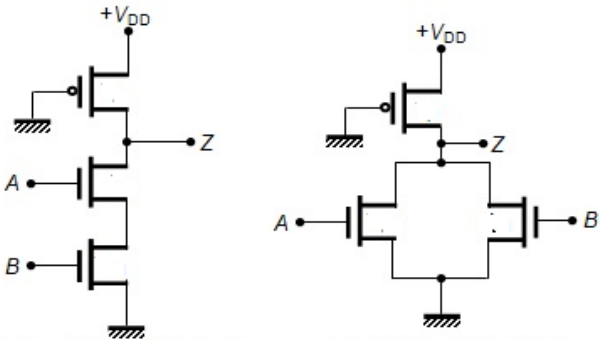

Fig. 9. CMOS NAND and NOR Using Pseudo nmos

F. EXCLUSIVE GATES USING PSEUDO NMOS

In this method, the PMOS always in ON state . the input changes from '1' to '0' or '0' to '1', it leads to output high. When both the inputs are low or high, the output is low in XOR and When both the inputs are low or high, the output is high in XNOR due to switching. [10]

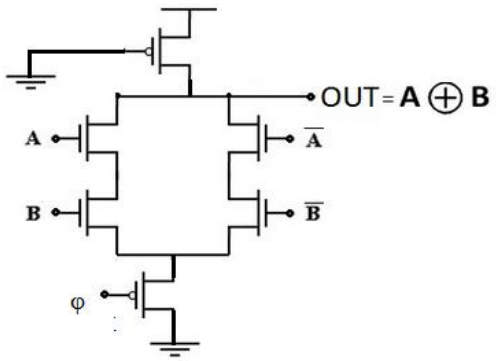

Fig. 10. CMOS XOR Using Pseudo nmos

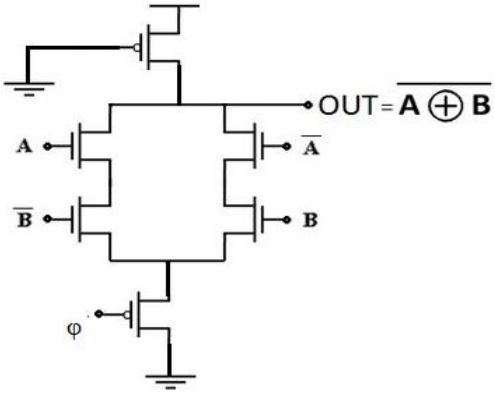

Fig. 11. CMOS XNOR Using Pseudo nmos

IV. COMPARISON

Table -2 Comparison In Terms of Power

CMOS DESIGN	NAND	NOR	XOR	XNOR
Static	**1.463µW**	**1.8 µW**	**1.51 µW**	**2.53 µW**
Dynamic (unfooted)	**0.010 µW**	**0.11 µW**	**0.052 µW**	**0.052 µW**
Dynamic (footed)	**0.21 µW**	**0.143 µW**	**0.024 µW**	**0.024 µW**
Pseudo NMOS	**0.128 µW**	**0.109 µW**	**0.052 µW**	**0.055 µW**

Table -1 Comparison In Terms of Average Delay

CMOS DESIGN	NAND	NOR	XOR	XNOR
Static	**0.176 ns**	**0.172 ns**	**0.3 ns**	**0.279 ns**
Dynamic (unfooted)	**0.098ns**	**0.18ns**	**0.298ns**	**0.298ns**
Dynamic (footed)	**0.56ns**	**0.62ns**	**0.76ns**	**0.76ns**
Pseudo NMOS	**0.77ns**	**0.85ns**	**0.91ns**	**0.92ns**

V.CONCLUSION

The design of universal gate and exclusive gates using static pseudo nmos and dynamic cmos design completed. The power and delay of this design are calculated by using microwind simulator. From this simulation result.
the static power is quite high than dynamic power but the leakage power in dynamic circuits is high.

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AUTHOR PROFILE

Surya.A is working as an Assistant professor, Department of Electronics and communication Engineering in Anjalai Ammal Mahalingam Engineering College. She published national and International journal and presented papers in national and international conference.