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PV Based Asymmetrical Cascade Three Phase Nine Level Multi Level Inverter Fed Induction Motor

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Abstract*: Motor performance and life is decreased due to presence of harmonic in the output voltage. Many inverter topologies were proposed for industrial drives application. PV based three phase asymmetrical cascade nine level inverter fed induction motor is proposed in this article. The proposed circuit has one dc source derived from PV with MPPT and nine level inverter with reduced components. The PV output voltage is regulated with help of boost converter using MPPT algorithm. The proposed inverter has unequal voltage source 1:2:4 ratios. The fundamental frequency modulation method is used for control the inverter output voltage. The proposed multi level inverter has less switching device and diode compare than other multilevel inverter topology. The circuit is modified further by replacing switching device with diode in the source section for reducing switching count; as a result, the control algorithm and driver circuit complexity are reduced further. The circuit performance is verified with help of simulation results.

***Index Terms*: PV source, Boost converter,Multi level inverter, Harmonic,Induction motor and MPPT technique.**

I. INTRODUCTION

Due to power demand and advancement of power semiconducting device availability increasing the research for developing power supply from renewable energy sources [1]. Many converters were developed for interfacing low voltage dc into high voltage dc for PV applications. Boost converter is the simple and best converter for low power applications. The boost converter is used to control the dc link voltage and maintains the constant voltage any variations occur in PV side [2]. The optimized PV energy is obtained with help of MPPT method. The inverter is used to convert DC into AC supply.Different inverter topologies were developed for reducing the harmonic and increase the voltage rating in [3-5]. Each topology has some merits and a demerit. Cascade multi level inverter is required more no of switches and dc power supply compare than other two methods . Many multi level inverter topologies are proposed for reducing the switches and DC power supply count.

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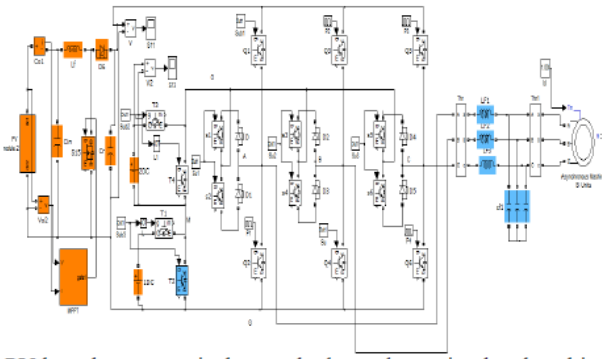
Asymmetrical topology is proposed for reducing the dc power supply and H-bridge count. In this method the voltage source is taken unequally . This topology is used to reduce the system cost, size and control system complexity. Hybrid multi level inverter topology is also proposed for reducing the components and voltage source of the inverter .

Bi-directional switches are used in the hybrid MLI to reduce the components count and improve the system performance [. These bi-directional switches are conducts in both directions. Many control method was developed for improve the switching sequence and system performance. In this paper PV based asymmetrical cascade three phase nine level multi level inverter fed induction motor is proposed for reducing the components count and reduce the system losses. The next sections explain the circuit operation, simulation results and conclusions one by one.

II. PROPOSED METHOD



PV based asymmetrical cascade three phase nine level multi level inverter fed induction motor circuit diagram is as shown in fig 1. This circuit is derived from three phase two level inverter. It consists of PV source, Boost converter, MPPT controller; two dc sources 1:2 ratios, bi-directional switches and two level inverter. The PV energy is regulated with help of boost converter using MPPT technique. The bi-directional switches are used to block the high voltage and easy current flow from mid point to other directions. The fundamental frequency modulation method is used to control the proposed nine-level inverter output voltage. The required output voltage level is achieved by turn on the corresponding switch and source. The switching states are as shown in Table-1. The detailed operation is explained in [21]

The inverter line-to-ground voltages Vag, Vbg , and Vcg in terms of switching states Sa, Sb, and Sc are given by

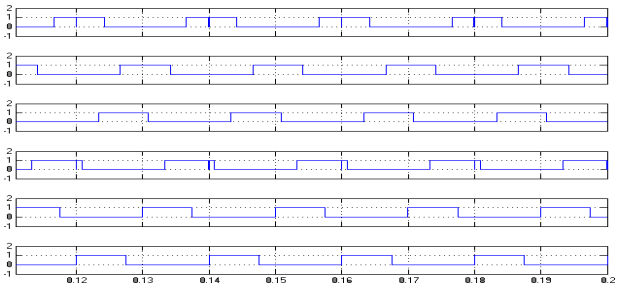
where N = 5 is the maximum number of voltage levels.

$$\begin{bmatrix} v_{ag} \\ v_{bg} \\ v_{cg} \end{bmatrix} = \frac{4V_{dc}}{N-1} * \begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix}$$

The balanced load voltages can be achieved if the proposed inverter operates on the switching states depicted in Table I. This inverter has 24 different modes within a cycle of the output waveform. According to Table I, it can be noticed that the bidirectional switches operate in 18 modes. For each mode, there is no more than one bidirectional switch in on state.As a result, the load current commutates over one switch and one diode (for instance: in (410), the load current *I*b can flow in S3 and Db1 or S4 and Db2).

Table 1: 3 phase nine level inverter switching pattern

	q1	q2	q3	q4	q5	q6	S1	S2	S3	S 4	S5	S6
4Vdc	1	0	1	0	0	1	1	1	0	0	0	0
3Vdc	1	0	0	0	0	1	0	0	1	1	0	0
2Vdc	1	0	0	0	0	1	0	0	1	1	0	0
Vdc	1	0	0	0	0	1	0	0	1	1	0	0
0Vdc	1	0	0	1	0	1	0	0	0	0	0	0
-Vdc	0	1	0	0	1	0	0	0	1	1	0	0
-2Vdc	0	1	0	0	1	0	0	0	1	1	0	0
-3Vdc	0	1	0	0	1	0	0	0	1	1	0	0
-4Vdc	0	1	0	1	1	0	1	1	0	0	0	0



Driving pulse for switch q1, q2, q3, q4, q5, q6

The inverter line-to-line voltage waveforms *V*ab, *V*bc, and *V*ca with corresponding switching gate signals are depicted in Fig. 2 where $v_{ab}v_{bc}v_{ca}$are related to $v_{ag}v_{bg}v_{cg}$ by

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} * \begin{bmatrix} v_{ag} \\ v_{bg} \\ v_{cg} \end{bmatrix}$$

The inverter line-to-neutral voltages $v_{aN}v_{bN}v_{cN}$ may be expressed as

$$\begin{bmatrix} v_{aN} \\ v_{bN} \\ v_{cN} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} * \begin{bmatrix} v_{ag} \\ v_{bg} \\ v_{cg} \end{bmatrix}$$

It is useful to recognize that the inverter voltages at terminals *a*, *b*, and *c* with respect to the midpoint (*o*) are given by

$$\begin{bmatrix} v_{ao} \\ v_{bo} \\ v_{co} \end{bmatrix} = \begin{bmatrix} v_{ag} \\ v_{bg} \\ v_{cg} \end{bmatrix} - \begin{bmatrix} v_{og} \\ v_{og} \\ v_{og} \end{bmatrix}$$

where *V*og is the voltage at midpoint (*o*) with respect to ground (*g*). *V*og routinely fluctuates among three different voltage values

$$V_{og} = \begin{cases} 1V_{dc} & if\ S_a + S_b + S_b \le 5 \\ 2V_{dc} & if\ S_a + S_b + S_b = 6 \\ 3V_{dc} & if\ S_a + S_b + S_b \ge 7 \end{cases}$$

$1v_{dc}\ 2v_{dc}\ 3v_{dc}$ follows:

The given equations can be used to derive *d* and *q* voltage components for all inverter vectors:

$$V_q = \frac{4V_{dc}}{3(N-1)}\ (2S_a - S_b - S_c)$$

$$V_d = \frac{4V_{dc}}{\sqrt{3}(N-1)}\ (S_c - S_b)$$

$$V = V_q - JV_d$$

THD% of the output voltage can be calculated by

$$THD\% = \frac{\sqrt{\sum_{k=2}^{\infty} {V_k}^2}}{V_1} * 100\%$$

where *V*1 and *V*k are the fundamental component and harmonic order, respectively.

One semiconducting switch T2 is replaced with a diode from the proposed inverter circuit.

As a result the circuit control mechanism is simplified and driver circuit requirement is also reduced. The modified circuit diagram as shown in the fig 3.The modified inverter is also give the same performance with less conducting switch. The next section explains the simulation results.

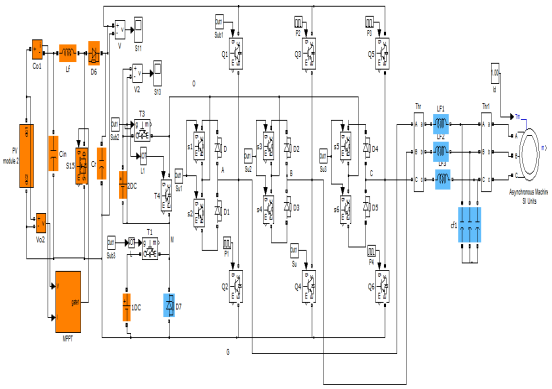


Figure3 Modified Nine level inverter circuit diagram.

Figure 1 shows the proposed nine level inverter fed induction motor circuit diagrams. The boost converter is used to convert low voltage dc into high voltage dc output. This output voltage is given to the inverter. The inverter is designed for 4kW power rating. The inverter circuit is used to convert dc supply into nine-level AC output. The LC filter is used to convert staircase output into sinusoidal output voltage and also reduce the harmonic and convert sinusoidal output voltage. Three phase induction motor power rating 3.75kW, 415V, 50Hz and 2 pole machine. The motor speed is plotted.

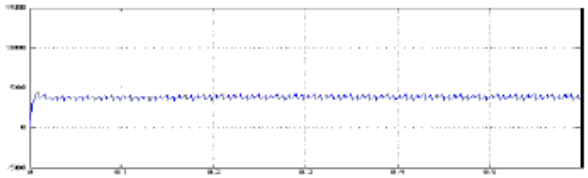


Figure 4 Boost converter output

Fig 4 shows the boost converter output voltage. Fig 5 shows the inverter output voltage across phase to phase before LC filter. Fig 6 shows the rotor current output. Fig 7 shows the rotor speed in RPM. It is settled at 1440 rpm. Fig 8 shows the torque output. It is settled at 5 N-m.

Figure 5 Inverter Phase to phase voltage before filter

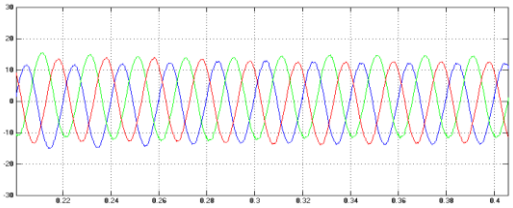


Figure 6 Inverter Current output

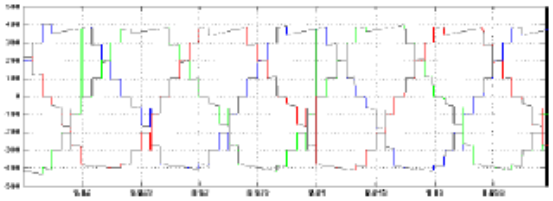


Figure 7 Motor rotor speed in rpm

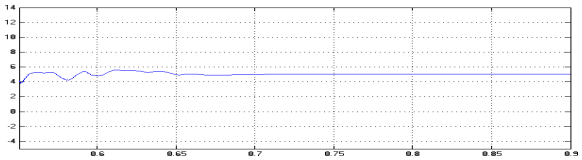


Figure 8 Induction motor Torque in Nm

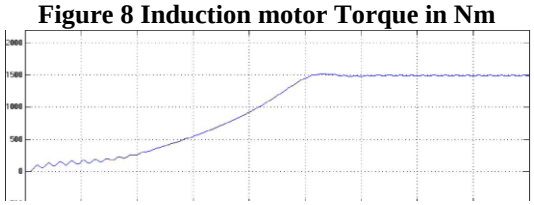


Figure 3 shows the Simu-link model of the modified nine level inverter circuit diagrams with using LC filter. One semiconducting switch T2 is replaced with a diode from the proposed inverter circuit. This circuit is used to convert dc supply into nine-level AC output. The LC filter is used to convert staircase output into sinusoidal output voltage and also reduce the harmonic. Fig 9 shows the inverter output voltage across phase to phase before LC filter. Fig 10 shows the rotor current output. Fig 11 shows the rotor speed in RPM. It is settled at 1440 rpm. Fig 12 shows the torque output. It is settled at 5 N-m.

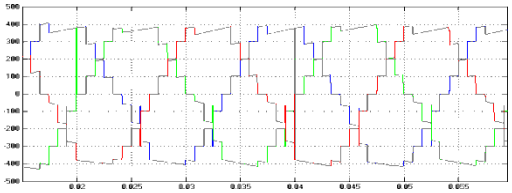


Figure 9 Inverter Phase to phase voltage before filter

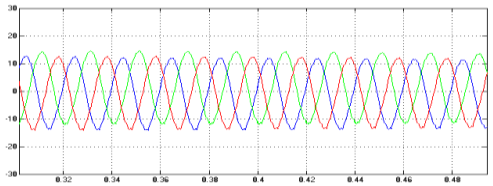


Figure 10 Inverter Current output

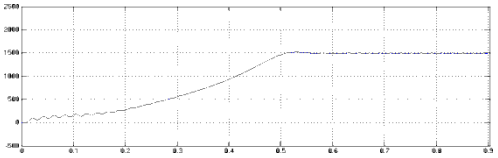


Figure 11 IM- rotor N / rpm

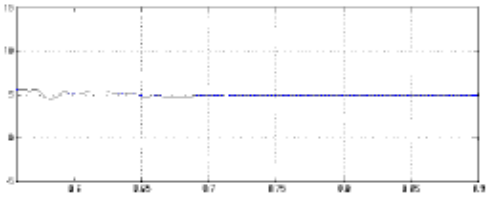
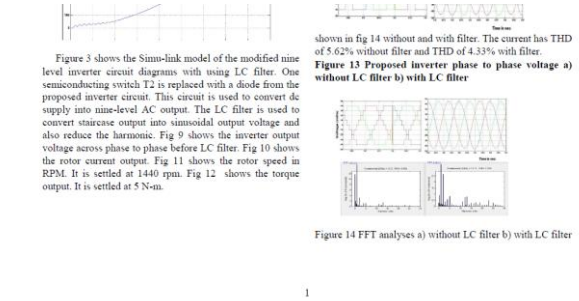


Figure 12 IM- T/ nm

III. RESULTS AND DISCUSSION

The circuit performance is compared from simulation results. The inverter output voltage is as shown in fig 13 using without filter and with filter. The voltage has staircase output and spike. This distortion and step wave is converted into sinusoidal form with help of LC filter. The current THD is as shown in fig 14 without and with filter. The current has THD of 5.62% without filter and THD of 4.33% with filter.



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shown in fig 14 without and with filter. The current has THD of 5.62% without filter and THD of 4.33% with filter.

Figure 13 Proposed inverter phase to phase voltage a) without LC filter b) with LC filter

Figure 14 FFT analyses a) without LC filter b) with LC filter

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Figure 13 Proposed inverter phase to phase voltage a) without LC filter b) with LC filter

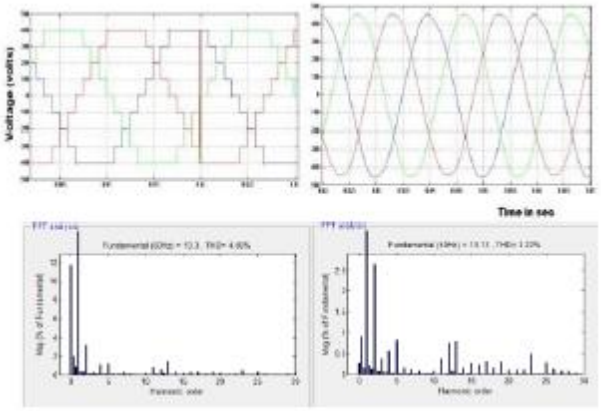

Figure 14 FFT analyses a) without LC filter b) with LC filter

The modified circuit performance is compared from simulation results. The inverter output voltage is as shown in fig 15 using without filter and with filter. The voltage has staircase output and spike. This distortion and step wave is converted into sinusoidal form with help of LC filter. The current THD is as shown in fig 14 without and with filter. The current has THD of 5.62% without filter and THD of 4.33% with filter. Both the proposed and modified circuit has same performance except switch count.

IV. CONCLUSION

PV based asymmetrical cascade three phase nine level multi level inverter fed induction motor were proposed in this paper. The circuit operation and simulation results were presented and discussed. The boost converter is used to fed 4Vdc power supply to the inverter. It is used to give constant and optimum output voltage from PV source with help of MPPT technique. The circuit performance is compared with simulation results. The modified three phase nine level inverter has less harmonic, less component count and less conduction loss compare than other lower level and nine level inverter . The circuit performance is verified with simulation results. The modified circuit produces more voltage spike in output voltage due to replacement of switch into diode. Need special consideration for spike arrester in the output voltage.

V. APPENDIX

Table.2 Simulation Parameters

Parameters	New 3ph 9-level without filter	New 3ph 9-level with diode	New 3ph 9-level with filter	New 3ph 9-level with diode and filter
DC source	3	3	3	3
Input voltage (4Vdc)	400V	400V	400V	400V
No. of switches	16	15	16	15
No. of Diodes	6	7	6	7
THD%	5.62	5.35	4.06	3.22

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Mr.M.Selvaperumal completed his Bachelors of Engineering Degree in Electrical and Electronics Engineering from Madras University in the year 2002 and Masters of Engineering in Power Electronics and Industrial Drive systems from Sathiyabama University, Chennai in the year 2005.Currently he is a research scholar in Electrical Engineering of Sathiyabama University. His full fledged interest is on the subjects PV based asymmetrical cascade 3 phase 9 level inverter circuits.

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