International Journal of Engineering and Advanced Technology (IJEAT)
ISSN: 2249-8958 (Online), Volume-8 Issue-6, August, 2019

Improved Fault Tolerant ALU Architecture

Shaveta Thakral, Dipali Bansal

Abstract: ***The birth to IC technology by Moore became driving force behind civilization and it spent almost 45 years successfully without any scruple in mind. It affected life of a mankind and brought pivotal moment in civilization. Now technology is hitting atomic levels and soon limits will be touched. Therefore time has come to rethink for an alternative solution that may slow down exponential rate demonstrated by Moore. Reversible computing is emerging as a superior technology and soon will be future of all smart computing applications. Although renowned physicists and computer scientists have investigated remarkable results in reversible logic based arithmetic logic unit (ALU) designing still research in the field of reversible ALU with add on fault tolerance is under progress and there is scope of further optimization. This paper aims in investigation of improved fault tolerant ALU architecture using parity preserving fault tolerant reversible adder (FTRA), double Feynman and conservative Fredkin gates. Performance evaluation of proposed architecture is done in respect of functionality, garbage lines, ancillary lines, quantum cost and number of gates. The quantum cost of all gates is verified using RCViewer+ tool. The proposed architecture is coded in Verilog HDL, Synthesized and simulated using EDA (Electronic Design Automation) tool-Xilinx ISE design suit 14.2.***

Index Terms: ***Fault Tolerant ALU, FTRA, Quantum, Reversible Computing, RCViewer+***

I. INTRODUCTION

Reversible logic is based on principle of no heat loss as randomness is avoided by mapping number of output lines same as input lines [1]. Smart and massive computing applications are demanding powerful and efficient deign of ALU. ALU designed with reversible logic saves power and suitable for portable systems. To avoid faults and errors in designed reversible logic based ALU, some techniques need to be employed. One of such technique is use of parity preserving logic based gates in complete designing process. Many renowned researchers have made their valuable efforts to design reversible logic based ALU but research work on reversible logic based ALU with add on fault tolerance property is investigated by very few. Thomsen et al [2] proposed ancillary and garbage free V-shape ALU design. Guan et al. [3] proposed optimized arithmetic and logic circuit with 32 arithmetic and logical operations which are highest in literature but fault tolerance is missing in their design. ALU architecture is designed with Morrison gate[4] but there is scope of improvement of its quantum cost yet other parameters are optimized. A significant study by Syamala and Tilak [5] demonstrated two approaches of ALU design. The first approach is based on control unit and another approach is based on multiplexer. A new reversible Vedic multiplier can be incorporated in design of ALU [6] and it is optimum balance of speed, power and energy. This Vedic multiplier will be helpful for smart and massive calculations in processors. Another effort in the area of fault tolerant design was proposed using "parity preserving reversible logic gates" [7]. Bashiri and Haghparast [8] proposed parity preserving reversible ALU using 22 gates. Rakshith and Saligram [9] proposed fault tolerant arithmetic logic unit using parity preserving logic but quantum cost is too high. Moallem et al. [10] provided another approach of designing arithmetic and logic unit but fault tolerance feature is not added to circuit. Sen et al. [11] proposed a modular approach for ALU design based on reversible multiplexer logic but unable to optimize it in terms of all metrics. The Proposed design [11] is also missing with fault tolerance property. Some researchers have proposed fault tolerant ALU architectures with new investigated "parity preserving reversible logic based gates "but not shown quantum implementation and therefore quantum cost of their proposed ALU remains unspecified. Mishra et al. [12] proposed fault tolerant ALU using UPPG gate and claimed 32 operations performed by their proposed design. There are some redundant operations in mentioned list [12]. It is concluded from literature survey that there is lot of scope for further improvement of performance of ALU. This paper presents improved fault tolerant ALU architecture with not only tremendous improvement in functionality but proves itself an optimum balance of quantum cost, ancillary inputs and garbage outputs. Proposed fault tolerant ALU architecture is designed based on conservative and parity preserving Fredkin, low quantum cost parity preserving based double Feynman and high functionality parity preserving based FTRA gates. Detailed discussion about these gates is presented in section A to C.

A. Fredkin Gate

It is 3x3 parity preserving and conservative reversible gate. It is parity preserving as "parity of input vector matches with parity of output vector" and as" number of 1's in input vector are equal to number of 1's in output vector". Hence it is also called conservative gate. It is also "one through gate" as one of its input is as it is received on output. If input vector of Fredkin gate is A, B, C and output vector is P, Q, R then "P=A", "Q=A'B XOR AC", "R= AB XOR A'C". The quantum cost of "Fredkin gate" is 5.

Revised Manuscript Received on October 30, 2019.
* Correspondence Author
Shaveta Thakral*, Department of Electronics & Communication Engineering, MRIIRS/ FET/ Faridabad, India.
Dipali Bansal, MRIIRS/ FET/ Faridabad, India.

It is used in designing of most of arithmetic and logic units as it standalone can act as AND gate, OR gate, NOT gate, XOR gate, XNOR gate and parity preserving multiplexer. It can also be utilized as parity preserving Toffoli structure when used along with F2G gate.

B. Double Feynman Gate (F2G/DFG)

It is 3x3 "parity preserving" reversible logic gate but not "conservative". It is also "one through gate" as one of its inputs is as it is received on output. If input vector of Double Feynman gate is A, B, C and output vector is P, Q, R then "P=A", "Q=A XOR B", "R= A XOR C". The quantum cost of "Double Feynman gate" is 2. It is used in designing of most of arithmetic and logic units as it can duplicate signal or invert signal or pass 0 or 1 as per logic requirement. It can also be utilized as parity preserving toffoli structure when used along with Fredkin gate.

C. FTRA Gate

It is 5x5 reversible logic gate .If input vector of FTRA gate is A, B, C, D, E and output vector is P, Q, R, S, T then "P=A", "Q= B", "R= A XOR B XOR C XOR D", "S = (A XOR B) (C XOR D) XOR (AB XOR D)", "T = (A XOR B) (C XOR D) XOR (A'B XOR D) XOR E". The quantum cost of "FTRA gate" is 8. It can work as full adder as well as full subtractor along with performing other logical operations; proving it to be a universal logic gate.

Summary of "parity preserving logic gates" used in proposed fault tolerant ALU architecture is presented in Table I. "Parity preserving logic gates" are presented with their optimized quantum implementation. Quantum cost of all gates is verified using RCViewer+ tool. Methodology of proposed architecture is given in section II. Operations performed by proposed architecture are given in section III. Performance evaluation of proposed architecture with existing design is given in section IV followed by conclusion in section V.

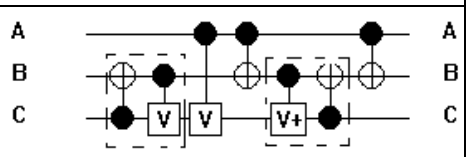
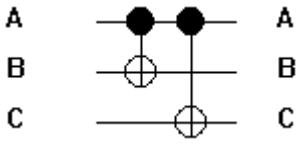
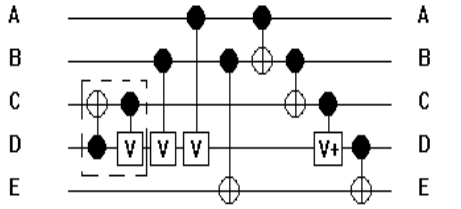
Reversible Logic Gate	Quantum Implementation
Fredkin	
Double Feynman	
Fault Tolerant Reversible Adder(FTRA)	

Table- I: Summary of "Parity Preserving Gates"

II. METHODOLOGY

The proposed fault tolerant ALU architecture is designed using nine parity preserving logic based gates including 5 Fredkin, 2 double Feynman and 2 FTRA gates. FTRA gate 1 is intended to perform logical operations depending upon various combinations of S2, S1 and So. FTRA gate 1 with input- output (I/O) signals is shown in Fig. 1.

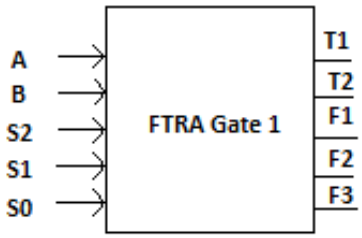


Fig.1: FTRA Gate 1

The various functions performed by "FTRA gate 1" are shown in Table II. FTRA gate performs various logical operations like "XOR", "XNOR", "AND", "NAND", "NOR", "OR", "comparison", "(A+B')", "(A'+B)", "(A'B)" and "(AB')" on F1, F2 and F3 output lines.

Table- II: Functionality of FTRA Gate 1

S2	S1	S0	F1	F2	F3
0	0	0	"(A'B+AB')"	"(AB)"	"(A<B)"
0	0	1	"(A'B+AB')"	"(AB)"	"(A+B')"
0	1	0	"(AB+A'B')"	"(A'B')"	"(A'+B)"
0	1	1	"(AB+A'B')"	"(A'B')"	"(A>B)"
1	0	0	"(A=B)"	"(A+B)"	"(AB')"
1	1	1	"(A'B+AB')"	"(A'+B')"	"(A'B)"

Fredkin gate 1 is acting as multiplexer. Fredkin gate 1 with I/O signals is shown in Fig. 2. S3, F1 and F2 are three inputs and F4 is desired output. G1 and G2 are garbage output lines.

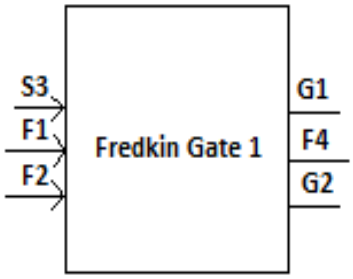


Fig.2: Fredkin Gate 1

The functionality of Fredkin gate 1as multiplexer is shown in Table III. It selects F1 or F2 depending upon S3. If S3 is 0, then F1 is selected; otherwise F2 is selected.

Table- III: Functionality of Fredkin Gate 1

S3	F4
0	F1
1	F2

Fredkin gate 2 is acting as multiplexer. S4, F4 and F3 are inputs and T3 is desired output. G3 and G4 are garbage output lines. Fredkin gate 2 with I/O signals is shown in Fig. 3.

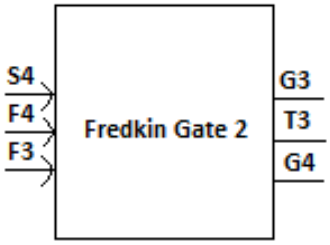


Fig. 3: Fredkin Gate 2

The functionality of Fredkin gate 2 is shown in Table IV. It selects F4 or F3 depending upon S4. If S4 is 0, then F4 is selected; otherwise F3 is selected.

Table- IV: Functionality of Fredkin Gate 2

S4	T3
0	F4
1	F3

Double Feynman gate 1 is used to avoid fan out. Henceforth it duplicate signal T3 and provides duplicated signal on Func1 as well as T4 output line. Double Feynman gate with various I/O signals is shown in Fig.4.

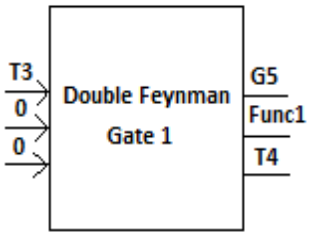


Fig. 4: Double Feynman Gate 1

The functionality of double Feynman gate 1 is shown in Table V. If S3S4 are "00", then F1 is passed on Func1 output line; else if S3S4 are "10", then F2 is passed on Func1 output line; else F3 is passed on Func1 output line.

Table- V: Functionality of Double Feynman Gate 1

T3	Func1/T4
F1	F1
F2	F2
F3	F3

Fredkin gate 3 is acting as swap gate. T4 and 0 are input lines and T5, T6 are desired output lines on which T4 and 0 can be swapped. G6 is garbage output line. Fredkin gate 3 with various I/O signals is shown in Fig. 5.

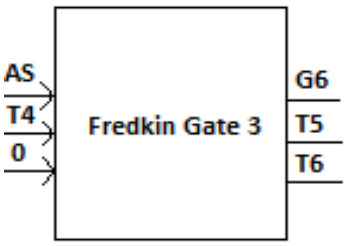


Fig. 5: Fredkin Gate 3

The functionality of Fredkin gate 3 is shown in Table VI. It swaps T4 and 0 inputs signals on T5 and T6 output lines if "AS" is 1; otherwise T4 signal is passed on T5 output line and 0 is passed on T6 output line.

Table- VI: Functionality of Fredkin Gate 3

AS	T5	T6
0	T4	0
1	0	T4

Double Feynman gate 2 is acting as copying gate if S5 is 0; otherwise it inverts signal T2. On T2 line, signal B is received from FTRA gate 1.T7 is desired output line. G7 and G8 are garbage output lines. Double Feynman gate2 with various I/O signals is shown in Fig.6.

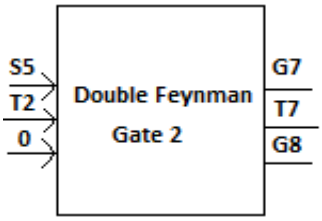


Fig. 6: Double Feynman Gate 2

The functionality of double Feynman gate 2 is shown in Table VII. Therefore B is received on T7 output line if S5 is 0; otherwise B' is received if S5 is 1.

Table- VII: Functionality of Double Feynman Gate 2

S5	T7
0	B
1	B'

Fredkin gate 4 is acting as multiplexer. S6 is select line. 0 and T7 are input lines and T8 is desired output line. Fredkin gate 4 with I/O signals is shown in Fig. 7.

Fig.7: Fredkin Gate 4

The functionality of Fredkin gate 4 is shown in Table VIII. It selects 0 or T7 depending upon S6. If S6 is 0, then 0 is selected; otherwise T7 is selected.

Table- VIII: Functionality of Fredkin Gate 4

S6	T8
0	0
1	T7

FTRA gate 2 is dedicated to perform arithmetic operations related to addition and subtraction. Adder is most important block of arithmetic and logic unit. Adder can be used to perform addition, subtraction, multiplication as well as division. T1, T8, T5, T6 and 0 are input lines on which operands are provided and Func2 is desired output line. Cout and Bout are output carry after addition and output borrow after subtraction respectively. FTRA gate with I/O signals is shown in Fig.8.

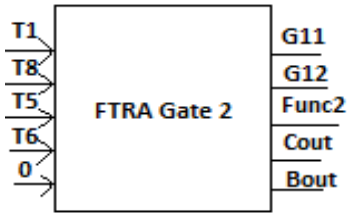


Fig. 8: FTRA Gate 2

The functionality of FTRA gate 2 is shown in Table IX. FTRA gate is acting as adder, when T6 is 0 and two operands are provided on T1 and T8 input lines and carry is provided on T5 input line. Same FTRA gate is acting as subtractor, when T5 is 0 and two operands are provided on T1 and T8 input lines and borrow is provided on T6 input line.

Table-IX: Functionality of FTRA Gate 2

T1	T8	T5	T6	Func2	Cout/Bout
A	B	Cin	0	A plus B plus Cin	Cout
A	B	0	Bin	A minus B minus Bin	Bout

Fredkin gate 5 is acting as multiplexer. AL is selection line. Func1 and Func2 are input lines and Func is desired output line. G13 and G14 are garbage output lines. Fredkin gate 5 with I/O signals is shown in Fig.9.

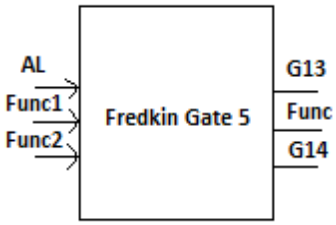


Fig. 9: Fredkin Gate 5

It selects Func1 or Func2 depending upon AL. If AL is 0, then Func1 is selected; otherwise Func2 is selected. The functionality of Fredkin gate 5 is shown in Table X.

Table- X: Functionality of Fredkin Gate 5

AL	Func
0	Func1
1	Func2

Proposed architecture is shown in Fig.10. Complete architecture is divided into two sections; dedicated logical block and dedicated arithmetic block. One FTRA gate (FTRA1) is dedicated to perform logical operations and another (FTRA2) is dedicated to perform arithmetic operations. Three Fredkin gates (FR1,FR2 and FR5) are acting as multiplexers and one Fredkin gate (FR3) is acting as swap gate depending upon AS signal so that if AS=0, then addition is performed and else subtraction is performed. Fredkin gate (FR4) along with double Feynman gate (DFG2) is passing B or B' or 0 depending upon S5 and S6 lines to FTRA2 gate. Double Feynman gate (DFG1) is duplicating functions performed by dedicated logical block to avoid fan out problem. Fredkin gate (FR5) is acting as multiplexer and generating desired operation depending upon AL signal (If AL=0; then logical otherwise arithmetic operations). Designed ALU proves itself to be reversible as it takes 17 input lines including 2 operand bits (A, B), 7 selection lines (S0-S6), 2 control lines (AS, AL) and six constant lines. Circuit produces 17 output lines including 14 garbage lines, one desired function line (Func), Carryout (Cout) and Borrow out (Bout) line.

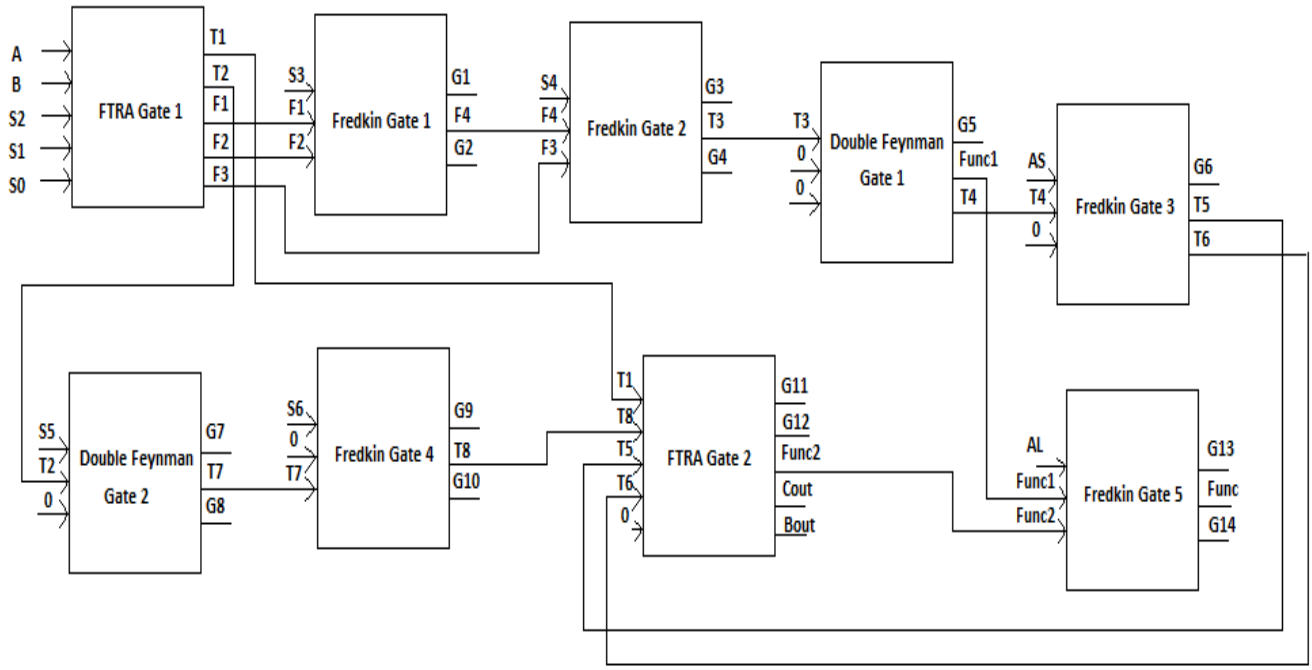


Fig. 10: Parity Preserving Logic Based ALU Design

III. OPERATIONS PERFORMED BY PROPOSED DESIGN

Operations performed by proposed ALU design are given in section A to G covering 73 operations including 13 logical and 60 arithmetic operations.

A. Logical Operations

Proposed ALU design performs 13 logical operations including bitwise and comparison related as shown in Table XI. For dedicated logical operations, AL=0 indicating logical operations are being performed. AS, S6 and S5 lines are put either 0 or 1. The 'X' indicated don't care means either 0 or 1 can be assigned to it.

Table- XI: Logical Operations

S4	S3	S2	S1	So	Func
0	0	0	0	1	"(A XOR B)"
0	1	0	0	1	"(A AND B)"
1	X	0	0	1	"(A + B')"
0	0	0	1	0	"(A XNOR B)"
0	1	0	1	0	"(A NOR B)"
1	X	0	1	0	"(A'+B)"
0	1	1	0	0	"(A OR B)"
1	X	1	0	0	"(AB')"
0	1	1	1	1	"(A NAND B)"
1	X	1	1	1	"(A'B)"
1	X	0	1	1	"(A>B)"
0	0	1	0	0	"(A =B)"
1	X	0	0	0	"(A<B)"

B. Arithmetic Operations (Set-1)

Proposed ALU design performs 10 arithmetic operations in set-1 as shown in Table XII. For dedicated arithmetic operations in set-1, AL=1 indicating arithmetic operations are being performed; AS =0 indicating arithmetic operations are related to addition; S6 line is put to either 0 or 1and S5 line is put to 0.

Table- XII: Arithmetic Operations (Set-1)

S4	S3	S2	S1	S0	Func
0	0	0	0	1	(A) plus (A'B+AB')
0	1	0	0	1	(A) plus AB
1	X	0	0	1	(A) plus (A+B')
0	0	0	1	0	(A) plus (AB+A'B')
0	1	0	1	0	(A) plus (A+B)'
1	X	0	1	0	(A) plus (A'+B)
0	1	1	0	0	(A) plus (A+B)
1	X	1	0	0	(A) plus (AB')
0	1	1	1	1	(A) plus (AB)'
1	X	1	1	1	(A) plus (A'B)

C. Arithmetic Operations (Set-2)

Proposed ALU design performs 10 arithmetic operations in set-2 as shown in Table XIII. For dedicated arithmetic operations in set-2, AL=1 indicating arithmetic operations are being performed; AS =0 indicating arithmetic operations are related to addition; S6 line is put to 1and S5 line is put to 0.

Table-XIII: Arithmetic Operations (Set-2)

S4	S3	S2	S1	S0	Func
0	0	0	0	1	(A) plus (B) plus (A XOR B)
0	1	0	0	1	(A) plus (B) plus (AB)
1	X	0	0	1	(A) plus (B) plus (A'B)'
0	0	0	1	0	(A) plus (B) plus (A XNOR B)
0	1	0	1	0	(A) plus (B) plus (A'B')
1	X	0	1	0	(A) plus (B) plus (AB')'
0	1	1	0	0	(A) plus (B) plus (A+B)
1	X	1	0	0	(A) plus (B) plus (A'+B)'
0	1	1	1	1	(A) plus (B) plus (A'+B')
1	X	1	1	1	(A) plus (B) plus (A+B')'

D. Arithmetic operations (set-3)

Proposed ALU design performs 10 arithmetic operations in set-3 as shown in Table XIV. For dedicated arithmetic operations in set-3, AL=1 indicating arithmetic operations are being performed; AS =0 indicating arithmetic operations are related to addition; S6 and S5 lines are put to 1.

Table- XIV: Arithmetic Operations (Set-3)

S4	S3	S2	S1	S0	Func
0	0	0	0	1	(A) plus (B') plus (AB+A'B')'
0	1	0	0	1	(A) plus (B') plus (AB)
1	X	0	0	1	(A) plus (B') plus (A OR B')
0	0	0	1	0	(A) plus (B') plus (A'B +AB')'
0	1	0	1	0	(A) plus (B') plus (A NOR B)
1	X	0	1	0	(A) plus (B') plus (A'+ B)
0	1	1	0	0	(A) plus (B') plus (A OR B)
1	X	1	0	0	(A) plus (B') plus (AB')
0	1	1	1	1	(A) plus (B') plus (A NAND B)
1	X	1	1	1	(A) plus (B') plus (A'B)

Arithmetic Operations (Set-4)

Proposed ALU design performs 10 arithmetic operations in set-4. As shown in Table XV. For Dedicated arithmetic operations in set-4, AL=1 indicating arithmetic operations are being performed; AS =1 indicating arithmetic operations are related to subtraction; S6 line is put to either 0 or 1and S5 line is put to 0.

Table- XV: Arithmetic Operations (Set-4)

S4	S3	S2	S1	S0	Func
0	0	0	0	1	(A) minus (A'B+AB')
0	1	0	0	1	(A) minus (AB)
1	X	0	0	1	(A) minus (A+B')
0	0	0	1	0	(A) minus (AB+A'B')
0	1	0	1	0	(A) minus (A+B)'
1	X	0	1	0	(A) minus (A'+B)
0	1	1	0	0	(A) minus (A+B)
1	X	1	0	0	(A) minus (AB')
0	1	1	1	1	(A) minus (AB)'
1	X	1	1	1	(A) minus (A'B)

Arithmetic operations (set-5)

Proposed ALU design performs 10 arithmetic operations in set-5. The different arithmetic operations performed by proposed design are shown in Table XVI. For Dedicated arithmetic operations in set-5, AL=1 indicating arithmetic operations are being performed; AS =1 indicating arithmetic operations are related to subtraction; S6 line is put to 1 and S5 line is put to 0.

Table-XVI: Arithmetic Operations (Set- 5)

S4	S3	S2	S1	S0	Func
0	0	0	0	1	(A) minus (B) minus (A B+A'B")'
0	1	0	0	1	(A) minus (B) minus (AB)
1	X	0	0	1	(A) minus (B) minus (A'B)'
0	0	0	1	0	(A) minus (B) minus (A'B+AB')'
0	1	0	1	0	(A) minus (B) minus (A'B')
1	X	0	1	0	(A) minus (B) minus (AB')'
0	1	1	0	0	(A) minus (B) minus (A+B)
1	X	1	0	0	(A) minus (B) minus (A'+B)'
0	1	1	1	1	(A) minus (B) minus (A'+B')
1	X	1	1	1	(A) minus (B) minus (A+B')'

G. Arithmetic operations (set-6)

Proposed ALU design performs 10 arithmetic operations in set -6. The different arithmetic operations performed by proposed design are shown in Table XVII. For Dedicated arithmetic operations in set-6, AL=1 indicating arithmetic operations are being performed; AS =1 indicating subtraction; S6 and S5 lines are put to 1.

Table-XVII: Arithmetic Operations (Set- 6)

S4	S3	S2	S1	S0	Func
0	0	0	0	1	(A) minus (B') minus (A XOR B)
0	1	0	0	1	(A) minus (B') minus (A AND B)
1	X	0	0	1	(A) minus (B') minus (A OR B')
0	0	0	1	0	(A) minus (B') minus (A XNORB)
0	1	0	1	0	(A) minus (B') minus (A NOR B)
1	X	0	1	0	(A) minus (B') minus (A'+B)
0	1	1	0	0	(A) minus (B') minus (A OR B)
1	X	1	0	0	(A) minus (B') minus (AB')
0	1	1	1	1	(A) minus (B') minus (A NANDB)
1	X	1	1	1	(A) minus (B') minus (A'B)

IV. PERFORMANCE EVALUATION

The performance evaluation of existing designs and proposed fault tolerant ALU architecture is done in terms of functionality, quantum cost, number of gates, garbage outputs and ancillary inputs. Highest number of operations reported in literature is 32 yet operations performed by proposed architecture are 73. The proposed circuit is designed with only nine gates yet minimum count reported in literature is 16[12]. Proposed ALU architecture took only six constant input lines yet minimum count reported in literature is 12[3]. Proposed circuit produces 14 garbage output lines yet minimum count reported in literature is 12[3]. The minimum quantum cost reported in literature is 70 [3] yet quantum cost of proposed fault tolerant ALU is 45. The simulation waveform for proposed ALU design is shown in Fig.11. The performance evaluation in terms of bar chart is given in Fig.12 for clear understanding and critical analysis.

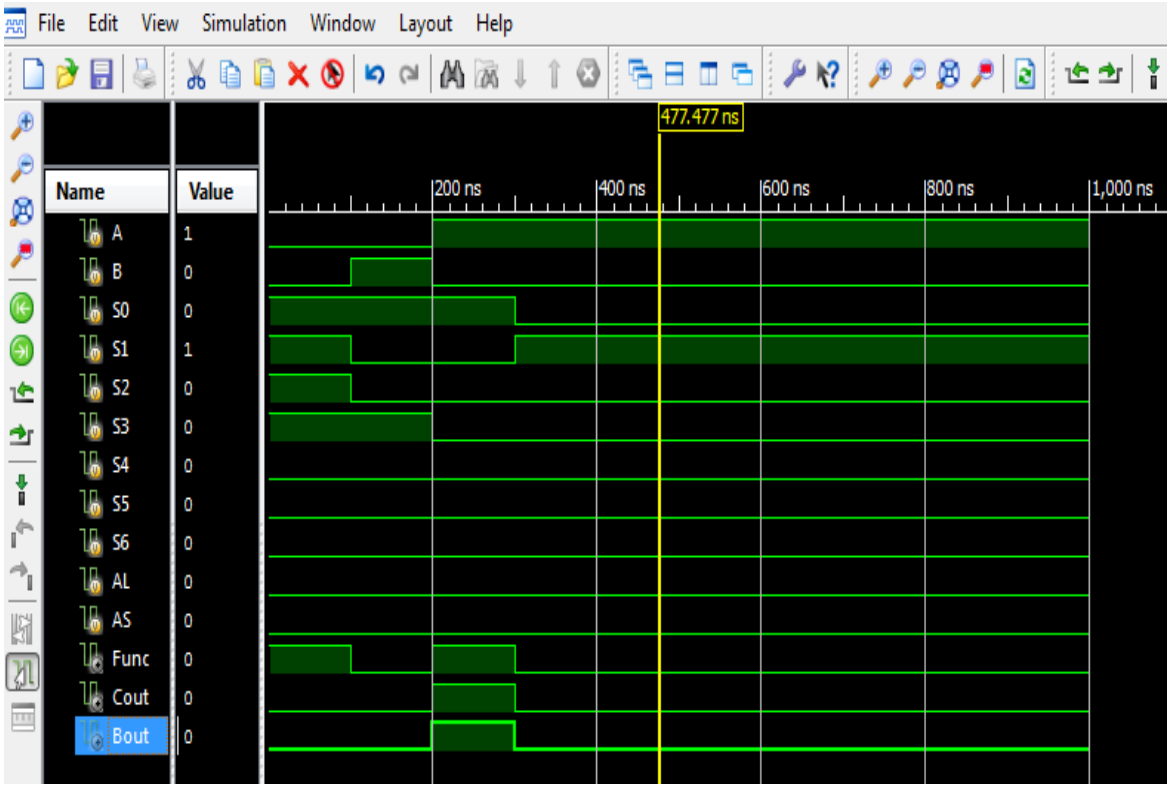


Fig. 11: Simulation Waveform of Proposed Fault Tolerant ALU

The proposed fault tolerant ALU design demonstrates 128% increase in functionality with 44% reduction in gates, 50% reduction in ancillary lines and 36 % reduction in quantum cost at the cost of 14% increase in garbage output lines as compare to other existing designs in literature. The Performance evaluation of designs under comparison is given in Table XVIII. The performance evaluation in terms of bar chart is given in Fig.12 for clear understanding and critical analysis.

Table- XVIII: Performance Evaluation

ALU Designs	Design I[3]	Design II[9]	Design III[12]	Proposed Architecture
No. of Gates	24	17	16	9
Quantum Cost	70	595	77	45
Arithmetic & Logic operations	32	32	32	73
Garbage outputs	12	37	25	14
Ancillary Inputs	12	33	25	6
Fault tolerance	No	Yes	Yes	Yes

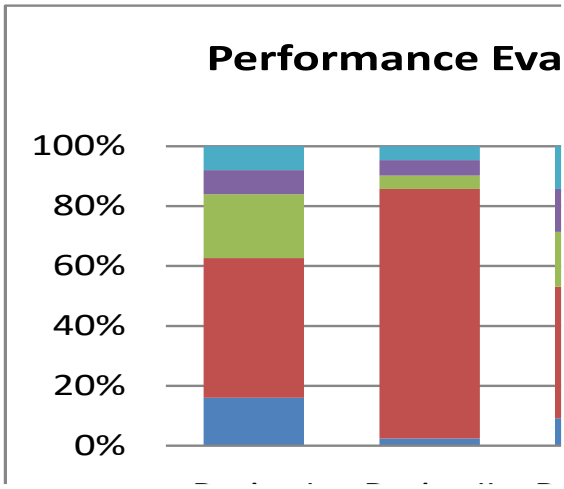


Fig.12: Performance Evaluation of Different ALU Designs

V. CONCLUSION

The proposed fault tolerant ALU architecture has two major advantages over existing designs. Firstly it produces more arithmetic and logical calculations and proves significant improvement in functionality. Secondly quantum cost of proposed circuit is least among all architectures. The proposed fault tolerant ALU design demonstrates 128% increase in functionality with 44% reduction in gates, 50% reduction in ancillary lines and 36 % reduction in quantum cost at the cost of 14% increase in garbage output lines as compare to existing fault tolerant ALU designs in literature.

The designed architecture is based on divide and conquers approach. Complete ALU design is splitted into two sections. One is dedicated logical block and other is dedicated arithmetic block. Control unit is designed using multiplexer which selects desired operation as per logic needed. The future scope of this research is to embed multiplier and divider in proposed ALU architecture.

REFERENCES

1. C.H.Bennett,"Logical reversibility of computation," *IBM Journal of Research and Development*, vol. 17, no.6, 1973, pp.525-532.
2. M.Thomsen, R.Glück and H.Axelsen,"Reversible arithmetic logic unit for quantum arithmetic," *Journal of Physics A: Mathematical and Theoretical.* Vol.43, no.38,382002, 2010
3. Z.Guan, W.Li , W.Ding , Y.Hang and L.Ni, "An arithmetic logic unit design based on reversible logic gates," *Communications, Computers and Signal Processing (PacRim), IEEE Pacific Rim Conference on.* Victoria, BC: IEEE, 2011, pp.925-931.
4. M.Matthew , L.Matthew , M.Richard and R.Nagarajan, "Design of a novel reversible ALU using an enhanced carry look ahead adder,"11th IEEE International Conference on Nanotechnology Portland Marriott. Portland, Oregon, USA, 2011
5. Y.Syamala and A.Tilak, "Reversible arithmetic logic unit," 101109/ICECTECH20115941987. Kanyakumari: IEEE, 2011, pp. 207-211.
6. A.Gupta , U.Malviya and V. Kapse," Design of speed, energy and power efficient reversible logic based vedic ALU for digital processors," *IEEE (NUiCONE),* 2012, pp. 1-6.
7. R.Saligram , S.S. Hegde, S.A. Kulkarni, H.R. Bhagyalakshmi and M.K Venkatesha ,"Design of parity preserving logic based fault tolerant reversible arithmetic logic unit," *International Journal of VLSI Design & Communication Systems*, vol.4, 2013, pp. 53-68.
8. R.Bashiri and M.Haghparast,"Designing a novel nanometric parity preserving reversible ALU," *Journal of Basic and Applied Scientific Research*, vol. 3, 2013, pp.572-580.
9. T.R.Rakshith and R.Saligram,"Parity preserving logic based fault tolerant reversible ALU," IEEE *Conference on Information & Communication Technologies*, 2013, pp.485–490.
10. P.Moallem, M.Ehsanpour, A.Bolhasani and M.Montazeri," Optimized reversible arithmetic logic units," *Journal of Electronics (China),* vol. 31, 2014, pp.394-405.
11. B.Sen , M.Dutta , M.Goswami and B. Sikdar,"Modular design of testable reversible ALU by QCA multiplexer with increase in programmability,"*Microelectronics Journal*,vol.45, 2014,pp.1522-1532.
12. N.K.Misra, S.Wairya and V.K.Singh ,"Approach to design a high performance fault-tolerant reversible ALU," *International Journal of Circuits and Architecture Design*, vol.2, no. 1,2016, pp.83-103.
13. S.Thakral and D. Bansal," Fault tolerant ALU using parity preserving reversible logic gates," *International Journal of Modern Education and Computer Science*, vol. 8, no. 8, 2016,pp.51-58.

AUTHORS PROFILE

Shaveta Thakral is presently working as an Associate Professor in Electronics & communication department, Faculty of Engineering and technology, MRIIRS, Faridabad. She obtained her BE in Electronics and communication from Lingayas Institute of management and Technology, Faridabad; MTECH from IASE Deemed University, Rajasthan. Currently she is pursuing PhD from MRIIRS, Faridabad. Her current research area includes Analog and Digital circuits, VLSI and Microprocessor. She has work experience of 14 years. She has published 30 research papers in prestigious indexed journals and conferences.

Dr. Dipali Bansal is presently Professor & associate Dean Academics, MRIIRS, Faridabad. She did her Bachelors in Electronics & Communication Engineering from BIT Sindri, a renowned and sought after learning hub and has also earned a PhD degree from Jamia Milia Islamia, New Delhi where she worked on Digital Signal Processing and its applications in home health care. She is a part of curiosity driven research group working in the field of bio-signal processing that brings together experimental and theoretical techniques and approaches in acquiring and analyzing human physiological parameters viz. ECG, EMG, EEG signals using professional tools like MATLAB and LabVIEW. Dr Bansal has over 70 publications in prestigious indexed journals and conferences, is mentor to 08 PhD scholars. She is also Reviewer of many international journals. Dr. Bansal is a member of various advisory boards at the University and is a motivational speaker at various forums.