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Implementation of Word Level Parallel Processing Unfolding Algorithm using VHDL

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Abstract: ***Aim of this paper is to apply the unfolding algorithm to FIR (Finite Impulse Response) and IIR (Infinite Impulse Response) filter and compare with original filter and parallel processing filters architecture. FIR filter and IIR filter are implemented by using VHDL (Very High Speed Integrated Circuit Hardware Description Language).In this paper, 2-parallel processing and 3-parallel processing of FIR and IIR filter are implemented and FIR and IIR filter are also implemented with unfolding factor 2 and unfolding factor 3 using VHDL. The simulation is done on Artix-7 series FPGA, target device (xc7a200tfbg676) (speed grade -1) using VIVADO 2016.3. Implemented design works on 1200 KHz clock whereas parallel inputs are generated on 3600 KHz clock. The proposed technique reduces the critical path delay in comparison with existing literature. Also, the experimental result shows that the speed for 3-unfolded IIR filter is more than 3-parallel IIR filter.***

Index Terms: DSP, FIR, FPGA, IIR, VHDL

I. INTRODUCTION

Speed is one of the important parameters in the performance of a device. The need for high speed devices increases as the demand for multimedia applications increase. To meet the demand for high speed, DSP (Digital signal processing) systems are used which uses different techniques like pipelining, parallel processing, unfolding etc. Applications of unfolding and parallel processing are, in receivers in communication system (GSM, spread spectrum receiver), radar, image processing, video processing, Military ESM (Electronic support measure) receiver operating in wide open configuration needs real time processing of intercepted radar signal (especially in VHF / UHF) [1],[2],[3]. Unfolding can be defined as it is a transformation technique that can be applied to a DSP program. As a result of this, get a new child program that newly child program describe more than one consecutive cycle (iteration) of the parent program. This is a graphical method or technique that tell about the hidden concurrencies of the program, so that the program can be run for a smaller cycle period with higher throughput [4], [5]. Parallel processing a technique where multiple inputs are processed to get multiple outputs. This is also a speed improvement technique that can be applied to any DSP program. The advantage of unfolding over parallel processing is that in unfolding loop iterations are possible where as in parallel processing only concurrent feed forward path processed simultaneously.

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II. DESIGN AND IMPLEMENTATION OF PROPOSED FIR AND IIR FILTERS

The data size of the input and multiplying coefficient is 6 bits that give 12 bits output. The main filter is working on 1200 kHz clock and wherever parallel input data needed, generated on 3600 kHz. These 1200 kHz and 3600 kHz clock are generated from 100 MHz system clock.

A. Design and implementation of the proposed 2-unfolded FIR filter

When we unfold the original FIR filter(Eq.(1)) using unfolding factor (J) = 2, we get two Equation 2 and Equation 3 that tells the 2 consecutive iterations of the original FIR filter.

$$y(n)=ax(n)+bx(n-4)+cx(n-6) \quad (1)$$

$$y(2k) = ax(2k)+ bx(2k-4)+ cx(2k-6) \quad (2)$$

$$y(2k+1) = ax(2k+1) + bx(2k-3) + cx(2k -5) \quad ($$

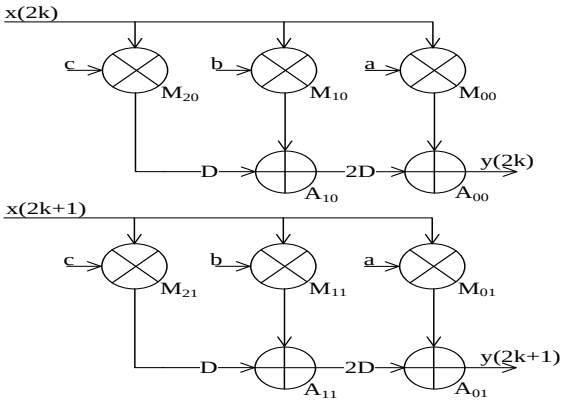

Fig 1: DFG diagram of the 2-unfolded 3-tap FIR filter

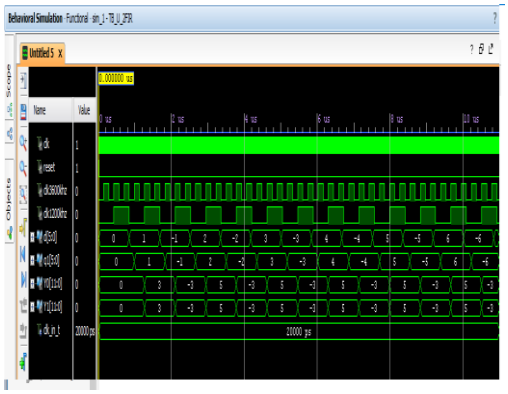

Fig 2: Simulated output waveform of the 2-unfolded 3-tap FIR filter

B. Design and implementation of IIR filter

We consider a simple IIR filter here it has only one pole.

$$y(n) = x(n) + ay(n-1) \quad (4)$$

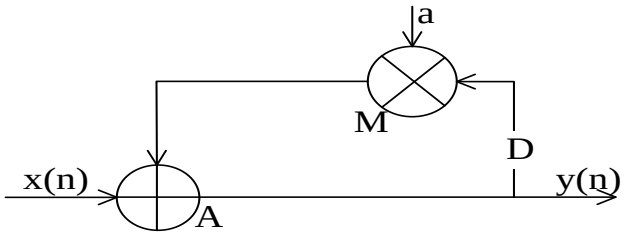

Fig 3: DFG diagram of IIR filter

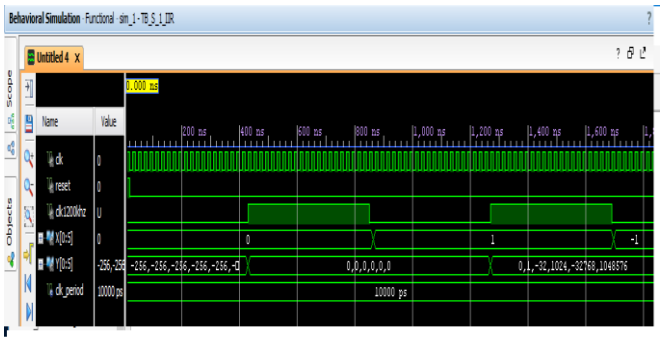

Fig 4: Simulated output waveform of IIR filter

C. Design and implementation of 2-unfolded IIR filter

Mathematical equations for 2 unfolded IIR filter is obtained by substituting '2k and 2k+1' in the place of 'n' in the original IIR filter Eq. 4.

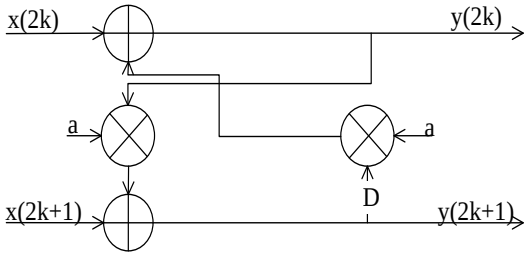

Fig 5: DFG diagram of 2-unfolded IIR filter

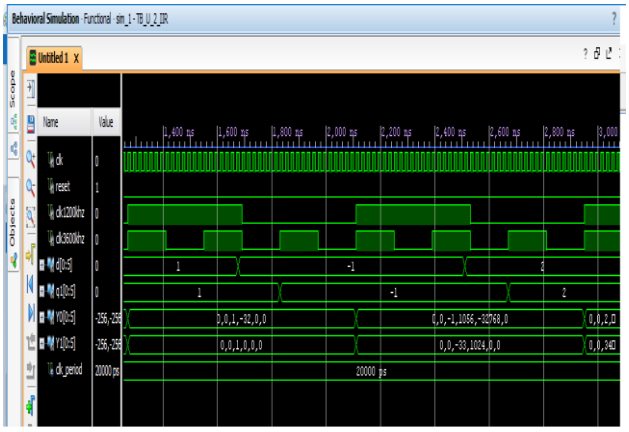

Fig 6: Simulated output waveform of 2-unfolded IIR filter

D. *Design and implementation of 3 unfolded IIR filter*

To implement 3-unfolded IIR filter we need 3 mathematical equations that are obtained from the simple IIR filter equation.

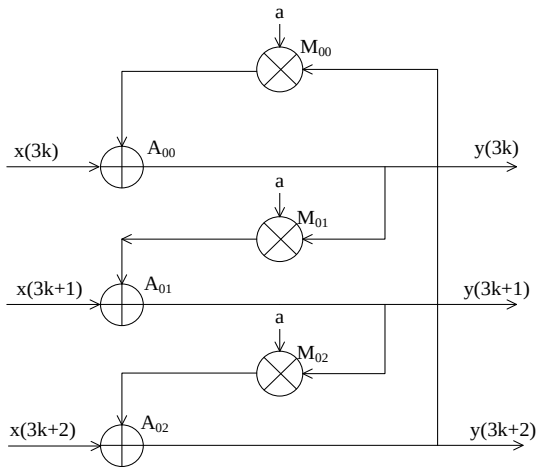

Fig 7: DFG diagram of 3-unfolded IIR filter

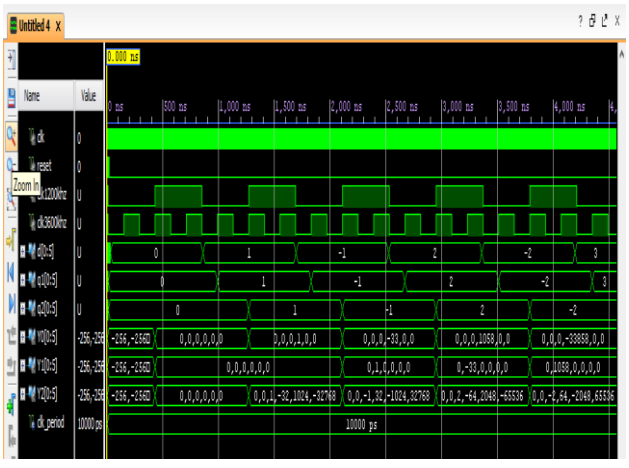

Fig 8: Simulated output waveform of 3-unfolded IIR filter

III. PARLLEL PROCESSING

Parallel processing is a process in which the same hardware is repeated to make the system faster.

A. Design and implementation of 3-parallel IIR filter

3-parallel IIR filters equations can be derived from Eq. 4. For 3-parallel FIR filter we need 3 parallel inputs x(3k), x(3k + 1) and x(3k + 2). When these inputs pass through the implemented filter, gives 3 outputs simultaneously.

$$y(3k) = ay(3k-1) + x(3k) \quad (5)$$

$$y(3k+1) = ay(3k) + x(3k+1) \quad (6)$$

$$y(3k+2) = ay(3k+1) + x(3k+2) \quad (7)$$

In Eq. 7, we put value of Eq. 6 then we will get Eq. 8.

$$y(3k+2) = a^2y(3k) + ax(3k+1) + x(3k+2) \quad (8)$$

$$y(3k+3) = ay(3k+2) + x(3k+3) \quad (9)$$

$$y(3k+3) = a^3y(3k) + a^2y(3k+1) + ax(3k+2) + x(3k+3) \quad (10)$$

$$y(3k+4) = a^4y(3k) + a^3x(3k+1) + a^2x(3k+2) + ax(3k+3) + x(3k+4) \quad (11)$$

$$y(3k+5) = a^5y(3k) + a^4x(3k+1) + a^3x(3k+2) + a^2x(3k+3) + ax(3k+4) + x(3k+5) \quad (12)$$

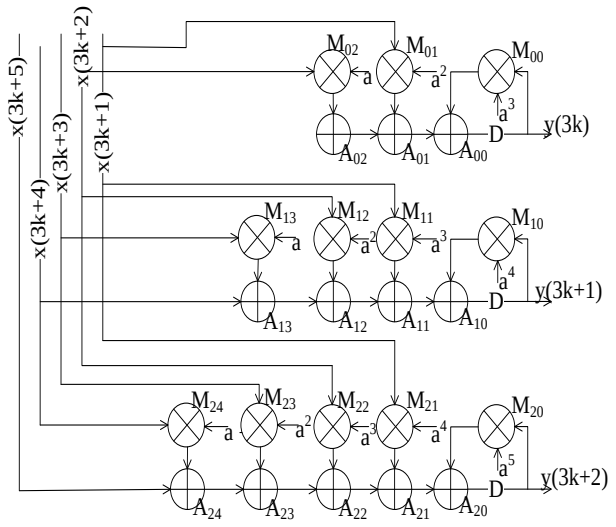

Fig 9: DFG diagram of 3-parallel IIR filter

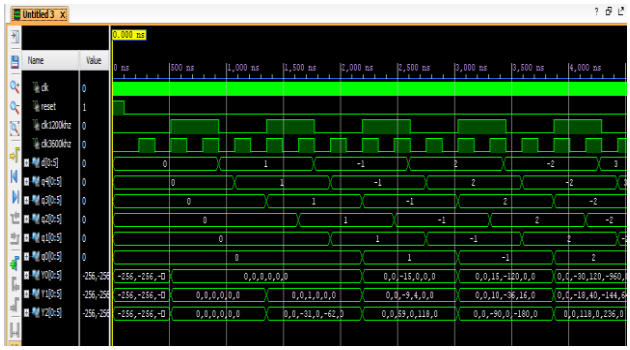

Fig 10: Simulated output waveform of 3-parallel IIR filter

IV. PERFORMANCE COMPARSION AMONG PARALLEL FIR FILTER AND UNFOLDED FIR FILTER

Table1 shows synthesis results comparison among parallel FIR filter and unfolded FIR filter.

Table 1: Synthesis results comparison among parallel FIR filter and unfolded FIR filter

Structure	Delay (ns)	Area (LUT)	Dynamic Power (W)
2-unfolded 3-tap FIR filter	5.298	54	22.857
2-parallel 3-tap FIR filter	5.020	52	24.359
3-unfolded 3-tap FIR filter	4.834	77	34.3978
3-parallel 3-tap FIR filter	5.013	75	34.928

Table 2 shows synthesis results comparison among parallel IIR filter and unfolded IIR filter.

Structure	Delay (ns)	Area (LUT)	Dynamic Power (W)
2-unfolded IIR filter	3.654	13	10.242
2-parallel IIR filter	5.64	35	35.133
3-unfolded IIR filter	3.377	18	15.993
3-parallel IIR filter	5.468	61	51.042

A. *Performance Comparison among existing FIR filter and implemented FIR filters*

Table 3 shows a comparison between existing FIR filters and implemented FIR filters.

Existing FIR filters		
Structure / Device	**Filter**	**Delay (ns)**
16 bit Vedic multiplier[6]	4-tap programmed sequential FIR filter	10.56
16 bit Wallace tree multiplier[6]	4-tap micro programmed sequential FIR filter	15.56
Virtex-4 (xc4vfx12)[7]	Serial FIR filter	24.648
Virtex-5 (xc5vl110t)[7]	Serial FIR filter	18.69

Virtex-6 (xc6vcx75t)[7]	Serial FIR filter	17.411

Implemented FIR filters		
Structure / Device	**Filter**	**Delay (ns)**
xc7a200tfbg676	3-tap FIR filter	6.970
xc7a200tfbg676	2-unfolded 3-tap FIR filter	5.298
xc7a200tfbg676	2-parallel 3-tap FIR filter	5.020
xc7a200tfbg676	3-unfolded 3-tap FIR filter	4.834
xc7a200tfbg676	3-parallel 3-tap FIR filter	5.013

V. CONCLUSION

In this paper, we designed and implemented unfolded architecture and parallel processing architecture for FIR and IIR filters. Synthesis and simulation are being carried out on Artix-7 series FPGA, target device (xc7a200tfbg676) (speed grade -1) using VIVADO 2016.3. Critical path delay of the simple 3-tap FIR filter is 6.970 ns, critical path delay for 2-unfolded 3-tap FIR filter is 5.298 ns, and critical path delay for 3-unfolded 3-tap FIR filter is 4.834 ns. So it is clear that as the unfolding factor (J) increases critical path delay become less means FIR filter become faster. Area utilized in terms LUT of simple IIR filter is 6. LUT consumed by 2-unfolded and 3-unfolded IIR filter is 13 and 18 respectively. Experimental results show that for IIR filter case as an unfolding factor (J), increases dynamic power consumption is increased and speed is improved also it has been shown that 3-unfolded IIR filter consumes less power and it is faster than 3-parallel IIR filter.

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