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# A Robust and Efficient Fault-Resilient Rad Hard ADPLL

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***Abstract*: Typically, classical PLLs adopt analog design methods. However integrating PLL with noise-prone application environment is highly tedious and somewhere confined. As per current knowledge majority of PLLs apply Analog Loop Filters (ALFs) and Voltage Controlled Oscillators which are practically highly complicated to integrate with noisy environment. Even the traditional PLLs can't be ported to the advanced processors. In last few years, the emergence of deep-submicron CMOS technologies have enabled digitization of major traditional analog circuits, comprising the analog PLLs that as a result could be vital to overcome above mentioned issues and to achieve more efficient solution than classical analog implementation.***

***Keywords* : ADPLL, Radhard, FDLC-ADPLL**

## I. INTRODUCTION

Literature Survey [1-10] reveals that ADPLL outperforms classical PLLs and have more significance towards communication systems as well as consumer applications. However, exploring in depth it can be found that there are numerous real-time application environments such as space radiation conditions where ADPLL undergoes adversaries due to emergence of relatively small square impulse in the main signal. Removal of such insignificant noise impulse is inevitable to avoid logical faults and resulting hazardous consequences. Eliminating the presence of jitter and other noise components while maintaining minimum lock period, can make ADPLL more suitable in real time applications for frequency synthesis, clock recovery, clock de-skewing, . With this motivation, in this research work a robust and highly radiation fault tolerant ADPLL design is proposed for frequency synthesis. Our proposed design incorporates a novel dual-mode operation, Frequency-Acquisition Mode (FAM) and Phase-Acquisition-Mode (PAM). In FAM process, we have applied a feed-forward compensation model that takes two distinct reference cycles for calculating ADPLL parameters (predict variable and desired variable). Once estimating the predict variable, it is fed as input to a Digitally Controlled Oscillator (DCO). It is then followed by the execution of PAM that activates PLL to minimize residual frequency error.

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## II. TYPES OF ADPLL BASED FREQUENCY SYNTHESISER

Typically, ADPLL is designed in two approaches; Feedback-Divider (FD) based ADPLL design [11-12] and Feedback-Divider-Less Counter (FDLC) enabled ADPLL design [13-14]. In fact, FDLC based ADPLL was developed before FD-ADPLL, but was not widely used, because FD-ADPLL closely represented Charge pump PLL architecture and was widely accepted by the PLL community. However off late FDLC-ADPLL is found significant in most of the commercial applications because of its lower power consumption, area and better performance[15-17].

In both ADPLL architectures discussed above VCO is replaced with a DCO for generating expected output frequency clock ($F_{out}$). Similarly, a Phase/Frequency Detector (PFD) and Charge Pump are replaced by a Time-to-Digital Converter (TDC) to detect phase difference of the varying output frequency vs. the frequency input reference ($F_{in}$) clock. In ADPLL design the passive loop RC filter is replaced by a Digital Loop Filter (DLF). The DLF generates the tuning bits for the DCO to keep the ADPLL in frequency and phase lock. Exploring in depth it can be visualized that the prime differentiating factor that distinguishes the two types of ADPLL is the way that the $F_{out}$ is fed into TDC for phase/frequency detection.
The Feedback Divider based ADPLL is as shown in Figure 1.

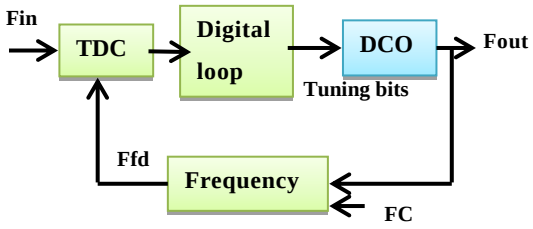


**Fig 1 Block Diagram of Feedback Divider Based ADPLL**

As depicted in Figure 1, the $F_{out}$ is frequency divided such that its average frequency is equivalent to the reference frequency $F_{in}$ clock, hence forcing the range of TDC to be augmented significantly. Furthermore, it is found that the phase error at TDC might impose or increase significantly high amount of phase-frequency noise which is required to be minimized or eliminated by means of certain loop filter. This as a result imposes additional burden of loop filtering to reduce noise components. The range of TDC is as given in Equation 1.

$$T_{Ref} = 1/F_{in} \quad \text{Equation 1}$$

The above mentioned complexities could is alleviated in FDLC-ADPLL by means of more efficient hardware design. The FDLC ADPLL is as shown in Figure 2.

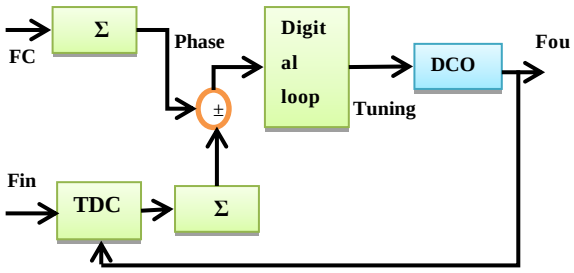


**Fig 2Block Diagram of Feedback Divider Less Counter based ADPLL**

Since, in this research we intend to develop a low jitter radiation hard fault resilient ADPLL design, we have preferred FDLC-ADPLL that not only reduces computational complexity but also achieves swift locking time to perform frequency synthesis. [15, 18-20]. Figure 2 presents the FDLC-ADPLL concept of phase-domain function. Interestingly, our proposed FDLC-ADPLL model avoids aforesaid problems in the classical FD-ADPLL design. In our proposed model, the classical TDC model is redefined and stated as Timestamp-to-Digital Converter (TDC) that comprises integer component of the variable phase. In this model, both $F_{out}$ as well as $F_{in}$are connected directly to the TDC and since no dithering is applied the TDC covers relatively narrow range of $F_{out}$ phase which is significantly lower than the $F_{in}$ phase, which can be increased significantly at the system level by means of a $F_{out}$ edge counter [21]. Noticeably, the output is a definite number comprising the integer count of the $F_{out}$ cycles and the normalized difference between $F_{in}$ and $F_{out}$edges. At the basic level, FDLC-ADPLL functions in the true-phase model [22,23], where it compares the variable phase of the multiple-Gigahertz (GHz) DCO with lower reference frequency, like20MHz. Since, in this research the emphasis is made on the frequency synthesis of 2.4 GHz by applying reference frequency of 20 MHz, FDLC-ADPLL becomes a potential solution to meet the requirement. In this model, the comparison output signifies the digital phase error which is then processed with digital loop filter so as to adjust DCO frequency in the negative feedback approach. Literatures [24-25] reveal that the FDLC-ADPLL model outperforms classical FD-ADPLL model in terms of computational time, power consumption and cost. It makes it suitable to be used in major higher-end applications such as mobile phone and consumer electronics and is being used in almost 33% of the mobile manufacturing globally. A schematic of the FDLC-ADPLL based phase domain operation is illustrated in Figure 3.

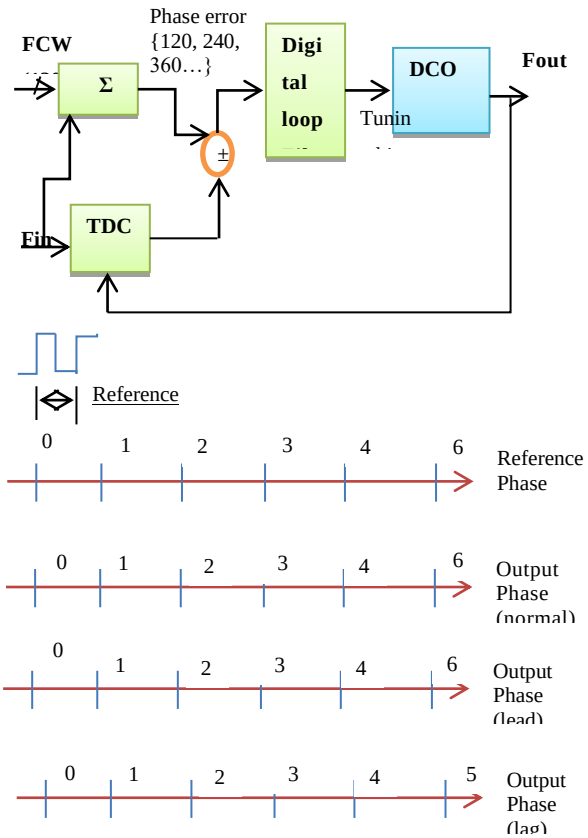


**Fig 3Block Diagram Illustration of a phase-domain FDLC-ADPLL function**

The reference frequency signal information is completely encompassed in the transition period, also called as the timestamps of the $F_{in}$ clock. Amongst the two feasible transition possibilities, in our proposed model only the edges of the rising clock are taken into consideration. Similarly, the time-information of the $F_{out}$ is also included in its rising edge timestamps. FCW signifies the expected or the targeted frequency multiplicative ratio, is assigned as 120. As, the oscillation period refers the inverse of the oscillating frequency, there can be 120 Fout clock cycles per single cycle of the reference frequency $F_{in}$. Here, it is assumed that the initial phase is zero and therefore the rising edges of $F_{in}$ and $F_{out}$ are aligned at the initial time (i.e., zero time), though it is not inevitable. In fact, the phase domain function takes place on the basis of numerical estimation of the phase error $PE[t]$, which is obtained as the difference in between the reference phase $FRef\phi[t]$ and the variable output phase $Fout\phi[t]$. Noticeably, here the phase estimation is denoted in terms of the Unit Interval (UI), which signifies clock period of the $F_{out}$. In this manner, the reference phase states the required $F_{out}$ cycles originating from the time zero. In practice it is estimated as the cumulative addition of FCW, i.e., $FRef\phi[t] = \sum FCW[t]$. In summary, estimating the difference between the actual and ideal count of $F_{out}$ cycles at each reference edge gives the value of phase error. Mathematically it is expressed as given in Equation 2.

$$PE[t] = FRef\phi[t] - Fout\phi[t] \quad \text{Equation 2}$$

Once retrieving the value of the phase error the DCO frequency is adjusted. In case, the phase error is positive i.e $F_{out}$ $\phi[t]$ lags $F_{in}$ $\phi[t]$, the DCO requires speeding up. Similarly, if the phase error is negative i.e $F_{out}$ $\phi[t]$leads $F_{in}$ $\phi[t]$it signifies that the DCO has to become slower. Considering $F_{ref}$ clock as stable and constant FCW, both conditions alter the DCO frequency. On contrary, if FCW increases, the DCO is supposed to be speed up to scale up to another reference frequency. Thus, applying Radhard fault tolerant design approach in the above discussed FDLC-ADPLL design architecture, in this research work a novel frequency synthesizer is developed and simulated.
The following section discusses the implementation of the proposed fault-tolerant Radhard FDLC-ADPLL design.

## III. RHBD-AL ADPLL BASED FREQUENCY SYNTHESIZER

Taking into consideration the robustness and efficiency, we have considered FDLC-ADPLL architecture for radiation-hard fault tolerant ADPLL based frequency synthesis. Author proposes the RHBD-AL ADPLL architecture as given in Figure. 4.

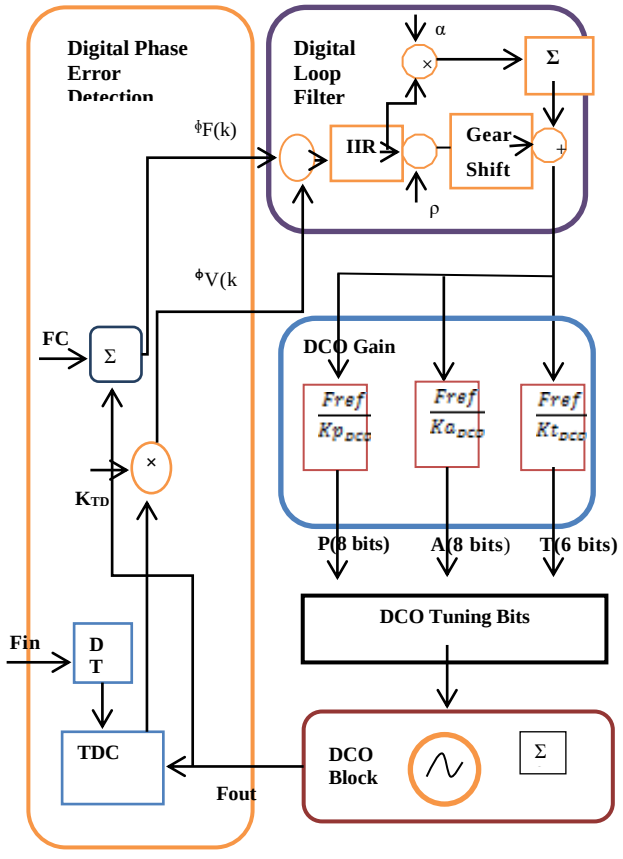


**Fig 1 Proposed Block Diagram of RHBD-AL ADPLL Frequency Synthesizer Architecture**

Unlike traditional phase prediction approaches, in our proposed ADPLL design, an enhanced phase prediction technique is applied [26]. As depicted in Figure. 4, the DCO component exhibits not merely a single but three distinct inputs (say, Tuning Word Inputs (TWI)) so as to control the Process, Voltage, Temperature centring (PVT); acquisition and tracking, distinctly. In this model, the PVT bank "p" re-centres the natural frequency of DCO to the mid of the chosen frequency band. Similarly, the acquisition bank signified as "a" exhibits channel selection by means of swift settling towards the expected frequency. The third bank (i.e., "t") refers the tracking bank which is the one actually used during communication. One of the key strengths of this ADPLL design is that it transverses the p/a/t banks swiftly with increasingly finer frequency steps while exhibiting reduction of the loop bandwidth iteratively.

Implementing this approach, the overall settling period can be made very fast irrespective of the initial frequency difference. Now, to enable efficient ADPLL control, particularly its filtering ability, 4th order IIR filter is applied which is then followed by the use of a PI controller that embodies gain parameters, $\alpha$ and $\rho$, respectively. $\alpha$ and $\rho$ are derived using Equations 3 and 4 respectively.

$$f_{CPLL} = \frac{F_{ref}}{2\pi} \times \alpha \quad \text{Equation 3}$$

$$\xi = \frac{1}{2}\frac{\alpha}{\sqrt{\rho}} \quad \text{Equation 4}$$

Where, $f_{CPLL}$ presents, the 3-dB cut-off of the ADPLL closed loop. In practice, the eventual value of $\alpha$ is selected as to provide low jitter in the DCO output. To alleviate the issue of flickering noise and radiation caused impulse noises, in our proposed model the proportional integral loop factor $\alpha = 0.6283$ **and** $\rho = 0.0986$ has been activated once the loop gets settled. In addition to it, in proposed digital phase error detector, at first we accumulate FCW so as to form a fixed digital reference phase $\phi F[t]$. After estimating $\phi F[t]$ it is compared with the DCO variable phase $\phi V[t]$ that as a result provides the value of digital phase error. In our model, we have implemented the integer phase error detection model distinctly by means of a phase prediction model that ultimately enhances the overall performance and power efficiency.
The detailed discussion of the proposed ADPLL system is given in the following sub-sections.

### A. *RHBD Digital Phase Error Detection*

This circuit primarily functions to generate digital phase error by exploiting phase information of $F_{ref}$, DCO clock $F_{out}$and FCW. This circuit encompasses two distinct functions, the integer fixed part (on the basis of $F_{out}$ cycle counter) and the integer variable part (on the basis of TDC) functions. One of the key novelties of the proposed design is the inclusion of the generation of the re-timed reference clock for digital operation for phase error detection. It makes overall phase error detection simple and more efficient with radiation hard frequency synthesis applications. Considering the need of a radiation hard, fault tolerant frequency synthesis requirement, to achieve the targeted closed-loop phase noise performance, typically the time resolution of the TDC is maintained in the range of 10– 20 $ps$ [27-28].

To cover a single unit $F_{out}$ time-period with a consistent time resolution, we have designed TDC that functions by performing sampling of $F_{out}$ outputs at each rising edge of the reference frequency$F_{in}$. In this mechanism, the sampled digital state encompasses primarily the knowledge about the $F_{out}$-$F_{in}$ timing difference. In practice, such TDC might require sufficient number of flip-flops and delay cells to obtain expected timing resolution. To deal with such issue, we have incorporated a novel phase prediction scheme. An illustrative presentation of the derived phase prediction model to be used in ADPLL is given in Figure. 5.

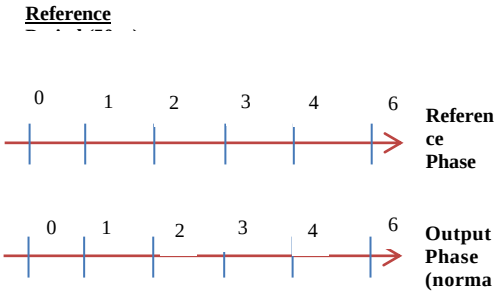


**Fig 2 FCW Based Phase Prediction Model**

The above lines signify the timestamps of the $F_{out}$ and the reference frequency $F_{in}$ rising edges, correspondingly. Noticeably, in this illustration $FCW$ is taken as $120$. In this method, the timing difference (or separation) between edges of $F_{out}$ and the $F_{in}$ edge exhibits a periodical pattern of $0$,120,240, etc, where the repetition interval is assigned as 120.In the proposed phase prediction model, the edges of reference frequency get delayed in such manner that it is often aligned with the consecutive edge of the $F_{out}$ edge. Thus, it enables TDC to cover relatively very small range merely to deal with the phase noise or jitter and errors in the delay control. In our proposed model, $F_{in}$ is fed through a DTC unit for generating a delayed form of the reference clock. In this approach certain finer resolution of TDC can also be used to reduce quantization error of the dynamic phase error $(PE_F[t])$. To achieve the total phase error, the estimated value of $\phi V[t]$ is added/subtracted with integer phase error $\phi F[t]$ which signifies the integer component of the phase error $PE[t]$. In this case, the total time resolution becomes equal to the resolution of the narrow TDC. Since this approach reduces the need of TDC operating range and therefore multiple high-resolution TDC circuits can be applied without exhausting additional power. It should be noted that, $\phi V[t]$equals zero at least for those period when the loop remains in the locked period (say, locked condition) and in this case its allied circuit elements (i.e., the circuit elements of the integer part) could be turned OFF to preserve power consumption. The other advantage of the proposed phase prediction technique is that it enables TDC to operate only on the edges needed for time quantization that significantly reduces power consumption. This enables our proposed model to be well suited for major real-time application environment, especially space radiation environment. Undeniably, to achieve fault tolerant radiation-hard ADPLL design enhancing TDC is of paramount significance.

### B. *RHBD Digital Loop Filter*

In our model the TDC unit function doesn't cause any reference spurs that eventually enables digital loop filter to be calibrated at the best performance point in between the noise components (i.e., reference phase noise and oscillator phase noise). It strengthens our proposed model to exhibit better filtering even at 1st or 2nd order. On contrary, PLLs require minimum 3rd order filtering to give equivalent result. On contrary, in radiation-hard environment it might require even more sharp filtering approach which might seem impractical with traditional PLLs. In our proposed ADPLL design, a digital loop filter encompassing phase error combiner unit, cascaded 4th order IIR filters with distinct filtering coefficient $(\varphi_1 - \varphi_4)$ is applied. In addition, it contains path loops gain coefficients, $\alpha$ (proportional path) and $\rho$ (integral path).

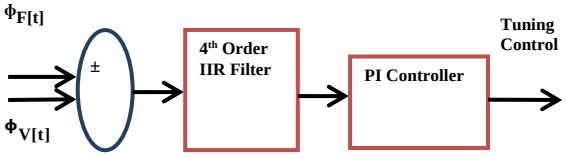


**Fig 3 Block Diagram of RHBD-AL Digital Loop Filter**

As depicted in Figure 6, our proposed phase error combiner model combines both $\phi F[t]$as well as $\phi V[t]$ components to estimate a complete error Phase error [PE]. Though, it can be accomplished by means of applying a binary adder, we find that the it can be applied as a multiplexer so as to select $\phi F[t]$ during loop acquisition and $\phi V[t]$once loop is in locked condition. The IIR filter under consideration follows the expression, as given in Equation 5 .

$$q_i[t] = (1-\varphi_i) \cdot q_i[\varphi - 1] + \varphi_i \cdot p_i[t]$$

**Equation 5**

where the variables $p_i[t]$ and $q_i[t]$ represents the inputs and outputs, correspondingly. Here, $i$ represents each stage while $\varphi_i$ presents respective coefficient value. Here, IIR filter processes the PI controller that intends to improve the narrow radiation spike rejection in the filtering characteristics of our proposed Radhard ADPLL design.

### C. *RHBD Digitally Controlled Oscillator*

Undeniably, DCO is considered as the heart of the ADPLL, which functions on the basis of an LC-tank having (-) resistance so as to enable oscillations, in the similar way as performed by VCO given in Figure. 7.

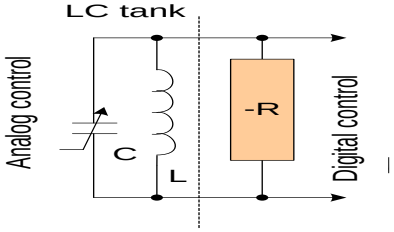


**Fig4Typical Voltage Controlled Oscillator**

Unlike traditional variable capacitor based VCO, DCO uses a number of binary controlled varactors as shown in Figure. 4.8,which could be set in either low or high capacitive state. As the input of DCO are usually controlled digitally, and as the varactors (i.e., DCO input) are digitally controlled and the output clock at multi-GHz frequencies is extensively applied shape of the digital waveform in DCO, which corrects its phase and frequency, can be called as fully digital [29-30].

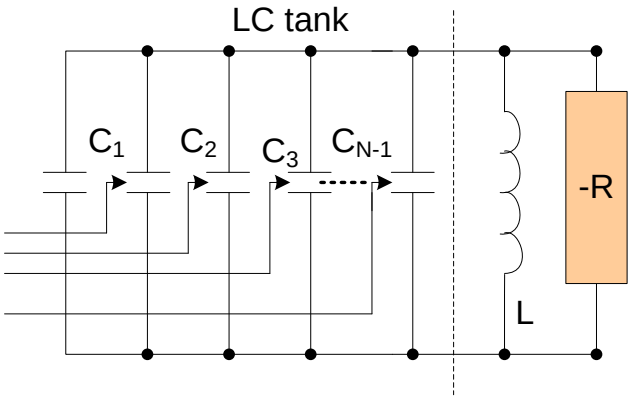


**Fig 5 Digital Controlled Oscillator**

It should be noted that the negative resistance signifies perpetuations of the resonance of the lossy LC tank. The smallest size of the varactor step is in the order of 156fF. It corresponds to the frequency step size of 32 kHz at 2.4 GHz DCO output. In our designed model, the tuning control is divided in multiple banks with different or varying frequency step size. In our DCO architecture, the oscillator phase noise has been controlled by means of the current dissipated, which has been arranged with the help of a 22-bit "bias" control. An illustration of the DCO oscillator core is as shown in Figure. 9.

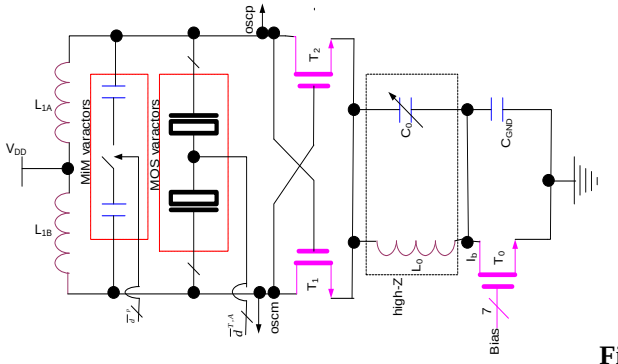


**Fig 6Digital Oscillator Core**

The DCO modes along with its centre frequency, frequency step and capacitor is given in Table 1. Inductor value is taken as 1H.

**Table 1 Digital Controlled Oscillator Modes of Operation**

| Mode | Frequency Range | Centre Frequency | $F_{min}$ | $F_{max}$ | Frequency Step | $C_{max\ (pF)}$ | $C_{min}$ (pF) | δC (pF) |
|---|---|---|---|---|---|---|---|---|
| PVT (8 bits) | 500MHz | 2.4GHz | 2.15GHz | 2.65GHz | 1.95MHz | 5.4 | 3.6 | 7.3 |
| ACQ (8 bits) | 100MHz | 2.4GHz | 2.35GHz | 2.45GHz | 390KHz | 4.56 | 4.21 | 1.36 |
| TRK (6 bits) | 2MHz | 2.4GHz | 2.399GHz | 2.401GHz | 31.25KHz | 4.40 | 4.39 | 0.15 |

The DCO gain normalization is the frequency range ($F_{max}$ .$F_{max}$) divided by the number of bits allocated to each bank. This DCO gain normalization is applied on the IIR Filter output, to obtain the new tuning word. Ideally, the gain normalization factor is unity. However by modifying this dynamically, the phase noise and jitter can be reduced .Fmin, Fmax and Capacitance values are measured using the following equations Equation 6-10

$$Fmin = \frac{fc - Range\ (PVT/ACQ/TRK)}{2}$$

**Equation 6**

$$Fmax = \frac{fc + Range\ (PVT/ACQ/TRK)}{2}$$

**Equation 7**

$$Cmax = \frac{1}{(2\pi fmin)^2}$$

**Equation 8**

$$Cmin = \frac{1}{(2\pi fmax)^2}$$

**Equation 9**

$$\delta C = \frac{Cmax - Cmin}{(2)^{b\ mode}}$$

**Equation 10**

This novel Radhard FDLC-ADPLL architecture explained above is modelled and simulated in MATLAB/SIMULINK. The Simulink model is as shown in Figure 10.

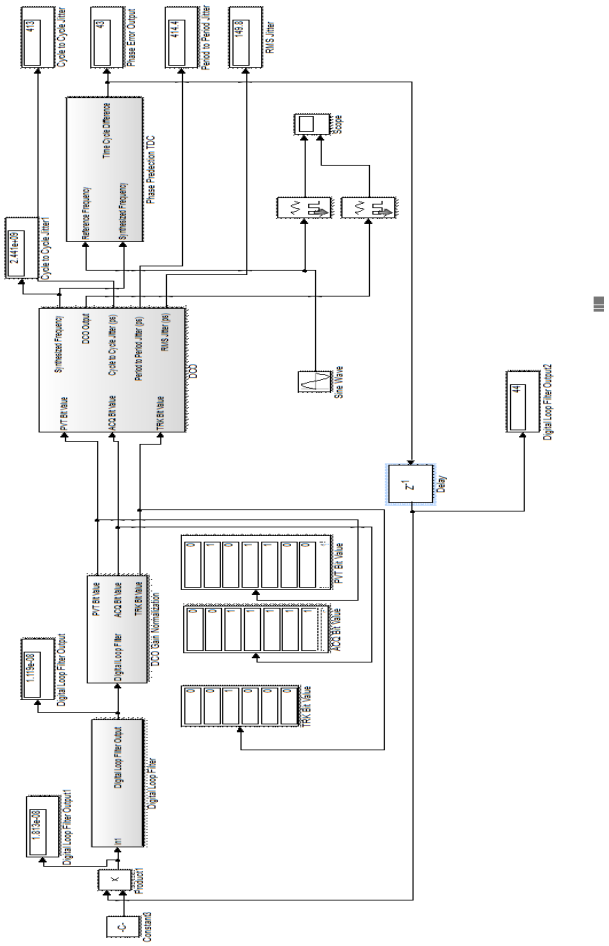

**Fig 7 Simulink Model of RHBD-ALFDLC ADPLL**

The centre frequency of this ADPLL is 2.4GHz and it locks frequencies from 2.15GHz to 2.65GHz. DCO operation switches from PVT mode to ACK mode and to TRK mode. PVT mode provides coarse tuning, ACK mode provides medium tuning and the TRK mode provides fine tuning. The jitter prediction block predicts the cycle, period and rms jitter. The results of this Simulink model are captured in the next section.

## IV. RESULTS OF RHBD-AL ADPLL

A robust radiation hardened ADPLL design was developed for space communication applications. The FDLC ADPLL model was developed for frequency synthesis purpose where the reference input frequency was fixed at 20 MHz, while the synthesis frequency was 2.4GHz.

A snippet of the test simulation and results obtained is given as follows in Table 2.

**Table 1 Simulation Results of RHBD-AL ADPLL**

| Sl No. | Parameter | Standard Specifications | Simulated Results of RHBD-AL ADPLL |
|---|---|---|---|
| 1. | Input Frequency | 20MHz+/- 5MHz | 20MHz input |
| 2. | Output Synthesized Frequency | 2.2GHz-2.5GHz | 2.4GHz |
| 3. | TDC resolution | 420ps | 416ps |
| 4. | Loop Filter Type and Order | 3rd Order | 4th Order ,IIR Filter |
| 5. | Settling Time | <10us | 0.6us |
| 6. | Cycle to cycle jitter | 120-300ps | 312ps |
| 7. | Period Jitter | 120-300ps | 256ps |
| 8. | Rms jitter | 120-300ps | 82ps |
| 9. | Phase Noise (calculated from rms jitter) | -110dbc/Hz | -115.75dbc/Hz |
| 10. | SET Impulse Noise | 1ns, 1mA input | 1ns, 1mA input |
| 11. | Settling time with noise | <10us | 1.2us |
| 12. | Rms jitter in presence of impulse noise | 120-300ps | 340ps |
| 13. | Phase Noise in presence of impulse noise(calculated from rms jitter) | -110dbc/Hz | -103.39dbc/Hz |

The RHBD-AL ADPLL in presence of SET pulse has obtained less settling time of 1.2us. The rms jitter and phase noise of RHBD-AL ADPLL is 340ps and -103.39dbc/Hz respectively.

The reference frequency and the phase error outputs of RHBD-AL ADPLL are illustrated in Figure. 11 and Figure. 12 respectively. Results reveal that the total phase error reduces and reaches to zero that makes instantaneous DCO frequency to reach targeted 2.4 GHz.

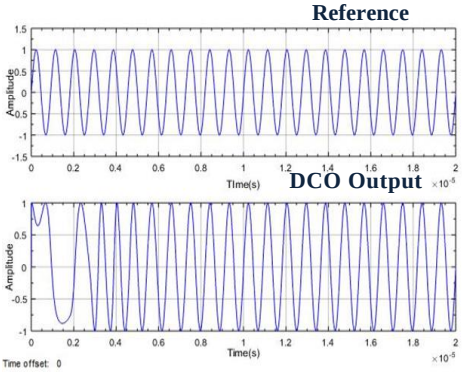


**Fig 1 Plot of Reference frequency Vs DCO output**

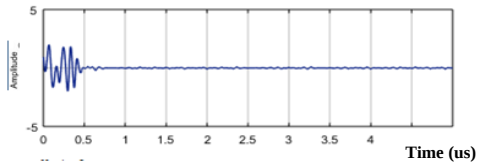


**Fig 2 Plot of Phase-error between $F_{ref}$ and $F_{out}$**

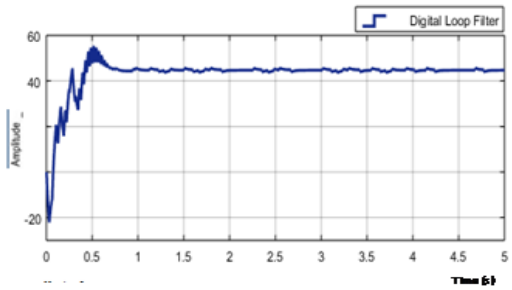


**Fig 3 Plot of Digital Loop Filter Output Settling Time**

Observing the results Figure 13, it can be easily observed that the proposed ADPLL design reduces the error soon before 0.6 us

When the RHBD-AL ADPLL is simulated in presence of SET impulse noise of 1ns and 1mA added at the reference the settling time of 1.2us obtained is shown in Figure 14.

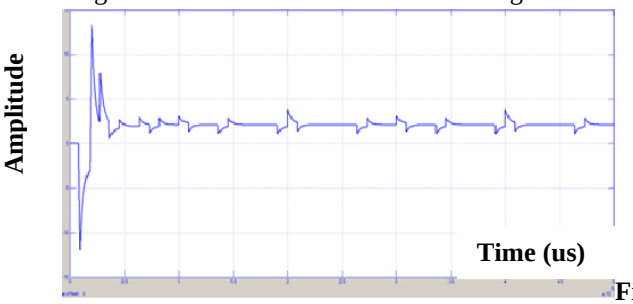


**Fig 4 Plot of Digital Loop Filter Output Settling Timein Presence of SET Impulse**

Thus, the results obtained from Table 4.2 have validated that the radhard RHBD-AL ADPLL architecture can be a potential fault tolerant solution to be used in high frequency, radiation hard by design "digital frequency-synthesis" applications where it has resulted in low jitter of 340ps, phase noise of -103.39dbc/Hz and less locking period of 1.2us in the presence of 1ns, 1mA radiation simulated impulse noise, as referring to the standard specified values.

The tuning control word obtained for different sample values of difference between $F_{ref}$ and $F_{out}$ is tabulated in Table 3.

**Table 2 Tuning Word Inputs to DCO**

| Sample Value | PVT Value | ACQ Value | TRK Value | PVT Digital Value(8 bit) | ACQ Digital Value (8bit) | TRK Digital Value (6 bit) |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0000 0000 | 0000 0000 | 000 000 |
| 10 | 2.014e-8 | 1.295e-7 | 1.403e-6 | 0001 0100 | 1000 0001 | 111 011 |
| 20 | 4.029e-8 | 2.59e-7 | 2.805e-6 | 0010 1000 | 0000 0011 | 110 101 |
| 30 | 6.043e-8 | 3.885e-7 | 4.208e-6 | 0011 1100 | 1000 0100 | 110 000 |
| 40 | 8.057e-8 | 5.18e-7 | 5.611e-6 | 0101 0001 | 0000 0110 | 101 011 |
| 50 | 1.007e-7 | 6.475e-7 | 7.014e-6 | 0110 0101 | 1000 0111 | 100 110 |
| 60 | 1.209e-7 | 7.769e-7 | 8.416e-6 | 0111 1001 | 0000 1001 | 100 000 |
| 70 | 1.41e-7 | 9.064e-7 | 9.819e-6 | 1000 1101 | 1000 1010 | 011 011 |
| 80 | 1.611e-7 | 1.036e-6 | 1.122e-5 | 1010 0001 | 0000 1100 | 010 110 |
| 90 | 1.813e-7 | 1.165e-6 | 1.262e-5 | 1011 0101 | 1000 0001 | 010 001 |
| 100 | 2.014e-7 | 1.95e-6 | 1.403e-5 | 1100 1001 | 0000 1111 | 001 011 |
| 110 | 2.216e-7 | 1.424e-6 | 1.543e-5 | 1101 1110 | 1001 0000 | 000 110 |
| 120 | 2.417e-7 | 1.554e-6 | 1.683e-5 | 1111 0010 | 0001 0010 | 000 001 |
| -120 | -2.417e-7 | -1.554e-6 | -1.683e-5 | 0000 1110 | 1110 1110 | 111 111 |
| -110 | 2.216e-7 | -1.424e-6 | -1.543e-5 | 0010 0010 | 0111 0000 | 111 010 |
| -100 | 2.014e-7 | -1.295e-6 | -1.403e-5 | 0011 0111 | 1111 0001 | 110 101 |
| -90 | -1.813e-7 | -1.165e-6 | -1.262e-5 | 0100 1011 | 0111 0011 | 101 111 |
| -80 | -1.611e-7 | -1.036e-6 | 1.122e-5 | 0101 1111 | 1111 0100 | 101 010 |
| -70 | -1.41e-7 | -9.064e-7 | -9.819e-6 | 0111 0011 | 0111 0110 | 100 101 |
| -60 | -1.209e-7 | -7.769e-7 | -8.416e-6 | 1000 0111 | 1111 0111 | 100 000 |
| -50 | -1.007e-7 | -6.475e-7 | -7.014e-6 | 1001 1011 | 0111 1001 | 011 010 |
| -40 | -8.057e-8 | -5.18e-7 | -5.611e-6 | 1010 1111 | 1111 1010 | 010 101 |
| -30 | -6.043e-8 | -3.885e-7 | -4.208e-6 | 1100 0100 | 0111 1100 | 010 000 |
| -20 | -4.029e-8 | -2.59e-7 | -2.805e-6 | 1101 1000 | 1111 1101 | 001 011 |
| -10 | -2.014e-8 | -1.295 | -1.403e-6 | 1110 1100 | 0111 1111 | 000 101 |

| | | | | | | |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0000 0000 | 0000 0000 | 000 000 |

## V. CONCLUSION

ADPLL outperforms classical PLLs and have more significance towards communication systems as well as consumer applications. The proposed ADPLL model uses a FDLC based architecture. This architecture model outperforms classical FD-ADPLL model in terms of computational time, power consumption and cost. The centre frequency of this ADPLL is 2.4GHz and it locks frequencies from 2.15GHz to 2.65GHz. DCO operation switches from PVT mode to ACK mode and to TRK mode. PVT mode provides coarse tuning, ACK mode provides medium tuning and the TRK mode provides fine tuning. The results obtained have validated that the radhard RHBD-AL ADPLL architecture can be a potential fault tolerant solution to be used in high frequency, radiation hard by design "digital frequency-synthesis" applications where it has resulted in low jitter of 340ps, phase noise of -103.39dbc/Hz and less locking period of 1.2us in the presence of 1ns, 1mA radiation simulated impulse noise, as referring to the standard specified values.

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