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Design and Performance Analysis of Hybrid Full Adder using Fin FET 40nm Technology

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Abstract: Designing a low power and energy efficient circuits in FinFET technology is of great Challenge. This paper presents the internal logic structure and circuit operation using the devices, CMOS and FinFETs for designing the hybrid adder cells. At transistor level, CMOS and FinFET based hybrid full adder (HFA) and improved hybrid full adder (IHFA) is designed. Simulations are carried out using the cadence tool in UMC 40nm and the performance analysis of these HFA and IHFA are compared with the 40nm FinFET technology. It is observed that IHFA is better when compared with the HFA in terms of propagation delay, power consumption and energy delay product. IHFA achieves the higher drive current and low leakage power for better mobility and transistor scaling as compared with HFA.

Index Terms: low-power, energy efficient, FinFET, Internal logic structure, hybrid adder, ultralow voltage.

I. INTRODUCTION

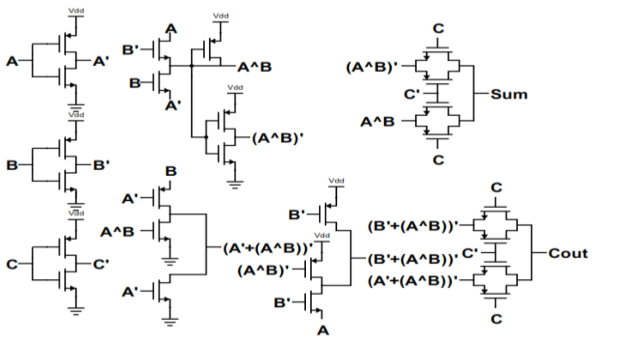
The development of mobile operating applications, for example, PDAs, PCs and the advancement of the contraction of the technology needs littler silicon area, high throughput hardware and low power consumption [1-3]. The multi-gate transistors such as double gate FinFETs achieves low sub-threshold Swing (SS) and low leakage current as compared with the Standard CMOS [4]. Adders play an important role in the complex arithmetic circuits to perform addition, subtraction, multiplication and division, act as the core elements and can significantly influence the performance of any system implemented in DSP based processors to accomplish applications such as video processing, filtering and Fast Fourier Transform, in terms of low power and energy efficiency[5-6]. By scaling the supply voltage and operating frequency, power consumption is reduced. But due to this delay and driving capability increases [7-9]. Number of Full Adders are designed in earlier, each one of it have its own merits and demerits. Full adder makes a center of attraction in carry select, carry skip, carry look ahead and conventional adders using efficient structures[10-11].Furthermore designing and enhancing the Full adder with better performance is necessary at ultra-low voltages. This paper organizes of

(1) Designing of 1-bit Full adder using Nano scale transistors such as FinFETs over standard CMOS for energy efficiency.
(2) Performance analysis of LVT FinFET and CMOS based 1-bit Hybrid full adder.

Rest of the paper is as follows. Section 2 gives the design and operation of proposed HFA (hybrid full adder) and IHFA (improved hybrid full adder) based on internal logic structure. Section 3 presents the performance analysis of CMOS and FinFET based HFA and IHFA by supply voltage scaling. Transient analysis of the CMOS and FinFET based HFA and IHFA at V_{dd} =0.2 V is shown and explained in Section 4. Section 5 presents the comparison table and the output swing table and their analysis. Finally conclusion is given in section 6.

II. DESIGN AND OPERATION OF PROPOSED HFA AND IHFA CELLS

Figure 1(a, b) shows the schematic diagrams of FinFET based HFA and IHFA. Swing restored pass transistor is logic structure is used for designing the HFA. This HFA consists of 25 transistors and uses 3 inverters, XOR/XNOR, modified NAND/NOR gates .The outputs Sum and Cout are selected based on intermediate signal C. when C=0 the Sum output is A^B and Cout is (A^B)'and when C=1 the sum output is (A'+ (A^B))'and Cout is (B'. (A^B)'))'. Due to the intermediate signal C the delay and power is reduced. Further reduction of delay and power can be achieved by improving the XOR/XNOR circuits and transistor sizing. The proposed IHFA consists of 20 transistor and designed using modified XOR/XNOR and four Transistor 2-1 MUX style. Transmission gate (TG) style is used for the design of 2-1 MUX which has no leakage power and good full output swing.



(a)

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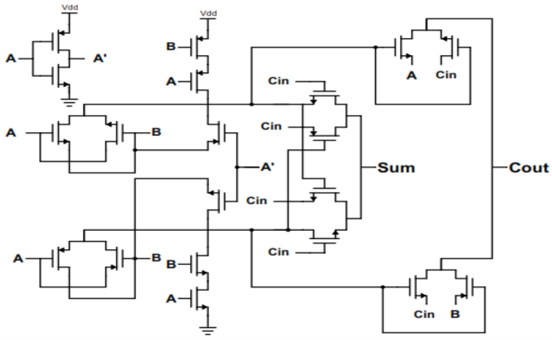


(b)

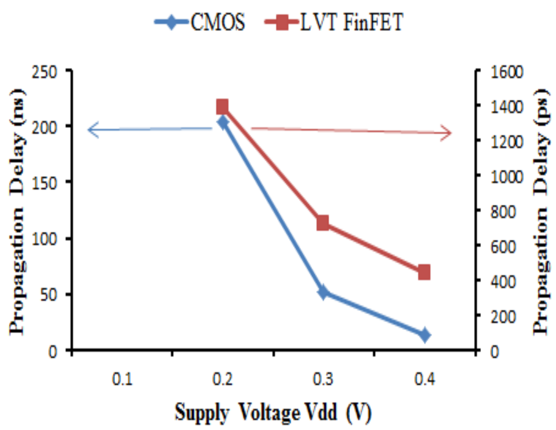
Figure 1: (a) Design of LVT FinFET based HFA; (b) Design of LVT FinFET based IHFA.

Based on the input combinations A, B, and Cin the output combinations Sum and Cout are selected. Due to this IHFA offers reduced delay, low power consumption, PDP, EDP and very high speed against the ultra-low voltage scaling.

III. PERFORMANCE ANALYSIS OF CMOS AND LVT FINFET BASED 1-BIT FULL ADDER

3.1 CMOS and LVT FinFET based performance analysis Of HFA with scaling supply voltage

The comparison of CMOS and LVT FinFET based HFA in terms of Propagation delay with supply voltage scaling is shown in the figure 2(a). FinFET suffers less dopant induced variation than standard CMOS which leads to better performance and lower delay. For the range considered LVT FinFET-HFA offers lower delay of ~146.7x to ~318.15x when compared with CMOS-HFA. Figure 2(b) presents the power consumption of FinFET and CMOS based HFA with supply voltage scaling. Due to faster switching and high current density LVT FinFET have lower power consumption. LVT FinFET HFA has ~5.43x to ~1.52x compared with CMOS-HFA. Power delay product (PDP) comparison of CMOS-HFA and LVT FinFET-HFA is shown in the figure 2(c).for the above reasons LVT FinFET-HFA has low PDP of ~27.04 times to ~20.80 times as compared with CMOS-HFA at supply voltage 0.2V.



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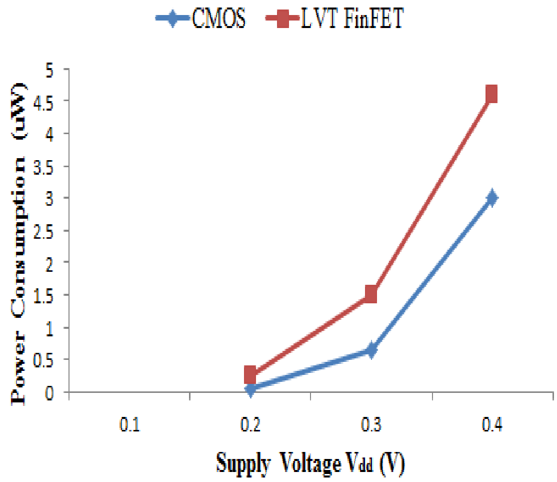

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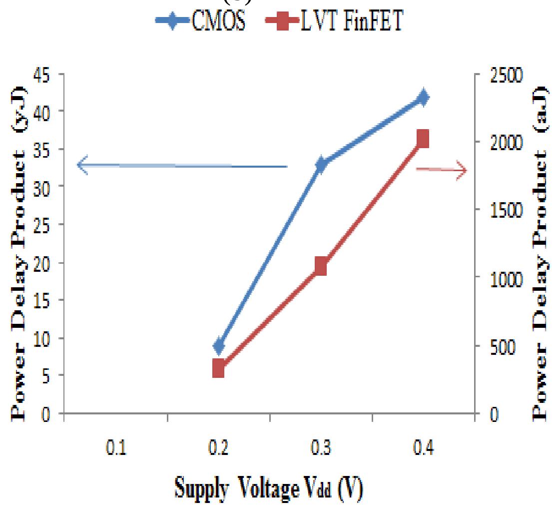
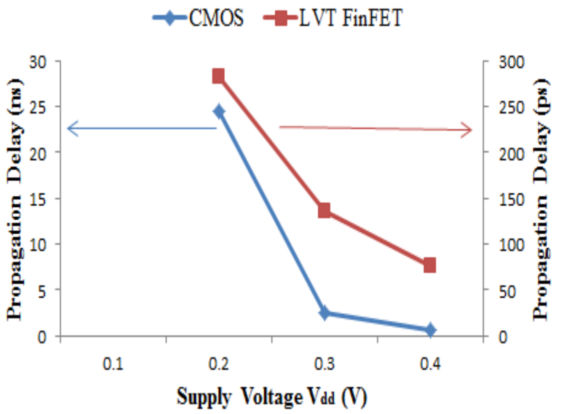


(c)

Figure 2: (a) Propagation delay; (b) Power Consumption; and (c) Power delay product comparison of CMOS and LVT FinFET based HFA design for the voltage range considered.

3.2 CMOS and LVT FinFET based performance analysis Of IHFA with scaling supply voltage

The comparison of CMOS and FinFET based IHFA in terms of Propagation delay with supply voltage scaling is shown in the figure 3(a). LVT FinFET–IHFA has lower propagation delay of ~86.54x to ~7.54x compared to CMOS-IHFA based adder designs for the 0.2 to 0.4 V due to less dopant induced variation. Figure 3(b) represents the power consumption of LVT FinFET and CMOS based IHFA for the voltage range considered. LVT FinFET-IHFA offers ~2.83 to ~0.33 compared with CMOS-IHFA for the voltages ranging from 0.2 to 0.4V due to the leakage currents. For all the above reasons LVT FinFET-IHFA has lower Power delay product (PDP) of ~30.54 times to ~22.35 times when compared with CMOS-IHFA is shown in figure 3(c).



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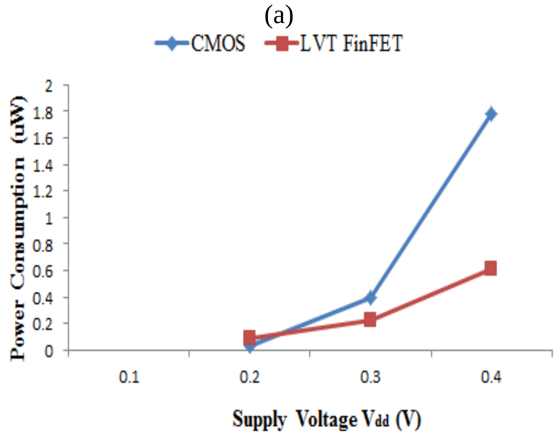

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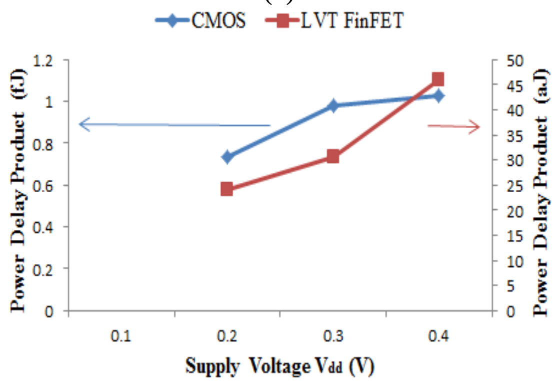

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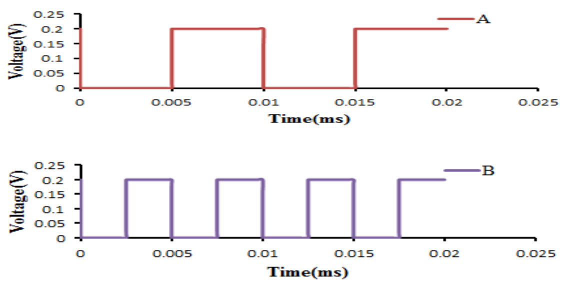
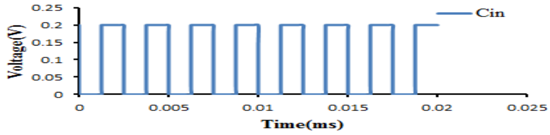
Figure 3: (a) Propagation delay; (b) Power Consumption; and (c) Power delay product comparison of CMOS and LVT FinFET based IHFA design for the voltage considered

IV. TRANSIENT ANALYSIS OF CMOS AND LVT FINFET BASED HFA AND IHFA DESIGNS AT LOW VDD

Transient analysis of CMOS and LVT FinFET based HFA and IHFA operated at Vdd=0.2V is presented in this section. The input A, B , Cin and the output signals (SUM ,Cout) of HFA are shown in figure 4(a-c).





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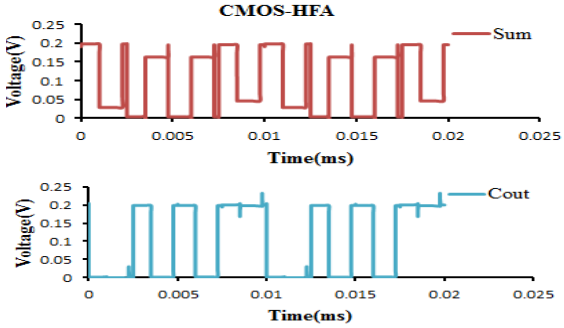

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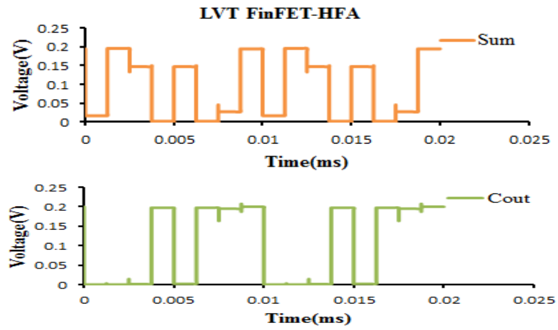
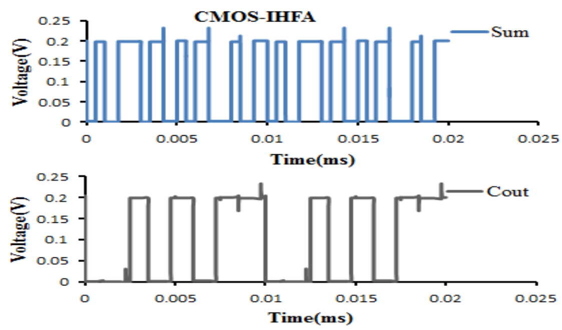


(c)

Figure 4: Transient analysis showing (a) inputs A, B, Cin (b) outputs of CMOS-HFA and (c) LVT FinFET-HFA at Vdd=0.2 V



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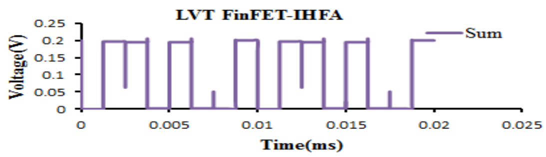

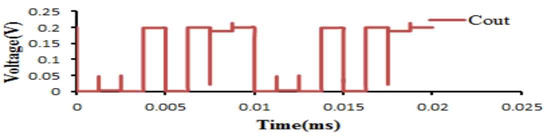

(b)

Figure 5: Transient analysis showing (a) outputs of CMOS-IHFA and (b) LVT FinFET-IHFA at Vdd=0.2 V

Due to the improved characteristics of FinFET, it offers good output swing when compared with standard CMOS. Figure 4(b) consists of glitches due to some Turn on voltage. Figure 5(a, b) shows the transient analysis outputs (Sum, out) of proposed CMOS and LVT FinFET based IHFA with full output swing. The output swing comparison table is shown below. The basic reason for glitches in CMOS is of due to on current and driving capability as compared to the LVT FinFET and these FinFETs have high on current and good driving capability.

V. COMPARISON OF LOGIC SWINGS AND PARAMETERS AT VDD=0.2V

Table1 presents the output voltage swings for Sum and Cout for the proposed CMOS and FinFET based HFA and IHFA. At 0.2V the LVT FinFET based HFA and IHFA have maximum logic swings which is reliable as compared with CMOS based HFA and IHFA.

Inputs			At 0.2V							
			CMOS-HFA		LVT FinFET-HFA		CMOS-IHFA		LVT FinFET-IHFA	
A	B	C	Sum	Cout	Sum	Cout	Sum	Cout	Sum	Cout
0	0	0	0.028	0.00006	0.0016	0.0001	0.0016	0.00001	0.00076	0.0002
0	0	1	0.197	0.007	0.195	0.0006	0.195	0.00063	0.196	0.0024
0	1	0	0.162	0.001	0.147	0.001	0.147	0.001	0.194	0.0031
0	1	1	0.034	0.198	0.001	0.197	0.001	0.197	0.001	0.198
1	0	0	0.162	0.002	0.147	0.001	0.147	0.001	0.194	0.0061
1	0	1	0.003	0.198	0.001	0.197	0.001	0.197	0.001	0.199
1	1	0	0.045	0.197	0.026	0.194	0.026	0.194	0.0078	0.188
1	1	1	0.195	0.199	0.194	0.199	0.194	0.199	0.199	0.199

Table2 Parameters (delay, power, PDP) comparison of CMOS and FinFET based HFA

Voltage (V)	CMOS-IHFA			LVT FinFET-IHFA		
	Delay (ns)	Power (uW)	PDP (fJ)	Delay (ps)	Power (uW)	PDP (aJ)
0.2	24.51	0.03	0.7353	283.2	0.085	24.072
0.3	2.46	0.398	0.979	135.7	0.2248	30.505
0.4	0.579	1.782	1.031	76.22	0.605	46.113

Table3 Parameters (delay, power, PDP) comparison of CMOS and FinFET based IHFA

Voltage (V)	CMOS-HFA			LVT FinFET-HFA		
	Delay (ns)	Power (uW)	PDP (fJ)	Delay (ps)	Power (uW)	PDP (aJ)
0.2	203.6	0.0432	8.795	1384	0.235	325.24
0.3	52	0.6317	32.848	723.6	1.49	1078.164
0.4	13.9	3.015	41.9085	436.9	4.61	2014.109

Table 2,3 shows the comparison for parameters such as delay, power and power delay product of CMOS and FinFET based HFA and IHFA. The analysis from the table describes that LVT- FinFET based HFA and IHFA have the better delay, power, power delay product and higher energy efficiency when compared with standard CMOS HFA and IHFA designs.

VI. CONCLUSION

This paper presents the internal logic structure and circuit operation using the devices, CMOS and Double gate FinFETs for designing the hybrid adder circuits at 0.2V. At transistor level two designs such as hybrid full adder (HFA) and improved hybrid full adder (IHFA) are designed. The LVT FinFET IHFA has 98.8% and 64.7% high speed and PDP respectively as compared with standard CMOS at 0.2V supply voltage. The analysis from the paper describes that double gate FinFET based HFA and IHFA have more energy efficiency as compared with standard CMOS. Thus the analysis shows that the double gate FinFET's are used for the technology scaling over the supply voltage range considered.

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