International Journal of Engineering and Advanced Technology (IJEAT)
ISSN: 2249-8958 (Online), Volume-8 Issue-6, August, 2019

Simulation of Single Phase Switching Capacitor 49 Level Inverter with Reduced THD

Ramesh Babu A, D.N.S Ravi Kumar, Geetha V

Abstract*: *The study of single phase Switched Capacitors Multi Level Inverter (MLI) is used with Switched Capacitor Converter (SCC) units. The SCC is used to increase the input DC voltage by connecting capacitor in string and shunt. This increassed DC link voltage is converted in to multilevel i.e. 49 level AC output. This SCMLI topology is used to reduce the number of switches, diodes, isolated dc power supply and Total Harmonic Distortion (THD). The SCMLI provides 49 level output voltage using 14 power switches and 3 isolated power supply. The performance of the SCMLI topology is confirmed by using MATLAB simulation result.

Index Terms*: *Boosted Voltage, Multilevel Inverter, Multiple DC links, Switched-Capacitor Converters and Tata Harmonic Distortion (THD).

I. INTRODUCTION

Nowadays multilevel inverters are increasing attention in industry and in electronic power conversion for high power application [2]. These converter applications are commonly seen in the growing groups of companies in the field. They promote the production from photovoltaic system to electrical grid [1]. In photovoltaic system is compared with other energy source, the current reaches focused with reduced manufacturing cost and increasing the production in overall system. These multilevel topologies are used in single phase converters [3].The multilevel inverter includes power semiconductors and capacitors voltage sources [4]. The advantage of using multilevel inverters is to increase the number of levels in the system and to improve harmonic content in the output waveform[5,6] and it also include high quality power with wide ranges of operation. Multilevel inverters is classified into three main topology namely neutral pointer (NPC), flying capacitor and cascaded multilevel (CM) [7, 8].The other technical aspects for the development of the multilevel inverter are modular realization, high availability, failure management and investment and life cycle cost [10].The drawbacks of conventional MLI's are need of more components like diode, capacitor & switches in addition to more input voltage sources [11, 14, 15].The main disadvantage of conventional MLI is overcome by using sub multi level inverter. The sub multilevel inverter consists of H-bridge inverter with switched capacitor. The level of output voltage increased by increasing the components still again [12-[13]. The terms of number of power switches, power rating of switches and switching losses cannot be calculated by presenting the mathematical formulas. The multilevel inverters are cost effective and also efficient solution for high power to medium voltage DC-AC conversion.[11].The main objective of SCC is to reduce THD value below 3% comparing other technique [16] [17]. The SCMLI structure is based on the proposed by SCC models. These are introduced to get high voltage level (even to odd) than existing developed topology. The SCMLI system does not need any H-bridge cell. The THD of SCMLI is reduced by increasing the number of level, but by increasing the level it leads to complexity of the circuit. The usages of these converters in various applications are Variable speed motor drives, High voltage system interconnections, Converter with harmonic distortion capacitor and Sinusoidal current rectifier.

II. PROPROPOSED SWITCHED CAPACITOR MLI

The proposed SCMLI system provides 49 level output voltage. This is obtained by 3 isolated dc power supply with the help of switched capacitor multilevel inverter (SCMLI) topology. In this system pure sinusoidal waveform is obtain with the output waveform. This topology is used for reducing the THD of the system.

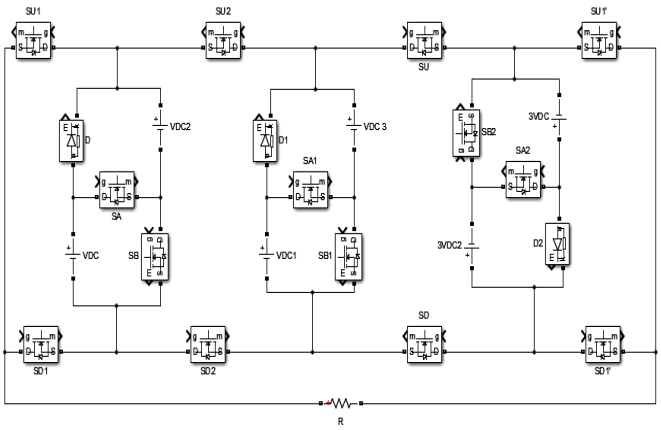

Fig.1 Representation Of 49 Levels With SCMLI Topology

Revised Manuscript Received on October 30, 2019.

* Correspondence Author

A.RameshBabu*, B.E. degree in Electrical&Electronics Engineering from manonmaniam sundaranar university, Tirunelvelli, India in 2001.

D.N.S Ravi Kumar, PhD in the field of Vehicular Communication (Distributed Embedded Systems) from Sathyabama Institute of Science and Technology since 2015,Chennai India.

V.Geetha, Ph. D under the faculty of Electrical and Electronics Engineering at Sathyabama Institute of Science and Technology,Chennai, India.

© The Authors. Published by Blue Eyes Intelligence Engineering and Sciences Publication (BEIESP). This is an open access article under the CC BY-NC-ND license (http://creativecommons.org/licenses/by-nc-nd/4.0/)

The figure 1 contains of 3 SCC and one SCMLI. Each SCC has two power switch, one diode and capacitor. This circuit diagram contains of 14 switches. These switches are classified into external switches and internal switches. It contains 8 external switches and 6 internal switches as seen in the SCC. Each MOSFET have internal diode in parallel with a series RC snubber circuit.

A) Switch Capacitor Converter (SCC)

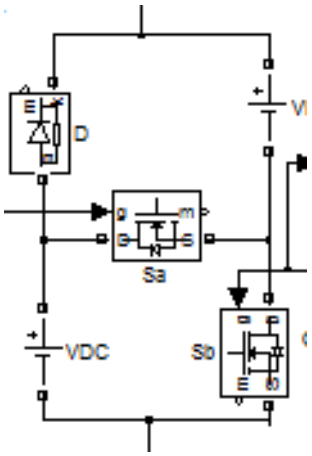

Fig.2 Construction of single SCC

The switching in SCC is classified into two modes namely hard switching and soft switching. The SCC contains of two MOSFET and one Diode. This proposed circuit is called basic unit. The circuit consists of dc power supply, one capacitor, one passive power diode and two active power switches. On the other hand these inverters are having three similar SCC units in the proposed SCMLI, with two isolated dc voltage sources and 2n capacitors are needed .Three dc voltage sources are utilized in the switching pattern (asymmetrical).

B) Switching Pattern

Table 1 Switching Pattern of the Proposed SCMLI

s

Voltage Level	Switching devices	Switching Voltage
1	SD1,SD2,SD, SD1'	0
2	SB,SU2,SU,SU1',SD1	VDC2
3	SA,SU2,SU,SU1',SD1	VDC,VDC2
4	SA2,SU1,SU2,SU, SD1'	3VDC,3VDC2
5	SU,SU2,D,SA,SB,SD1,SD1'	3VDC
6	SA,SA2,SU2,SU,SD1,SD1',D2	VDC,VD2,3VDC
7	SB2,SU1,SU2,SU,SD1'	VDC2,3VDC2
8	SB,SB2,SU2,SU,SD1,SD1'	VDC2,3VDC2
9	SA,SB2,SU2,SU,SD1,SD1'	VDC,VD2,3VDC2
10	SB1,SU,SU1',SD1,SD2	VDC3
11	SA,SB1,SU1,SU,SD2,SU1',D,SB	VDC3
12	SB,SB1,SB2,SU1,SD2,SD1'	VDC2
13	SB1,SA1,SU,SD1,SD2,SD1'	VDC3,3VDC,3DC2
14	SA,SB1,SB2,SU1,SU,SD2,SD1',D	VDC3,3VDC2
15	SB,SB1,SB2,SU1,SU,SD2,SD1'	VDC2,VDC3
16	SB1,SB2,SU,SD1,SD2,SD1'	VDC3,3VDC2
17	SA,SA1,SU1,SU,SU1',SD2, D, B, SU	VDC1,VDC3
18	SB,SA1,SU1,SU,SU1',SD2	VDC2,VDC1,VD3
19	SA1,SU,SU1',SD1,SD2	VDC1,VDC3
20	SA,SA1,SA2,SU1,SU,SD2,SD1',D,SB	VDC1,VDC3,3VDC,3VDC2
21	SB,SA,SA2,SU1,SU,SD2,SD1'	VDC2,VDC1,3VDC,3VDC2
22	SA1,SA2,SU,SD1,SD2,SD1'	VDC1,VDC1,VD3,3VDC,3VDC2
23	SB,SA1,SB2,SU1,SU,SD2,SD1',D,SB,	VDC1,VDC3
24	SB,SA1,SB2,SU1,SU,SD2,SD1'	VDC2,VDC3,3VDC2
25	SA1,SB2,SU,SD1,SD2,SD1'	VDC1,3VDC2
26	SB,SA1,SB2,SU1,SU,SD2,SD1'	VDC2,VDC3,3VDC2
27	SB,SA1,SB2,SU1,SU,SD2,SD1', D,SB	VDC1,VDC3
28	SA1,SA2,SU,SD1,SD2,SD1'	VDC1,VD3,3VDC,3VDC2
29	SB,SA,SA2,SU1,SU,SD2,SD1'	VDC2,VDC1,VD3,3VDC,3VDC2
30	SA,SA1,SA2,SU1,SU,SD2,SD1', D,SB	VDC1,VDC3,3VDC,3VDC2
31	SA1,SU,SU1',SD1,SD2	VDC1,VDC3
32	SB,SA1,SU1,SU,SU1',SD2	VDC2,VDC1,VD3
33	SA,SA1,SU1,SU,SU1',SD2, D,SB, SU	VDC1,VDC3
34	SB1,SB2,SU,SD1,SD2,SD1'	VDC3,3VDC2
35	SB,SB1,SB2,SU1,SU,SD2,SD1'	VDC2,VDC3
36	SA,SB1,SB2,SU1,SU,SD2,SD1'	D,VDC3,3VDC2
37	SB1,SA1,SU,SD1,SD2,SD1'	VDC3,3VDC,3VDC2
38	SB,SB1,SB2,SU1,SD2SD1'	VDC2
39	SA,SB1,SU1,SU,SD2,SD1'	D,SB,VDC3
40	SB1,SU,SU1',SD1,SD2	VDC3
41	SA,SB2,SU2,SU,SD1,SD1'	VDC,VDC2,3VDC2
42	SB,SB2,SU2,SU,SD1,SD1'	VDC2,3VDC2
43	SB2,SU1,SU2,SU,SD1'	VDC2,3VDC2
44	SA,SA2,SU2,SU,SD,SD1',D1	VDC,VD2,3VDC
45	SB,SA2,SD1,SU2,SU,SD1'	3VDC
46	SA2,SU1,SU2,SU,SD1	3VDC,3VDC2
47	SA,SU2,SU,SU1',SD1	VDC,VDC2
48	SB,SU2,SU,SU1',SD1	VDC2
49	SD1,SD2,SD,SD1	0

The above table 1 denote the switching pattern of 49 level inverter. The switching pattern explains in detail about the operation of the proposed SCMLI. In level1 operation SD1, SD2, SD, SD1' switches are conducting. In this mode of operation, no voltage source is connected. In level2 operation the order of switches SB, SU2, SU, SU1 and SD1 are conducting. In this mode of operation source VDC2 is active. In level3 of the inverter, the order of operating switches are SA, SU2, SU, SU1' and SD1.In this mode VDC and VDC2 sources are active. When level4 operation begins the switches SA2, SU1, SU2, SU, SD1' and the sources 3VDC, 3VDC2 are active. When level5 of the converter working with the switches SB, SA2, SD1, SU2, SU, SD1', 3VDC source is active. In level 6 the order of operation of switches is SA, SA2, SU2, SU, SD, D1, SD1'. VDC, VDC2, 3VDC sources are active in this mode. When the 7^{th} level voltage is applied to the inverter, the order of operation of switches are SB2, SU1, SU2, SU, SD1', only VDC2, 3VDC2 sources are active. When the 8^{th} level voltage is given to the inverter then the operating switches will be SB, SB2, SU2, SU, SD1, SD1'.Three source voltages VDC, VDC2, 3VDC2 are active. In 9^{th} level voltage is applied to the inverter, the order of active switches are of SA, SB2, SU2, SU, SD1, SD1'. The active voltage sources of the 9^{th} level are VDC, VD2, and 3VDC2. When the 10^{th} level operation starts the order of active switches are SB1, SU, SU1', SD1, SD2 .In this mode of operation VDC3 source is active. In 11^{th} level the order of operation will be SA, SB1, SU1, SU, SD2, SD1', D and SB. In this mode only VDC3 source is active. In 12^{th} level the operation will be SB, SB1, SB2, SU1, SD2 and SD1' during this mode of operation switching voltage source VDC2 is active. In 13^{th} level order of the switches under on condition will be SB1, SA1, SU, SD1, SD2, SD1'. In this mode of operation the active voltage sources are VDC3, 3VDC, 3DC2. In level 14 switches inn active condition are SA, SB1,SB2, SU1, SU, SD2, SD1'. VDC3, 3VDC2 sources are active.

In 15th level SB, SB1, SB2, SU1, SU, SD2, SD1' switches are active. In 16th level active switches are SB1, SB2, SU, SD1, SD2, SD1'and active voltage sources are VDC3, 3VDC2 .In 17th level order of switches under on condition are SB, SU2, SU, SU1 and SD1. In this mode of operation VDC2 is active. Under 18th level the order of operation will be SA, SU2, SU, SU1' and SD1.In this mode of operation VDC and VDC2 sources are active. In 19th level switches under on condition are SA2, SU1, SU2, SU and SD1'.The voltage source active are 3VCD1 and 2VDC2. In level 20 order of the switches will be SA, SA1, SA2, SU1, SU, SD2, SD1', SB. In this mode of operation VDC1, VDC3, 3VDC, 3VDC2 sources are active.

In level 21 active switches are SB, SA, SA2, SU1, SU, SD2, SD1', sources VDC2, VDC1, VD3, 3VDC1, 3VDC2 are active. In level 22 the order of switches are SA1, SA2, SU, SD1, SD2, and SD1' are active. In this mode of operation VDC1, VDC1, VD3, 3VDC1, 3VDC2 sources are active. In 23rd level voltage operation will begin with switches SB, SA1,SB2,SU1,SU,SD2,SD1', D,SB. The sources VDC1, VDC3 are active. In 24th level the voltage path will be SB, SA1, SB2, SU1, SU, SD2, SD1'.The voltage sources VDC2, VDC3, 3VDC2 are active .In 25th level order of switches are SA1, SB2, SU, SD1, SD2, SD1'. In this mode of operation VDC1, 3VDC2 are active. In 26th level the order of operation will be SB, SA1, SB2, SU1, SU, SD2, SD1'. In this mode of operation the voltage sources VDC2, VDC3, 3VDC2 are active. In 27th level the operation will be SB, SA1, SB2, SU1, SU, SD2, SD1' D, SB. Voltage sources like VDC1, VDC3 are active. In 28th level order of the active switches are SA1, SA2, SU, SD1, SD2, SD1'. In this mode of operation sources VDC1, VD3, 3VDC1, 3VDC2 are active. In 29th level the active switches are SB, SA, SA2, SU1, SU, SD2, SD1'. In this mode of operation VDC2, VDC1, VD3, 3VDC1, 3VDC2 are active. I n 30th level the order of operation will be SA, SA1, SA2, SU1, SU, SD2, SD1', D, SB. In this mode of operation sources VDC1, VDC3, 3VDC1 are active.

In 31st level operation of the switches are SA1, SU, SU1', SD1, SD2. The voltage sources VDC1, VDC3 are active. In 32nd level voltage the order of switches are SB, SA1, SU1, SU, SU1', SD2 .In this mode of operation VDC2, VDC1, VD3 are active. In 33rd level order of operation will be SA, SA1, SU1, SU, SU1', SD2 .In this mode VDC1, VDC3 sources are active. In 34th level switches in on condition are SB1, SB2, SU, SD1, SD2, SD1' and during this level active voltage sources are VDC3, 3VDC2. In 35th level the order of the switches will be SB, SB1, SB2, SU1, SU, SD2, SD1'. In this mode of operation voltage sources VDC2, VDC3 are active. In 36th level the order of switches in on state are SA, SB1, SB2, SU1, SU, SD2, SD1'.In this mode of operation VDC3, 3VDC2 are active.

In 37th level the order of operation will be SB1, SA1, SU, SD1, SD2, SD1'. In this mode of operation voltage sources VDC3, 3VDC, 3DC2 are active. In 38th level the operation of the switches will be SB, SB1, SB2, SU1, SD2, SD1', voltage source VDC2 is active. In 39th level volt order of switches will be of SA, SB1, SU1, SU, SD2, SD1' and the voltage source active is VDC3 .In 40th level the order of switches in on states are SB1, SU, SU1', SD1, SD2 . In this mode of operation VDC3 is active. When 41st level the order of operation of the switches is SA, SB2, SU2, SU, SD1, SD1'and active voltage sources are VDC, VD2, 3VDC2. In 42nd level the operation will be SB, SB2, SU2, SU, SD1, and SD1' and voltage sources VDC2, 3VDC2 are active. In 43rd level the order of the switches will of SB2, SU1, SU2, SU, SD1'. In this mode of operation VDC2, 3VDC2 are active. In 44th level the order of switches are SA, SA2, SU2, SU, SD, SD1'. In this mode of operation VDC, VD2, 3VDC1, are active.

In 45th level the order of operation will be SB, SA2, SD1, SU2, SU, SD1'. In this mode of operation voltage source 3VDC1 is active. In 46th level the operation will be SA2, SU1, SU2, SU, and SD1. Voltage sources 3VDC1, 3VDC2 are active. In 47th level the order of switches are SA, SU2, SU, SU1', SD1. In this mode of operation voltage sources VCC, VDC2 are active. In 48th level the order of switches are SB, SU2, SU, SU1', SD1. In this mode of operation VDC2 is active. In 49th level the order of operation will be SD1, SD2, SD, and SD.

III. SIMULATION RESULT

The proposed SCMLI simulation diagram is shown in figure 3. It is made up of MOSFET, Diode, capacitor and three separate DC source. The separate DC source values are 1, 3, 9 volt. The driving pulses of the SCC switches and external switches are generated by using look up table. The look up table is created by using repeating table. The level of the output voltage is verified by using scope, which is connected across the R-load.

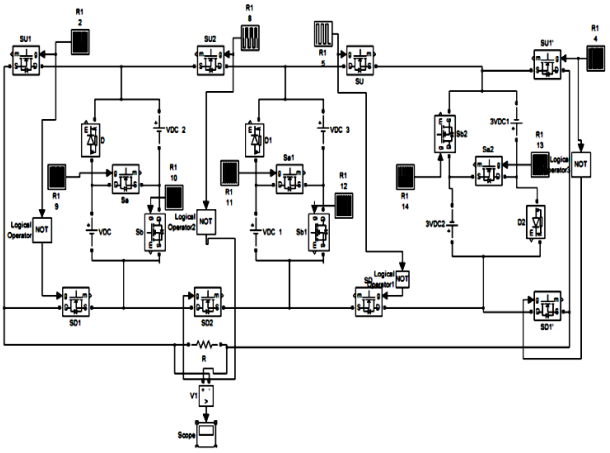

Fig.3 Simulation of SCMLI (49 level)

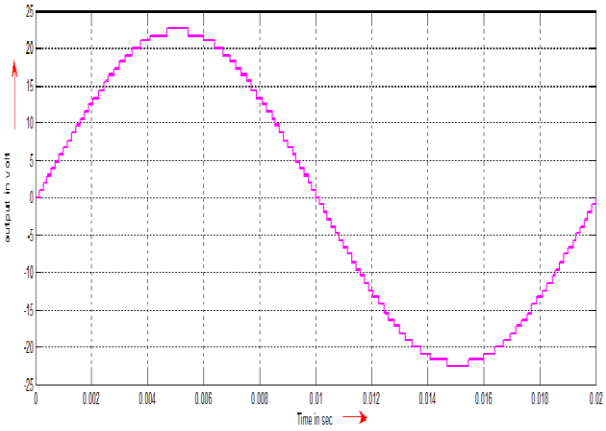

Fig.4 Simulation result of proposed 49 level SCMLI

Output waveform of the simulated SCMLI is seen in the Fig 4. The THD value obtained in 49 level inverter is 1.86%.

By using 2 isolated switches the THD value is 5.5%. By comparing both isolated switches THD value is lesser than 3%. The above list [fig 5] obtained by FFT analysis. It contains sampling time for the system is 5e-005s, samples per cycle in the operation are 400 and fundamental range of the system is 22.29peak (15.76 rms). The maximum harmonic frequency used to calculate the THD in the range of 9950.00Hz.This list also gives step by step frequency range with respective degree.

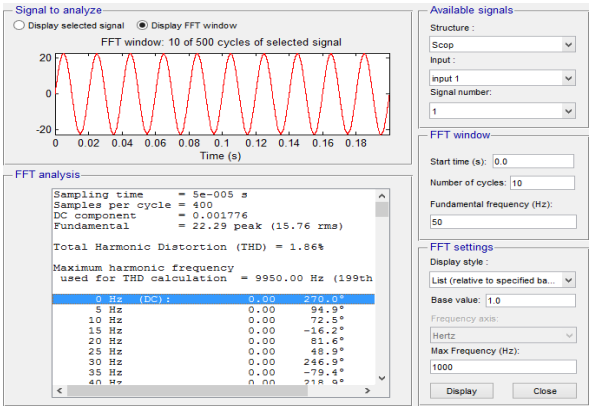

Fig 5 THD Value Of Proposed 49 Level SCMLI

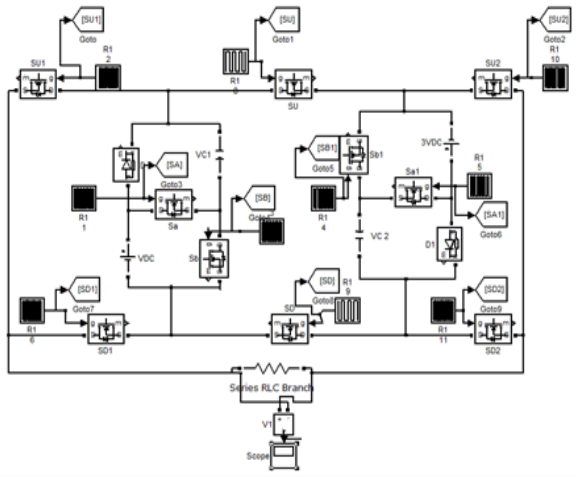

Fig 6 Simulation Of The17 Level Inverter

The description of the 17 level inverter and its simulation circuit is depicted in Fig 6 and the number of switched capacitor cell is two in 17 level and for 49 level the number of cell is three and its result of 17 level output voltage is shown in Fig 7.

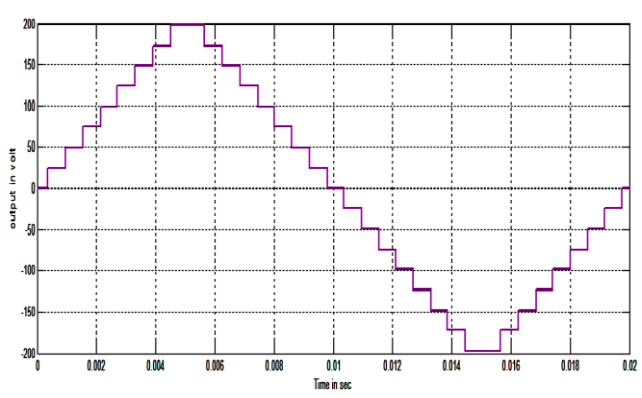

Fig 7 Simulation Result Of The 17 Level Inverter

Table 2 Comparison of result of proposed 49 level SCMLI

Sl. No	Comparison	3 Isolated Switches	2 Isolated Switches
1	No of switches	14	10
2	No of level obtain	49	17
3	THD	1.86%	5.5%
4	Output	1:3	1:3:9
5	Voltage Level	49 level	17 level

The comparison table between 17 level and 49 level is shown in table 2.The result comparison proves that the 49 level output shows the output with better THD and the output ratio is comparatively high compared to 17 level.

IV. CONCLUSION

The main advantage using this topology is to reduce the harmonic distortion in the output level this proposes a SCC topology with reduced number of switches. The SCC circuit proposed by binary asymmetrical algorithm as they are self balancing .The SCC units as dc link with only from the proposed system we can obtain14 active power switches, three isolated dc power supplies and three capacitors with 49 level inverter. This paper gives out switching characteristic, less power factor and 49 level output waveform. The proposed topology is used to reduce number of switches, diodes; total block voltage and cost of the system will be same of other topologies. Finally the performance of proposed 49 level SCMLI topology have been verified.

REFERENCES

1. Javier chavarria, Domingo, Francese Guinjoan, Carlos Meza and Negroni "Energy -balance control of cascaded multilevel grid -connected inverters under level-shift and phase –shift PWM"IEEE trans ind.electronic.Vol.60, No.1,Jan 2013.
2. Samir kouro,Mariusz Malinowski, Gopakumar, Josep Pou,Leopoldo,Jose Rodriguez,marcelo A.Perez and Jose I.Loen "Recent advances and industrial applications of multilevel converts"IEEE trans ind.electronic.vol-57,No.8,August 2010.
3. Giampaolo Buticchi,Emilio Lorenzani and Giovanni"A five level single phase grid-conned converter for renewable distributed systems"IEEE trans ind.eletronic .Vol.60, No.3, March2013.
4. Jose Rodriguez, Jih-Sheng and Fang Zhen "Multilevel inverters: a survey of topologies , controls and applications" IEEE tran ind.electronic.Vol.49,No.4,August 2002.
5. Engin Ozdemir,Sule Ozdemir and Leon M. Tolbert"Fundamental –frequency-modulate six-level diode –clamped multilevel inverter for three phase stand-alone photovoltaic system" IEEE tran ind.electonic.Vol.56, No.11, November 2009.
6. Moncef Ben Smida and Faouzi Ben Anmar"Modelling and DSC-PSC-PWM control of a three phase flying-capacitor stacked multilevel voltage source inverter"IEEE tran ind.electonic.Vol57, No.7, July 2010.
7. Javier Pereda and Juan Dixon"Cascaded multilevel converters : optimal asymmetries and floating capacitor control" IEEE tran ind.electronic.Vol.60, No.11 ,November 2013.
8. Atollah Mokhberdoran and Ali Ajami"Symmetric and asymmetric design an implementation of new cascaded multilevel inverter topology"IEEE tran on power electonic Vol.29, No.12, December 2014.

9. Mostafa Khazraci,student member,IEEE, Hossein Sepahvands,student memberIEEE,Keith A.Corzine, senior member,IEEE and Mehdi Ferdowsi,member IEEE"Active caacitor voltage balancing single -phase flying - capacitor multilevel power conver"IEEE trans. on industrial electronics vol. 2,Feb. 2012.
10. Krishna Kumar Gupta,Shaliendra Jain "Comprehensive review of a recently proposed multilevel inverter"IET power electron. Vol.7, 2014.
11. V.Geetha, V.Sivachidambaranathan," Multi carrier PWM switching technique for multilevel inverter for various loads", 6th International Conference on Computation of Power, Energy, Information and Communication, ICCPEIC 2017, 1758-0270,23March 2017,pp-568-574.
12. V.Geetha, V.Sivachidambaranathan," Double frequency SPWM inverter topology for PV systems", 6th International Conference on Computation of Power, Energy, Information and Communication, ICCPEIC 2017, 1758 - 0270,23 March 2017,pp-800-803.
13. Kui Wang, member,IEEE Yongdong Li,member of IEEE,Zheneng Zheng,member,IEEE and Lie Xu ,member IEEE"Voltage balancing and fluctuation - suppression method of floating capacitor in a new modular multilevel converter"IEEE trans on industrial electronics ,Vol 60.No 5,may 2013.
14. K. Selvamuthukumar, M. Satheeswaran and A. Ramesh Babu," Single phase thirteen level inverter with reducednumber of switches using different modulation techniques" ARPN Journal of Engineering and Applied Sciences, Vol. 10, No 22, ISSN 1819-6608,pp 10455-10462, Dec. 2015.
15. A. Ramesh Babu," Comparative Analysis of Cascadeded Multilevel Inverter for Phase Disposition and Phase Shift Carrier PWM for Different Load" Indian Journal of Science and Technology, ISSN 0974-5645 Vol 8(S7), 251-262, April 2015.
16. Babu, A. Ramesh, and T. A. Raghavendiran. "Performance analysis of novel three phase High step-up dc-dc interleaved boost converter using coupled inductor." In Circuit, Power and Computing Technologies (ICCPCT), 2015 International Conference on, pp. 1-8. IEEE, 2015.
17. Babu, A. Ramesh, and T. A.Raghavendiran. "Analysis of non-isolated two phase interleaved high voltage gain boost converter for PV application." In Control, Instrumentation, Communication and Computational Technologies (ICCICCT), 2014 International Conference on, pp. 491-496. IEEE, 2014.

AUTHORS PROFILE

A.RameshBabu has completed B.E. degree in Electrical&Electronics Engineering from manonmaniam sundaranar university, Tirunelvelli, India in 2001. He got his M.E. in Power Electronics and Industrial Drives from Sathyabama University Chennai, India in 2008. He is life member of Indian Society for Technical Education(ISTE). Presently he is pursuing ph.D. program at Sathyabama University Chennai, India. His Research interest include DC-DC Boost converter for PV application.To his contribution he has published more than 30 papers indexed in scopus and web of science

D.N.S Ravi Kumar has completed his M.Sc.(Applied Electronics) in the year 2003 from Bharathiyar University Coimbatore ,India and M.E Applied Electronics in the year 2006 from Sathyabama Institute of Science & Technology Chennai India.He is pursing PhD in the field of Vehicular Communication (Distributed Embedded Systems) from Sathyabama Institute of Science and Technology since 2015,Chennai India.His field of intrests includes Embedded Systems ,Vehicular Communication and Robotics. He is currently working on Smart car Technology (V2V).Apart from research an innovator to spark startups from ideas to implementation.

V.Geetha was born in India on june 18, 1984, has received her B.E degree in Electrical and Electronics Engineering from Anna university, Tamilnadu, India in 2005 and M.E degree in Power electronics and industrial drives from Sathyabama institute of science and technology, Tamilnadu, India in 2008. She is pursuing her Ph. D under the faculty of Electrical and Electronics Engineering at Sathyabama Institute of Science and Technology from 2015. Her research interest includes Fuzzy logic controller, Artificial Neural network and Power Electronic Converters for induction heating application.published more than 10 scopus indexed journals and attended more than 5 international conferenceas and a life time member in IAENG..