International Journal of Engineering and Advanced Technology (IJEAT)
ISSN: 2249-8958 (Online), Volume-8 Issue-6, August, 2019

Resilient Soft-Error Endurable Latch Design

J.Sofia Priya Dharshini, B. Sirisha

Abstract*: Errors may occur in the circuit output because of upset in the stored or communicated charge. Such errors are considered as Transient Faults. The Transient Fault (TF) causes the soft error in the circuit output. So, designing of the latches which are unsusceptible to the Transient Faults disregarding the hitting particles energy is proposed in this project. Traditionally the soft-error based VLSI is limited to applications which require high reliability and operated in high radiation environment such as avionics applications, medical equipments, space industry and military applications. However, CMOS technology scales down to nanometre region, VLSI circuits also get affected by soft errors at ground level which features low radiation energy. Here, in this paper, totally three soft error tolerant latch designs are proposed, which includes High Performance, low cost and resilient soft error endurable latch, HLR-CG, HLR-CG1 and modified HLR-CG1. The proposed designs achieve better reliability with lower power consumption, delay, power delay product and area. The latches proposed are implemented in 45 nm technology and 32 nm technologies.

Index Terms: Transient Fault, Soft Error, radiation hardening, reliability.

I. INTRODUCTION

As CMOS technology keeps scaling down, circuit designers face a lot of challenges. The amount of charge that can be stored on a node reduces as the supply voltage and capacitance at the node scale down. This result in the circuit prone to noise which is occurred due to the high-energy neutrons those are emerged from the cosmic rays, alpha particles produced from packaging materials. [3], [4], [5].
Alpha particles in the radioactive impurities of device materials, neutrons from high-energy cosmic rays and neutron induced 10B fission are the three different radiation sources which could induce Soft Error in the circuit. The energy particles with less energy can easily affects the smaller CMOS devices, which leads to more rates of soft errors.Area per bit decreases as well, with the scaling down in CMOS technology. This results in reduction of amount of average node capacitance. In order to preserve the electrostatics of the circuit and to avoid failure caused by the high electric fields, the supply voltage also scaled down. The net effect of decrease in node capacitance and the supply voltage is that the amount of charge stored at a specific node is going down every generation. This causes in increased vulnerability of latches and flip-flops to the soft errors caused by the radiation [7], [8], [9],[10].

A DICE cell [10] which is a storage cell is introduced in order to overcome the problem of single-event-upsset. These storage cells can be used in designing of the flip-flops and static RAM cells.

The robustness of the execution does not rely on the transistor size or the capacitance at the nodes of the cell. The novel cells designed in [11] are dominant in the aspect of area, power and radiation hardening.

The Robustness of latches can be increased by increasing the capacitance at the internal node or by changing the transistors sizes. So, the latch circuit need additional charge to change its voltage and it will endure the Transient fault with certain energy levels. To achieve this some techniques are proposed [12] [13] [2]. In [16] another technique is proposed to get fully immune soft error independent to hitting particle energy. But, when clock gating (CG) is implemented to the device, it results in floating values of the voltage at output which may be caused either by the charging or discharging of the leakage current or by TF occurred at any other internal node of the device. This may still results in wrong logic at the output stage.

These soft error tolerant latch techniques are based on increasing the size of the capacitance of internal nodes using redundant transistors. These techniques and techniques discussed before can only attenuate the soft error and the performance of these designs still fail due to TF caused by high energy particles and in some of the previously discussed techniques not all the internal nodes are safeguarded. The objective of this paper is to propose novel techniques to harden latch circuits with low power consumption in CMOS. These techniques offer better features when compared with the some of the techniques found in the technical literature. In this paper four different latch circuits are proposed those are with increased speed, low cost and resilient against the Transient Fault occurred. All proposed latches endure TFs irrespective to their energy levels and striking area. Initially, a unique latch which is High speed-Low cost and Resilient (HLR) latch is proposed. Later two more latches (HLR-CG and HLR-CG1) which are convenient to use with clock gating design are introduced. There is another resilient latch introduced, a Modified HLR-CG1, which can be implemented with clock gating with reduced cost; these proposed latches are implemented in 32 nanometre technology. When TF occurs at any of the internal nodes of HLR, the output will last in a high impedance state. If this occurs in a device with clock gating system, in latching mode, SE may occur at the output of the device due to the high impedance node when TF occurs at another node or due to the leakage current. With scaling in the CMOS technology, as the threshold voltage reduces the leakage current raises exponentially.

Revised Manuscript Received on October 30, 2019.
* Correspondence Author
Dr.J.Sofia Priya Dharshini*, Dept. of ECE, RGMCET, Nandyal, AndhraPradesh,India.
Mrs.B.Shirisha, Dept. of ECE, RGMCET, Nandyal, AndhraPradesh,India.

However, the frequency for operation of the latch circuit also increases. For system without clock gating system, the node which is in high impedance state will remain in this state for less than half clock cycle which is very short period for leakage current that it cannot charge or discharge the node with high impedance state. Thus, if clock gating is not applied to the proposed HLR latch circuit then it is not expected to have this issue. In order to overcome this issue when CG is applied, another two latch designs HLR-CG and HLR-CG1 are proposed. When these two latch designs are compared to HLR circuit design, the output nodes of HLR-CG and HLR-CG1 latches will not reach the high impedance state when TF occurs at any of the internal nodes of corresponding latch. Therefore, HLR-CG and HLR-CG1 are considered to be apt for systems with clock gating (CG).

II. PROPOSED HLR LATCH AND ITS IMPLEMENTATION

The proposed HLR latch is implemented in 32 nanometre technology, at room temperature with clock frequency 200 MHz at 0.35V power supply. In transparent mode that is when CLK=1, all the transmission gates TG1, TG2 and TG3 are in ON state and input passes through the transmission gate TG2 to output Q. Internal node d1 is connected to transmission gate TG1 and d2 is connected to transmission gate TG3. Internal node d1 drives the internal node d1b through the inverter I1, and similarly, internal node d2 drives the internal node d2b through the inverter I2. The CMOS circuit in the feedback circuits gets turned OFF because of the clock signal applied in the feedback circuit. This helps in preventing the possible conflict at the internal nodes d1 and d2. The MOSFETs T1 to T6 at the output stage also gets turned OFF because of the clock signal. This helps in preventing the possible conflicts at the output stage. Here, input D biases all the internal nodes of the circuit.

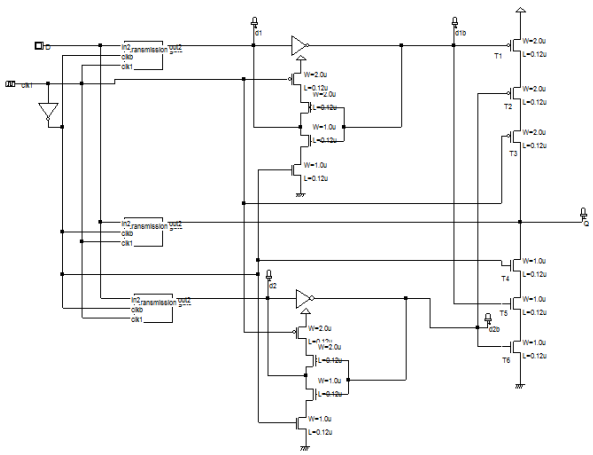

Fig.1. HLR Latch Circuit

In latch mode that is when clock is low (clk =0), the transmission gates TG1, TG2 and TG3 get turned OFF. So, the internal nodes d1, d2 and output Q get disconnected from input D. The feedback circuits get turned ON because the clock is 0. Due to the clock=0, the MOSFETs T1 to T6 at output get turned ON as well. The internal nodes d1 and d1b are controlled by the inverter I1 and corresponding feedback circuit. Similarly, the internal nodes d2 and d2b are controlled by the inverter I2 and corresponding feedback network. So, the output voltage Q is controlled by output stage which is driven by the internal nodes d1b and d2b

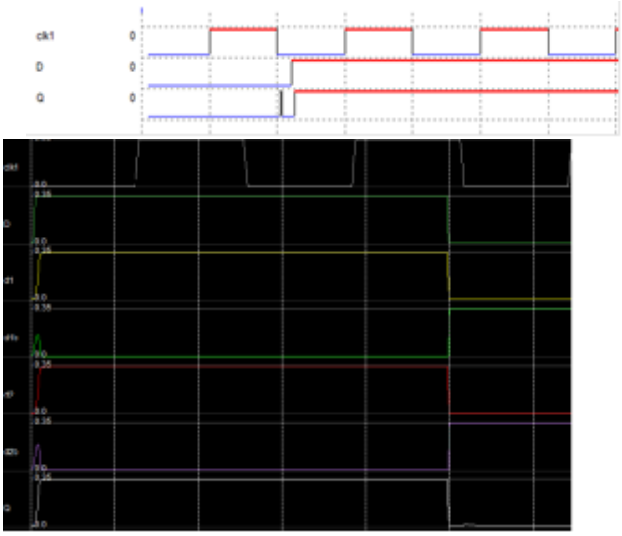

Fig.2. HLR Latch Simulation Without Error

Now considering the transient fault occurred at individual internal nodes. 1).Q=1, d1b=d2b=0; d1=d2=1; Transistors T1 and T2 ON and T5 and T6 OFF. If Transient Fault occurs at internal node d1, the voltage level at internal node d1b flips to '1' and Transistor T1 turns OFF where as the transistor T5 turns ON. Thus, path from Q to Vdd gets disconnected by leaving output Q at high impedance state. Thus, the correct logic is still maintained at Q. 2). Q=0, d1b=d2b=1; d1=d2=0; Transistors T1 and T2 in OFF state and T5 and T6 in ON state. If Transient fault occurs at d1, the voltage level at internal node d1b flips to '0'.The path connecting from output node Q to GND gets disconnected and Q lies in high impedance state. Thus the correct logic is still preserved at output Q. This can be understood by observing the Fig. 3 Which shows the simulation result of HLR latch with TF at internal node d1.

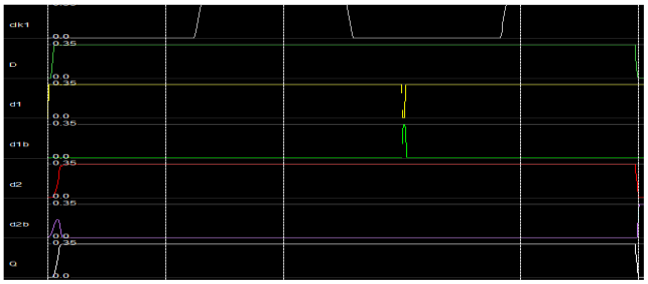

Fig.3. HLR latch simulation result with TF at d1

In the same way, When HLR latch is in latch mode, if Transient Fault occurs at internal node d2, the Transistors T2 and T6 change their state and thus, the path gets disconnected from Q to Vdd or GND. Output Q reaches high impedance state. Thus, the output logic maintains its correct logic state. Fig.4 represented below shows the simulation result when TF occurs at d2. Same process occurs when TF affects the internal nodes d1b and d2b, thus the output Q remains at its correct logic state.

Fig 5 and Fig 6 represents the simulation of HLR when TF affects d1b and d2b respectively.

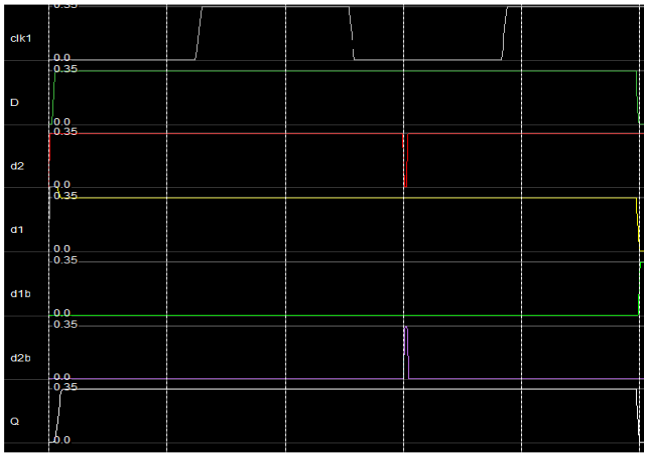

Fig.4. HLR latch simulation result with TF at d2.

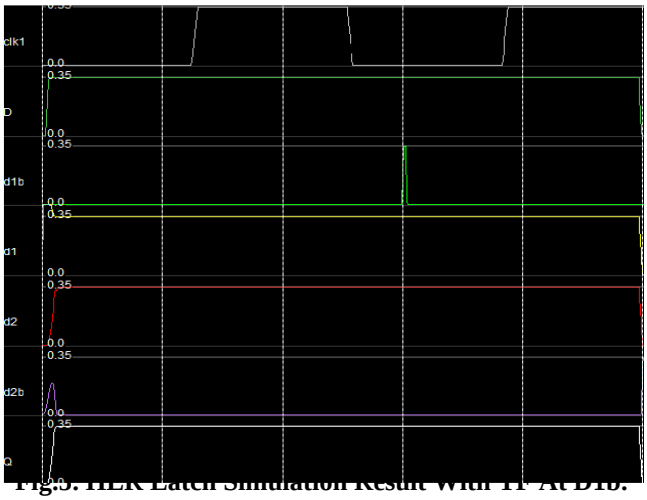

Fig.5. HLR Latch Simulation Result with TF At D1b.

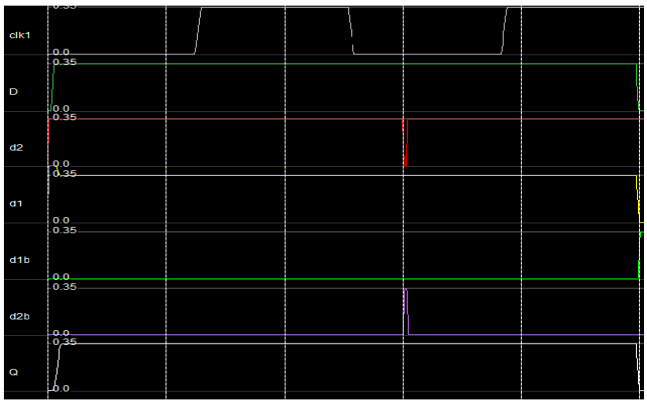

Fig.6. HLR latch simulation result with TF at d2b.

In order to reduce the dynamic power consumptions, clock signal is gated to the circuit. Here, output Q which is in high impedance state may get charged or discharged by the leakage current over the clock gated period. Thus, Soft Error may occur at the output. As it is discussed above that Transient Fault occurred at any of the internal nodes when clk = 0 that is in the latch mode, it may generate wrong logic value at the corresponding node at which TF occurred and it remains same until the succeeding clock cycle. The output stage turns OFF and Q reaches high impedance state maintaining correct logic level until the succeeding clock rises. This may not lead to an issue for HLR latch if Clock Gating is not applied because, though the leakage current rises with the scaling in the CMOS technology, the clock frequency also increases. Thus, the output stage stays in high impedance state for period of less than half clock cycle which is very short period for leakage current, that it cannot charge or discharge the output Q. In order to lessen the power consumption, if clock gating is used in the circuit, the clock signal cannot switch over a long time which is lengthier than a single clock cycle period. Here, if TF occurs at any of the internal nodes of HLR latch circuit, the output node Q will reach high impedance state for a longer time interval which is enough to charge or discharge the node due to the leakage current. Moreover, the internal node, affected by the TF cannot be corrected until the succeeding clock cycle rises. Before correcting the affected node, another node may gets affected which may result in SE at the output.

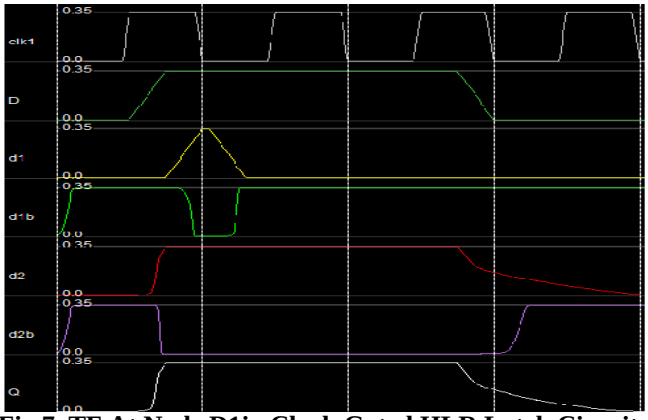

Fig.7. TF At Node D1in Clock Gated HLR Latch Circuit

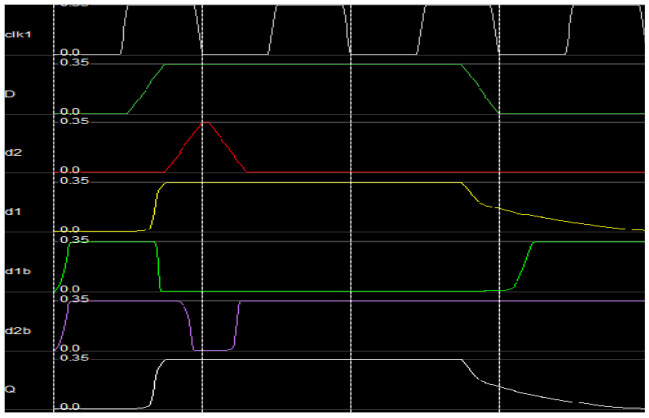

Fig.8. TF at node d2 in clock gated HLR latch circuit.

III. PROPOSED HLLR-CG LATCH AND ITS IMPLEMENTATION

Another latch which is resilient against the soft error, with high speed and reduced cost is proposed. By using this latch we can overcome the problem arose in the HLR latch as discussed above. It can be referred as the HLR-CG. In this proposed HLR-CG latch a Dual Inter-locked storage Cell (DICE) is used, which is introduced in the reference paper [11]. This DICE cell controls the input signals for output stage. The purpose of this storage cell is to tolerate the Transient Fault without depending on the size of the transistor.

The redundant signals which are produced in the DICE cell will correct the Transient Fault occurred at any of the internal nodes. This system is apt for using with clock gating system. Hence, after the Transient Fault dies down, no node will reach the high impedance state.

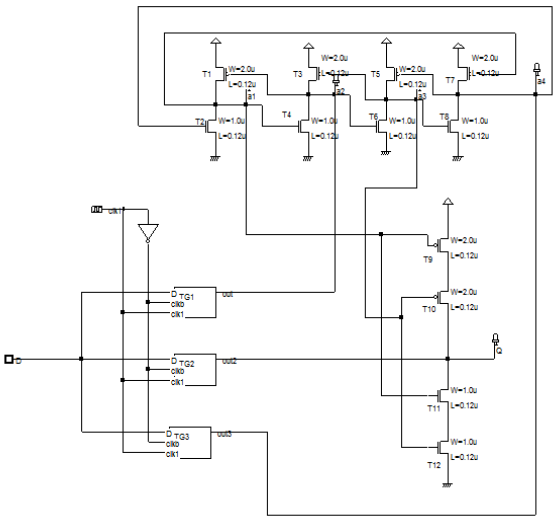

Fig.9. HLR-CG latch circuit

In HLR-CG latch the control signals for output stage are produced by utilizing this DICE cell. Here, the redundant nodes a2, a4 of the DICE cell preserve the control signals. If any incorrect logic occurred at the node a1 and node a3 will be rectified by the other nodes in the DICE cell. Thus, the voltage at output Q does not change its correct value. If Transient Fault occurs at output Q, it is rectified by input signals of output stage, since, these voltages are not affected.

When clock is high, clk1=1, The Transmission Gates TG1 to TG3 turns ON. The input D reaches output Q through the transmission gate TG2. Voltages at node a2 and node a4 are biased with voltage at input D. Consider the two scenarios: when D=1 and D=0. 1). When D is high that is D=1; nodes a2 and a4 are at '1'. Since a4=1, the node a4 of the DICE cell drives transistor T2, T2 gets ON which discharges a1 to '0' V. As a1=0, transistor T7 gets ON which confirms the voltage at node a4. Since a2=1, T6 gets ON, which discharges the voltage of a3 to '0'V. Transistor T3 turns ON, which confirms the voltage at a2, because a3=0. Therefore, when D=1; a2=a4=1; and a1=a3=0. 2). When D=0; nodes a2 and a4 are at'0'; since the node a4 =0, T5 turns ON, thus results in charging the voltage of a3 to Vdd. Since the node a3=1, transistor T8 turns ON thus it confirms the voltage at a4.since a2=0, T1 turns ON, thus results in charging the voltage of node a1 to Vdd. Transistor T4 turns ON, because of voltage at a1=1. This will confirm the voltage at a2. Thus, if D=0; a2=a4=0; a1=a3=1.When clock is low that is clk=0, the transmission gates TG1, TG2 and TG3 get turned OFF. If input D and output Q are at '1' before the changing of clock cycle, then the a1=a3=0. The transistors T9 and T10 turn ON and the transistors T11 and T12 turn OFF. Thus, the voltage at output Q is maintained at '0' through transistors T9 and T10. If the voltage at input D and output Q are '0' before the changing of clock, then a1=a3=1. Transistors T11 and T12 get turn ON T9 and T10 turn OFF. Thus the output voltage Q is maintained at 0 through T11 and T12.

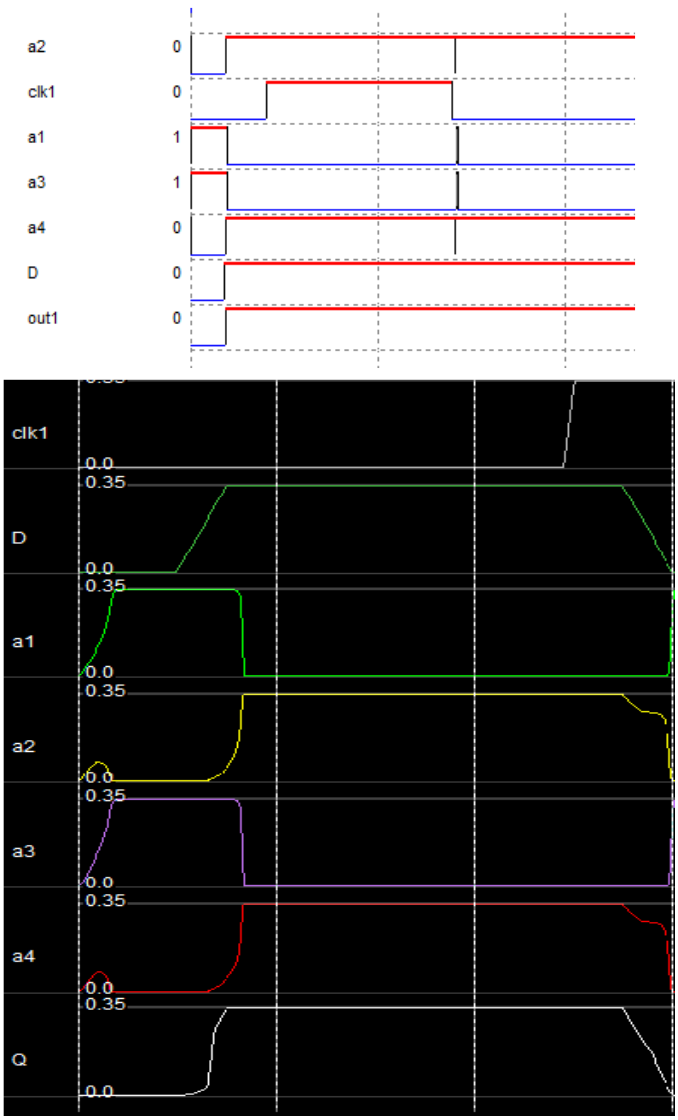

Fig.10. HLR-CG latch Simulation result without error.

When, TF occur the internal nodes a1, a2, a3 and a4 of HLR-CG latch is discussed in detail here. Figures 11 to 13 represent

the simulation results of the HLR-CG latch when TF occur at the corresponding internal nodes. Consider that TF occurs at the internal node a1. If TF occurs at internal node a1, the node a1 accurately flips to 1 which accurately turns ON the transistor T4. When this happen both the transistors T3 and T4 get turned ON. Internal node a2 gets discharged because of the stronger NMOS T4. Transistor T9 accurately turns OFF and T11 accurately turns ON. Thus, output Q is accurately in a high impedance state. The incorrect voltage level at node a2 turns OFF the transistor T6. Since, the voltage level at node a3 is '0' and it is not affected by the TF at a1. Transistor T3 still maintains ON state because of the voltage at a3. Hence, the voltage at a2 gets recovered to 1 through T3 after TF dies down. As the voltage at a4 is 1 and it is not affected by the TF at a1. Transistor T2 will be maintained in ON state because of the voltage at a4. Thus the a1 is corrected to '0'V through T2 after TF dies down.

Transistors T9 turns ON and T11 turns OFF. Output Q leaves the high impedance state and connects to Vdd through transistors T9 and T10 again.

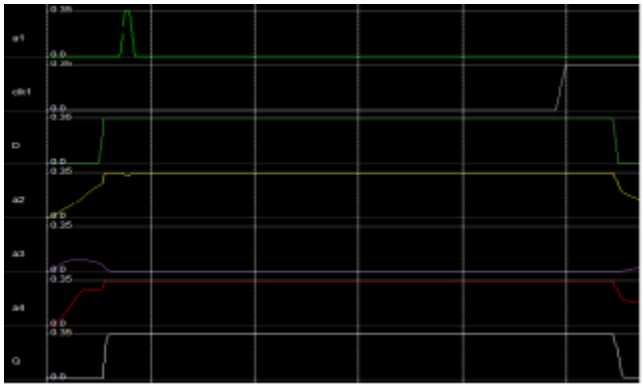

Fig.11. HLR-CG latch Simulation result when TF occurred at node a1.

Similarly when TF occurs at the internal node a2, a2 will accurately discharge to '0'V which turns the transistor T1 to ON state, both transistor T1 and transistor T2 are in ON state. The voltage at a1 is not fully charged through T1.Transistor T6 turns OFF by the incorrect voltage at a2 but voltage at a3 remains '0', which maintains the transistor T3 in ON state. Hence, voltage at a2 recovers to 1 through T3 after TF dies down.

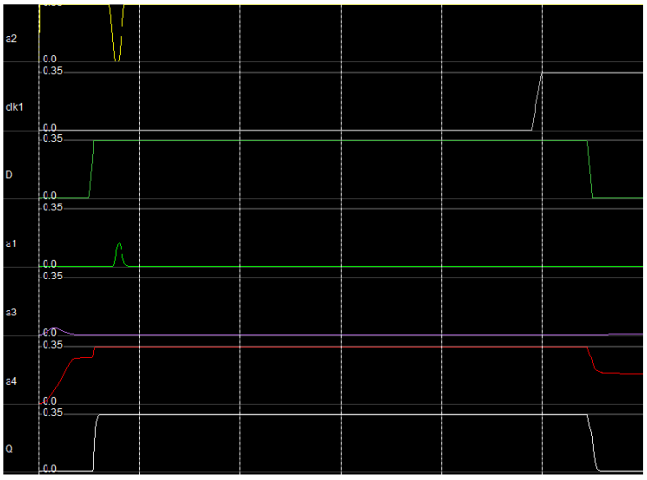

Fig.12. HLR-CG latch Simulation result when TF occurred at node a2

When TF occurs at the internal node a3 similar analysis can be applied as TF occurs at node a1 and if TF occurs at internal node a4 similar analysis can be applied as TF occurs at node a2.

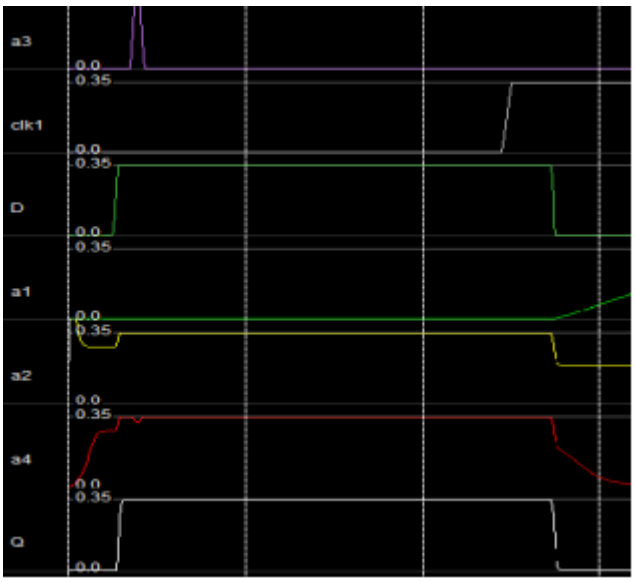

Fig.13. HLR-CG latch simulation result when TF affects nodes a3 and a4

When TF occurs at the internal nodes a1, a2, a3 and a4, at the affected node accurately changes the logic and restores to its correct logic quickly. The time required to restore the affected node depends on the particle energy, strength of the transistor which drives the affected node and capacitance node. Thus the HLR-CG latch is highly tolerant to the TF affected at any of the nodes.

IV. PROPOSED HLR-CG1 LATCH AND ITS IMPLEMENTATION:

Another latch which is robust against the TF affected at any of the internal nodes due to the radiation of alpha particles and neutrons. This latch works with high speed and low cost as well. The proposed latch is shown in the fig below. This latch is apt for applying clock gating.This circuit consists of two transmission gates TG1 and TG2. There are four stacked MOSFET blocks b1, b2, b3 and b4. The blocks b1 and b4 have two inputs and one output. The both the inputs for b1 and b4 are d1 and Q. Output of b1 is d2 and output for b4 is d3. Inputs for b2 and b3 are both d2 and d3, whereas output of b2 is Q and output of b3 is d1.

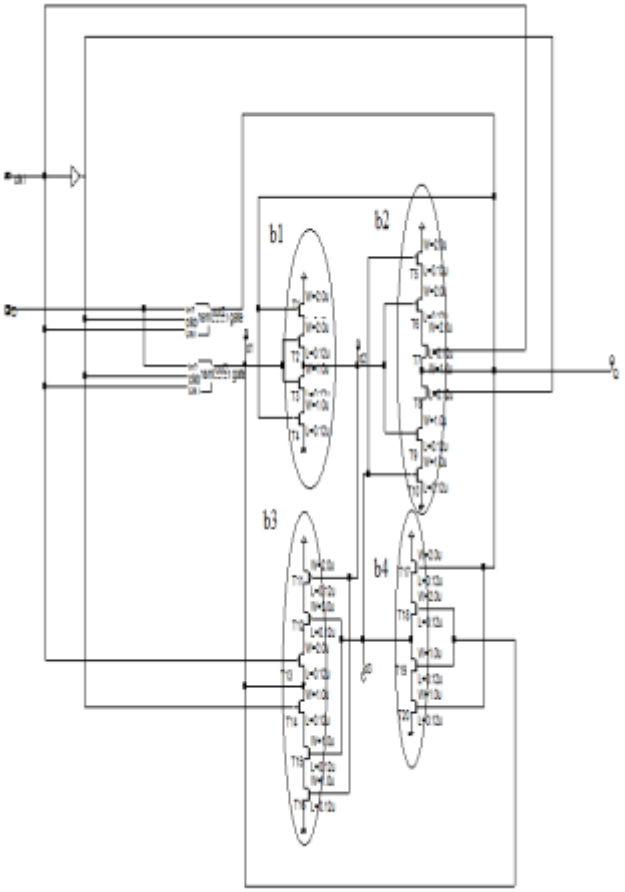

Fig.14. HLR-CG1 Latch Circuit

A detailed circuit structure of HLR-CG1 analysis is discussed below. When clock=1, the input D propagates to Q through the transmission gate TG1 and to d1 through transmission gate TG2. The MOSFET blocks b2 and b3 will get turned OFF because of the clock signal provided. This helps in preventing the contention at the output stage Q and at internal node d1. As d2 and d3 both the internal nodes are complementary to the logic level at the internal node d1 and output stage Q as well. Whereas, d1 and Q have the similar logic as D. Let us analyze, the condition when input D =1 and clk=1, Q and d1 are biased at 1. Thus, transistors T3 and T4 turn ON and the transistors T19 and T20 as well. Internal nodes d2 and d3 discharges to 0. All the internal nodes d1, d2 and d3 are biased through the transistors TG1, TG2, and blocks b1 and b4.When clk=0, transmission gate TG1 and TG2 gets turn OFF, blocks b2 and b3 turns ON. The logic value at internal node d1 is approved by the output of block, b3 and the logic value at node d2 is approved by output of block b4. Thus, the output Q is confirmed by the output of b2. Now let us consider an example below. Assume that logic at node d1 =1, at d2=0, d3=0 and at output Q=1.when clk=0, transistors T11, T12 and T13 gets turned ON, since, d2=d3=clk=0, the voltage at node d1 is preserved at 1. As d1=Q=1, transistors T3 and T4 gets turn ON, the voltage at node d2 is preserved at 0. As d2=d3=clk=0, the transistors T5, T6 and T7 gets turned ON. Then voltage at output Q is preserved at logic 1. As d1=Q=1, the transistors T19 and T20 gets turned ON, voltage at d3 is preserved at 0. Thus, all the voltages at the internal nodes are confirmed. The circuit structure is implemented in 32 nanometre technology with frequency 200 MHz at room temperature.

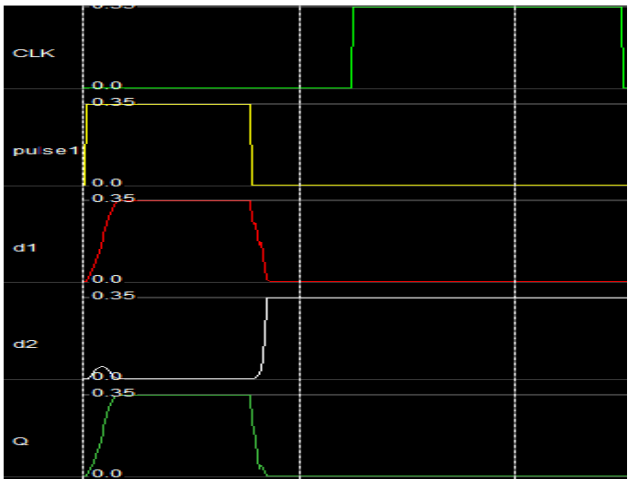

Fig.15. HLR-CG1 latch simulation result without error.

Let us analyze in detail how the latch preserves its correct logic level at output Q when a Transient Fault occurs at the internal node d1, d2 and d3 individually. Assume that, clock=0, d1=Q=1, d2=d3=0. If TF occurred at the internal node d1, d1 accurately changes to 0 and thus it accurately turns OFF the transistor T3 and turns ON transistor T2. As the voltage Q is not affected by TF, T1 maintains OFF state and T4 maintains OFF state. So, node d2 accurately enters high impedance state without changing its logic. As TF does not affect the logic at node d3, transistors T12, T11 and T13 are still maintained in ON state and thus it charges d1 to Vdd. Hence, it recovers its correct logic level. Then transistor T3 turns ON, the voltage at node d2 got confirmed and leaves the high impedance state. Thus, the Transient Fault occurred at d1 does not affect the output voltage Q.

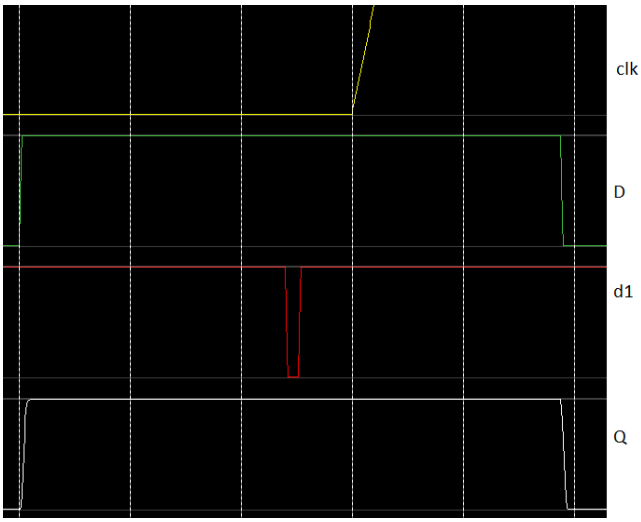

Fig.16.HLR-CG1 latch Simulation result when TF occurs at node d1.

If Transient Fault occurs at node d2, d2 accurately flips to 1 which in turn accurately turns OFF the transistor T6 and Turns ON transistor T9. As TF at does not affect the logic at node d3, transistor T10 is still in OFF state and the T5 is still in ON state. So, output Q enters the high impedance state without altering its logic level.

As TF does not affect the logic at node d1, transistors T3 and T4 will be still in ON state. This results in discharging of node d2 to '0'V and hence recovers its correct logic. Then transistor T6 gets turned ON, the voltage at Q is approved by leaving it in the high impedance state. Hence, the TF at node d2 does not affect the logic level at output Q. If Transient Fault affects the node d3, similar analysis can be extracted as at the node d2 got affected by Transient Fault.

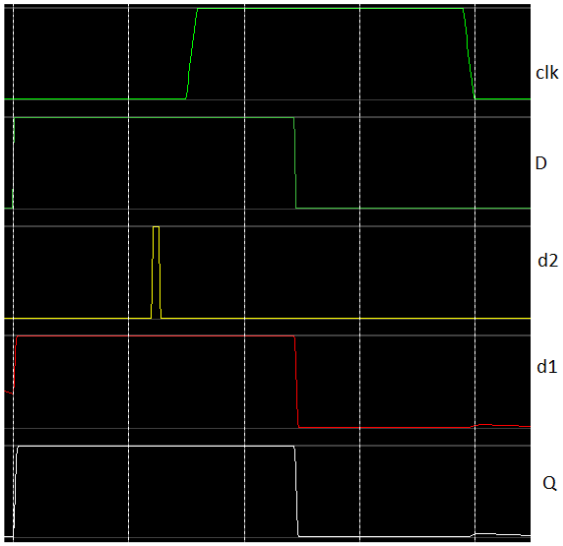

Fig.17. HLR-CG1 latch Simulation result when TF occurs at d2.

Below represented simulation results when TF the internal nodes got affected by the TF in clock gated latch, when proposed latch is in latch mode ie., clk=0 for longer time interval.

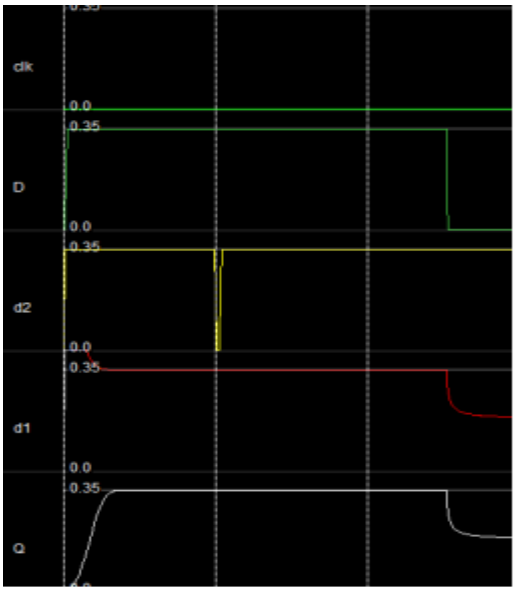

Fig.18. Simulation Of Gated HLR-CG1 Latch When TF Affects Node D2.

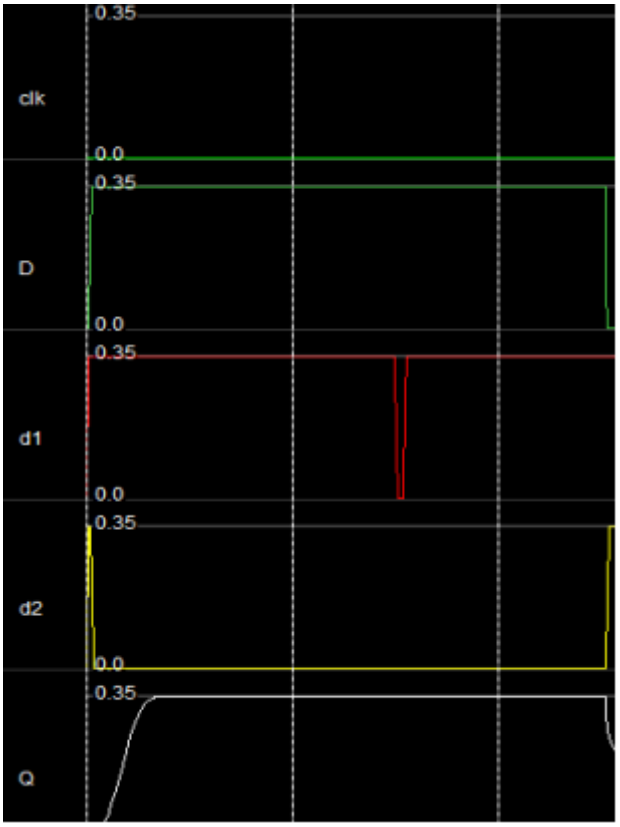

Fig.19. Simulation Of Gated HLR-CG1 Latch When TF Affects Node D1.

By observing the above results we can say that HLR-CG1 is tolerant to the TF affected at the nodes.

V. PROPOSED MODIFIED HLR-CG1 LATCH AND ITS IMPLEMENTATION

Another latch which is Robust against the transient Fault is proposed now. This circuit works similar to the HLR-CG1 latch with reduced power and reduced time delay.

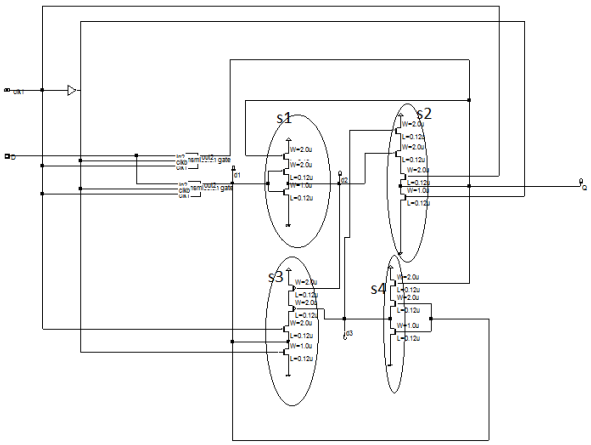

Fig.20. Modified HLR-CG1 latch circuit

A detailed circuit structure of HLR-CG1 analysis is discussed below. In this circuit M1, M2, M4, M5,M6, M8, M9, M10,

M12, and M13 are PMOS and the remaining transistors are of NMOS. When clock=1, the input D propagates to Q through the transmission gate TG1 and to d1 through transmission gate TG2. The MOSFET blocks s2 and s3 will get turned OFF because of the clock signal provided. This helps in preventing the contention at the output stage Q and at internal node d1. As d2 and d3 both the internal nodes are complementary to the logic level at the internal node d1 and output stage Q as well. Whereas,d1 and Q have the similar logic as D. Let us analyze, the condition when input D =1 and clk=1, Q and d1 are biased at 1. Thus, transistors M3 turn ON and the transistors M14 as well. Internal nodes d2 and d3 discharges to 0. All the internal nodes d1, d2 and d3 are biased through the transistors TG1, TG2, and blocks s1 and s4.

When clk=0, transmission gate TG1 and TG2 gets turn OFF, blocks s2 and s3 turns ON. The logic value at internal node d1 is approved by the output of block, s3 and the logic value at node d2 is approved by output of block s4. Thus, the output Q is confirmed by the output of s2. Now let us consider an example below. Assume that logic at node d1 =1, at d2=0, d3=0 and at output Q=1.when clk=0, transistors M8, M9 and sd1 is preserved at 1. As d1=Q=1, transistors M3 gets turn ON, the voltage at node d2 is preserved at 0. As d2=d3=clk=0, the transistors M4, M5 and M6 gets turned ON. Then voltage at output Q is preserved at logic 1. As d1=Q=1, the transistors M14 gets turned ON, voltage at d3 is preserved at 0. Thus, all the voltages at the internal nodes are confirmed. The circuit structure is implemented in 32 nanometers technology with frequency 200 MHz at room temperature.

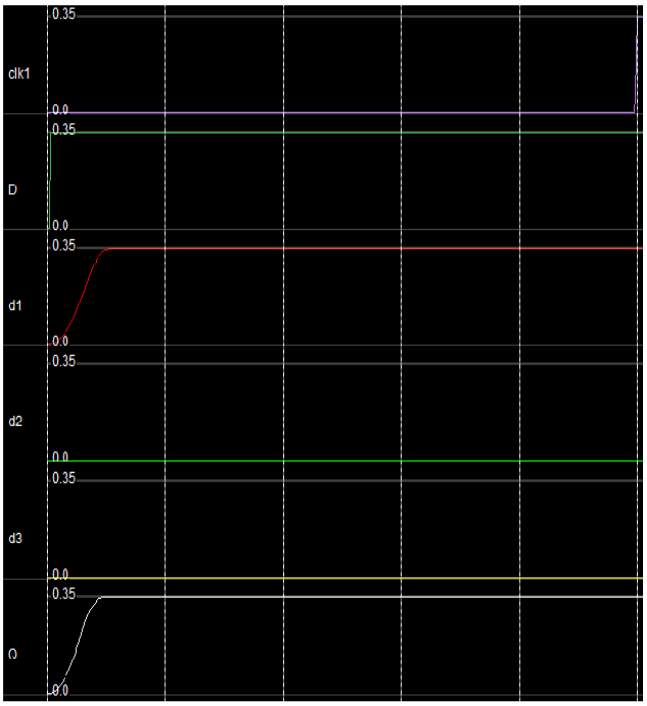

Fig.21. Modified HLR-CG1 latch simulation result without error.

Now here, we analyze in detail, how the latch preserves its correct logic level at output Q when a Transient Fault affects the internal node d1, d2 and d3 individually. Let us assume that, clock=0, d1=Q=1, d2=d3=0. If TF affects the internal node d1, d1 accurately changes to 0 and thus it accurately turns OFF the transistor M3 and turns ON transistor M2. As the voltage Q is not affected by TF, M1 maintains OFF state. So, node d2 accurately enters high impedance state without changing its logic. As TF does not affect the logic at node d3, transistors M9, M8 and M10 are still maintained in ON state and thus it charges d1 to Vdd. Hence, it recovers its correct logic level. Then transistor M3 turns ON, the voltage at node d2 got confirmed and leaves the high impedance state. Thus, the Transient Fault occurred at d1 does not affect the output voltage Q.

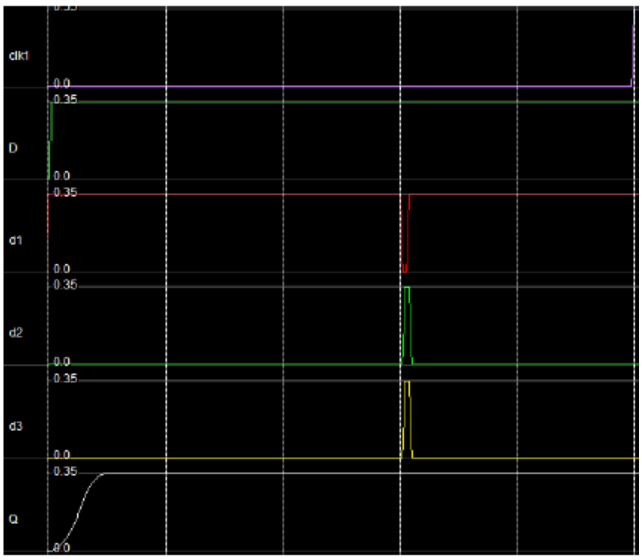

Fig.22. Simulation result of modified HLR-CG1 when TF affects the different nodes d1, d2, and d3.

If Transient Fault affects node d2, d2 accurately changes to 1 which in turn temperately turns OFF the transistor M5. As TF at does not affect the logic at node d3, transistor M4 is still in ON state. So, output Q enters the high impedance state without altering its logic level. As TF does not affect the logic at node d1, transistors M3 will be still in ON state. This results in discharging of node d2 to '0'V and hence recovers its correct logic. Then transistor M5 gets turned ON, the voltage at Q is approved by leaving it in the high impedance state. Hence, the TF at node d2 does not affect the logic level at output Q. If Transient Fault affects the node d3, similar analysis can be extracted as at the node d3 got affected by Transient Fault.Similarly, If Transient Fault occurred at node d2, d2 accurately changes to 1 which will turn OFF the transistor M5accurately. As TF at does not affect the logic at node d3, transistor M4 is still in ON state. So, output Q enters the high impedance state without altering its logic level. As TF does not affect the logic at node d1, transistors M3 will be still in ON state. This results in discharging of node d2 to '0'V and hence recovers its correct logic. Then transistor M5 gets turned ON,

the voltage at Q is approved by leaving it in the high impedance state. Hence, the TF at node d2 does not affect the logic level at output Q. If Transient Fault affects the node d3, similar analysis can be extracted as at the node d3 got affected by Transient Fault.

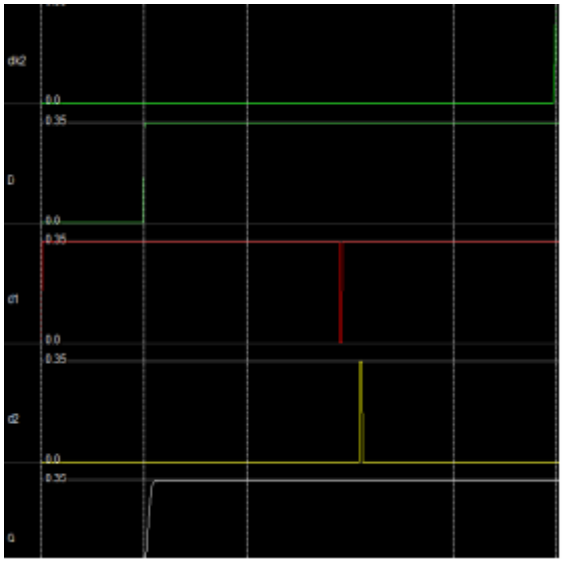

Fig 23: when TF occurs at nodes d1 and d2 of the gated modified HLR-CG1

VI. EVALUATION

In this section the proposed latch designs are compared with the previously proposed design that is split internal node highly resilient latch. The comparison is about the cost and power.The tabular column represented below shows the evaluation of power, area and delay of the split internal node highly robust latch (SINHR) [2] and the three proposed latches in 45 nanometre technology.

TABLE I

Latch	Area	Power	Delay	PDP (j)
SINHR	46um^2	0.232uw	12ps	2.70E-18
HLR	94.6um^2	0.527uw	9ps	4.74E-18
HLR-CG	81.7um^2	0.838uw	9ps	7.50E-18
HLR-CG1	97.3um^2	0.221uw	13ps	2.80E-18
Modified HLR-CG1	75.3um^2	0.221uw	10ps	2.21se-18

Comparison table of the proposed latches in 45 nm technology

By considering the below given table we can estimate the power, area and delay of the SINHR latch and the three proposed latches when implemented in 32 nanometer technology.

TABLE II

Latch	Area	Power	Delay	PDP (j)
SINHR	29.5um^2	0.218uw	11ps	2.39E-18
HLR	60.5um^2	0.452uw	8ps	3.62E-18
HLR-CG	52.3um^2	0.586uw	8ps	4.60E-18
HLR-CG1	62.4um^2	0.213uw	12ps	2.54E-18
Modified HLR-CG1	48.3um^2	0.19uw	9ps	1.90E-18

Comparison table of the proposed latches in 32 nm technology

VII. CONCLUSION

In this paper, four types of latches are proposed those are more susceptible to the Transient Faults at the internal nodes. The technique SINHR latch discussed before only mitigate the soft error effect and their designs still suffer functionality fail due to TF caused by high energy particles and not all the internal nodes are protected. Whereas, these proposed latches work with high speed and reduced cost. The first one is a HLR latch which is vulnerable to Transient Fault at the internal nodes regardless of the energy of the hitting particles. However, when clock gated system is used to reduce power consumption in HLR, the internal node got affected by the TF at any internal node, results in SE which output node is left in high impedance state. Thus, it results in leakage current. In order to overcome this issue three other latches HLR-CG, HLR-CG1 and modified HLR-CG1 which are immune to Soft Error are proposed. These latches can be used with the clock gating system. The performance of these latches can be estimated by considering the area, power, and propagation delay. The Modified HLR-CG1 is with Power Delay Product (PDP) and area when compared.

REFERENCES

1. High Performance, Low Cost, and Robust Soft Error Tolerant Latch Designs for sscale CMOS Technology Haiqing Nan and Ken Choi, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, VOL. 59, NO. 7, JULY 2012
2. M. Omana, D. Rossi, and C. Metra, “Latch susceptibility to transient faults and new hardening approach,” IEEE Trans. Comput., vol. 56, no. 9, pp. 1255–1268, Sep. 2007
3. C. M. Hsieh, P. C. Murley, and R. R. O’Brien, “Collection of charge from alpha-particle tracks in silicon devices,” IEEE Trans. Electron Devices, vol. 30, no. 6, pp. 686–693, Jun. 1983.
4. L. Lantz, “Soft errors induced by alpha particles,” IEEE Trans. Rel., vol. 45, no. 2, pp. 174–179, Dec. 1996.
5. R. C. Baumann, “Soft errors in advanced semiconductor devices—Part I: The three radiation sources,” IEEE Trans. Device Mater. Rel., vol. 1, no. 1, pp. 17–22, Mar. 2001.
6. P. E. Dodd and L. W. Massengill, “Basic mechanisms and modeling of single-event upset in digital microelectronics,” IEEE Trans. Nucl. Sci., vol. 50, no. 3, pp. 583–602, Jun. 2003.
7. N. Miskov-Zivanov and D. Marculescu, “A systematic approach to modeling and analysis of transient faults in logic circuits,” in Proc. IEEE Int. Symp. Quality Electron. Design (ISQED’09), pp. 408–413.
8. S. Gangadhar, M. Skoufis, and S. Tragoudas, “Propagation of transients along sensitizable paths,” in Proc. IEEE Int. On-Line Test. Symp., 2008, pp. 129–134.
9. sN. Seifert, B. Gill, V. Zia, M. Zhang, and V. Ambrose, “On the scalability of redundancy based SER mitigation schemes,” in Proc. IEEE Int. Conf. Integr. Circuit Design Technol. (ICICDT), 2007, pp. 1–9.
10. T. Calin, M. Nicolaidis, and R. Velazco, “Upset hardened memory design for submicron CMOS technology,” IEEE Trans. Nucl. Sci., vol. 43, no. 6, pp. 2874–2878, Dec. 1996.
11. M. Nicolaidis, R. Perez, and D. Alexandrescu, “Low-cost highly-robust hardened cells using blocking feedback transistors,” in Proc. IEEE VLSI Test Symp., 2008, pp. 371–376.
12. H. K. Alidash, S. M. Sayedi, H. Saidi, and V. G. Oklobdzija, “Soft error filtered and hardened latch,” in Proc. IEEE 8th Int. Conf. ASIC, 2009, pp. 613–616.

13. S. Lin, Y. B. Kim, and F. Lombardi, "Soft-error hardening designs of nanoscale CMOS latches," in Proc. IEEE Very Large Scale Integr. (VLSI) Test Symp., 2009, pp. 41–46.
14. T. Karnik, S. Vangal, V. Veeramachaneni, P. Hazucha, V. Erraguntla, and S. Borkar, "Selective node engineering for chip-level soft error rate improvement," in Proc. Symp. Very Large Scale Integr. (VLSI) Circuits Dig. Tech. Papers, 2002, pp. 204–205.
15. M. Omana, D. Rossi, and C. Metra, "High-performance robust latches," IEEE Trans. Comput., vol. 59, no. 11, pp. 1455–1465, 2010.
16. M. Fazeli, A. Patooghy, S.G. Miremadi and A.Ejlali, "feedback redundancy : A power aware efficient SEU tolerant latch design for submicron technologies" in proc.ieee/ifip int.conf. dependable system.netw.,jun2007, pp 276 to 285.

AUTHORS PROFILE

Author-1

Dr.J.Sofia Priya dharshini was awarded doctorate from JNTUA ,Anantapuram, She did her PG in RGMCET under JNTUA and B.Tech in GPREC, Kurnool from SK University. Her areas of interest are communications, VLSI and Image processing. She has more than 14 years of teaching and research experience. She published more than 20 papers in various International and national journals and conferences. At present, she is working as associate professor in RGMCET, Nandyal and is member of IE.

Author-2

B.Shirisha did her B.Tech in Intel engineering college, Anantapuramu, under JNTUA. At Present she is pursuing M.Tech from RGMCET, Nandyal,AP.