International Journal of Engineering and Advanced Technology (IJEAT)
ISSN: 2249-8958 (Online), Volume-8 Issue-6, August, 2019

Bulk Junctionless Transistor (JLT) with non-uniform doping: A high performance and scalable device

Dipak Kumar Singh, Priyanka Mondal, M. W. Akram

Abstract*: In this paper we have presented the non-uniformly doped bulk Junctionless transistor (JLT) and investigated bulk-JLT and SOI-JLT with non-uniform doping in terms of its electrical performance parameters and short channel effects (SCEs) parameters comparatively. Effective thickness of channel depends on non-uniform doping distribution parameters and this affects the performance of bulk-JLT notably, however it is not so in case of SOI-JLT. The effect of non-uniform doping on electrical characteristics of JLTs (bulk and SOI) in terms of Subthreshold Slope (SS), ON-current, OFF-Current and ON/OFF current ratio has been investigated, and the non-uniformly doped bulk-JLT exhibits high ON/OFF ratio (10^9 for 20 nm Gate Length). Moreover, the non-uniformly doped bulk-JLT also shows improved short-channel effects (SCEs) parameters (such as Drain Induced Barrier Lowering, Threshold Voltage variations etc.) compared to SOI-JLT. Lastly, the effect of standard deviation, dielectric constant, substrate doping, and well biasing on the device performance are examined to further improve the performance of bulk-JLT independently.

***Index Terms*: Bulk-JLT, Non-Uniform (NU) Doping, SOI-JLT.**

I. INTRODUCTION

The introduction of various device architectures namely (FinFET and gate all around (GAA) etc.) and new material system (such as fully depleted silicon-on-insulator) leads to better controllability of channel of the scaled devices. Multi-gate devices provide the better control of mobile charge carriers in the channel, and hence short channel effects (SCEs) are alleviated substantially. However further scaling of devices to the sub-micron regime puts stringent condition to form ultra-steep impurity profile at junctions (source-channel and drain-channel) and also require higher thermal budget [1]. Recently a device named junctionless FET (JLFET) has been presented as future device which has simpler fabrication process as no doping concentration gradient between channel and source/drain is required [2-5]. To turn the JL-SOI devices OFF completely, either a narrow channel width or uniform ultrathin channel required however fabrication of JL-SOI devices are technologically difficult and expansive. The self-heating effects arise from its buried oxide in JL-SOI device reduces the ON-state performance whereas JL-Bulk devices have better scalability and improved immunity towards SCEs [6-8]. Also in JL-Bulk devices, its performance can be improved by optimizing additional parameter like substrate doping and substrate bias. Non-uniformly (NU) doped JL devices have shown improved SCEs and subthreshold behaviors over the uniformly doped JL devices, as reported in various literatures. In 2013, Mondal *et al*. [9] reported that non-uniform (Gaussian) doping in channel vertical direction can be used to improve ON to OFF current sratio and suppress short channel behavior. Also, Bal *et al*. [10] demonstrated that laterally graded double gate (DG)-JLT have better I_{ON}/I_{OFF} ratio than uniformly doped its counterpart. Step doping profile has been used in Multigate JLTs for better scalability and improved SCE immunity as suggested by Song and Li [11]. Further vertical doping profile has been used in SOI-JL FinFET in his extended work to enhance sub-threshold behavior [12]. Recently, Singh *et al*. [13] demonstrated numerically that Gaussian-like function (in place of Gaussian doping profile) in DG-JLT can be used for optimization of subthreshold characteristics. By employing Gaussian-like doping (maximum and minimum at gate surfaces) in DG-JLT as demonstrated recently in Ferhati *et al*. [14], the self-heating effect can be suppressed. In 2017, Ferhati *et al*. [15] demonstrated that graded channel doped JL MOSFET can be used for high performance and ultralow power application.

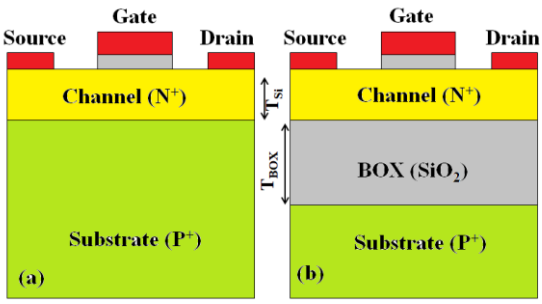


Figure 1. Schematic structure of (a) Bulk-JLT and (b) SOI-JLT

Revised Manuscript Received on October 30, 2019.

* Correspondence Author

Dipak Kumar Singh*, Department of Electronics and Communication Engineering, National Institute of Technology, Patna, India.

Priyanka Mondal, Department of Electronics and Communication Engineering, National Institute of Technology, Patna, India.

M. W. Akram, Department of Electronics and Communication Engineering, F/O Engineering and Technology, Jamia Millia Islamia, New Delhi, India.

The numerical investigation of non-uniformly doped DG-JLT shows that Leakage current and SCEs can be improved (reduced) by optimized non-uniform doping profile parameters, as shown in Vandana

TABLE 1

Parameter	SOI-JLT	Bulk-JLT
Effective oxide thickness (T_{OX})	1 nm	1 nm
Device layer/channel thickness /Device Width (T_{si})	6-10 nm	6-10 nm
Gate length (L_g)	20-60 nm	20-60
Source/channel/drain doping (N_d), Peak Concentration (N_0)	N type $1.5\times10^{19}cm^{-3}$	N type $1.5\times10^{19}cm^{-3}$
Substrate doping (N_{sub})	-	P-Type $1.5\times10^{18}cm^{-3}$
Gate Workfunction ($ø_m$)	5.1 eV	5.1 eV
Supply voltage (V_{DD})	1V	1V

et al. [12]. Recently a Gaussian Channel (GC) JL FinFET proposed with optimized parameter for future digital and analog application [17]. All of the above works of non-uniformly doped JLT are based on the SOI technology. In this work we have explored the non-uniformly doped Bulk Junctionless Transistor. Electrical performance of bulk-JLT is compared with SOI-JLT with uniform and non-uniform doping. Also performance of NU doped bulk-JLT has been estimated on the basis of parameters (gate oxide thickness, gate dielectric constant, gate length, standard deviation of Gaussian doping profile, well biasing as well doping).

II. DEVICE STRUCTURE

Fig. 1 shows simulated structures of SOI-JLT and bulk JLT using Sentaurus TCAD [18]. Both devices have same device dimensions as given in Table 1 except buried oxide thickness (T_{BOX}) in SOI-JLT. The basic principle behind JL device is a uniformly doped channel having high doping without any metallurgical junction. In our simulation we have taken non-uniform doping profile, where maximum concentration is

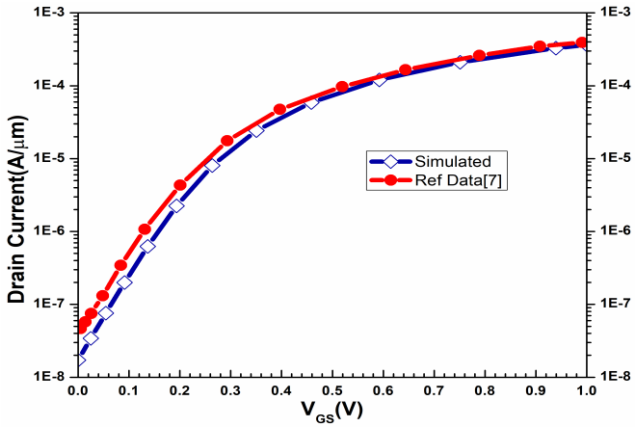


Figure 2. Calibration of models with refrence data (SOI-JLT)

considered at the interface between gate oxide and channel and concentration decreases gradually (Gaussian distribution) across the channel thickness and reaches its minimum value at channel-BOX/substrate interface. Practically non-uniform doping in the channel is feasible; it can be implanted by proper control of impurities dose and energy of ion-implantation. The impurity doping distribution model in the device channel is Gaussian-like for our simulation, and is specified by equation Eq. (1). In this equation, N_D (y) represents the doping concentration in vertical direction (y-axis), σ stands for standard deviation, and N_0 denotes the extreme value of doped quantities at its mean position μ. In our simulation μ changes from 3 nm to 6 nm across device thickness. The extreme value of non-uniform doping is chosen as equal as uniform doping concentration (1.5×10^{19} cm^{-3}).

$$N_D(y) = N_0 \exp\left[-\frac{(y-\mu)^2}{2\sigma^2}\right] \quad (1)$$

III. RESULT AND DISCUSSION

This section comprises detail discussion of electrical characteristics of non-uniformly doped JLTs and parametric variation. Our main motivation to use non-uniform doping (Gaussian doping) in bulk-JLT is to achieve better electrical characteristics. The non-uniformly doped JL device has similar operation as uniformly doped JL device, as the SOI-JL with non-uniform doping and its improved characteristics shown in [9]. Here we have studied the effect of non-uniform doping on bulk JLT.

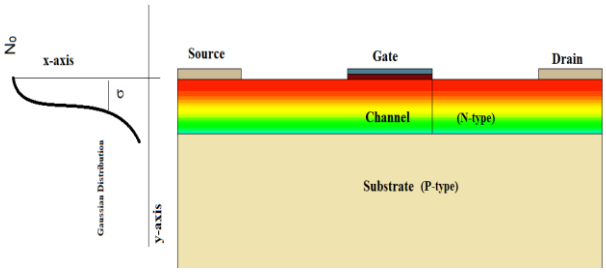


Figure 3. Gaussian doping distribution function and electron-density variation across the Silicon-channel of bulk-JLT/SOI-JLT

A. Comparison between the NU Doped JLTs (Bulk and SOI)

The transfer characteristics of JLTs (bulk and SOI) with uniform and NU doping are plotted in Fig 4. As in bulk-JLT substrate-channel junction develops a depletion region which reduces effective channel thickness and provide more control of gate than SOI-JLT. Non-uniform doping in both SOI-JLT and bulk JLT further improve the gate controllability as carrier concentration decreases from top of gate/channel interface to BOX/substrate interface. Due to non-uniform doping, OFF state current is reduced substantially (order of 10^4) in comparison to ON-state current in both JLTs (bulk and SOI).

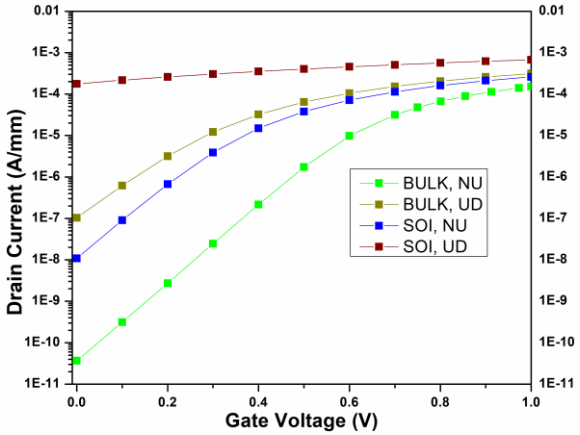


Figure 4. IDS-VGS characteristics of JLTs (Bulk and SOI) with uniform and NU doping (VDS= 1V, VGS= 1V, Gate Length = 20 nm, Thickness of Channel = 10 nm)

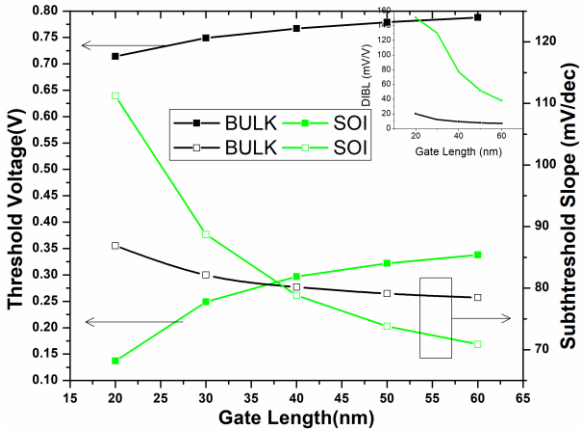


Figure 6. Variation of Threshold Voltage, Subthreshold Slope and DIBL (inset) against variation of Gate length (TOX=1 nm, VDS = 1 V, VGS= 1V, Thickness of Channel = 10 nm, SD = 3 nm)

i. Impact of Gate Length Variation on Device Performance

The scaling behavior of non-uniformly doped JLTs (bulk and SOI based) are shown in Fig 5. Bulk JLT with non-uniform doping has improved ON to OFF current ratio (10^9-10^{11}) than non-uniformly doped SOI-JLT (10^2-10^7) as similar to bulk-JLT with uniform doping has better short channel characteristics.

Fig. 6 shows the deviation of threshold voltage, subthreshold slope (SS) and DIBL with gate length scaling. The controlling of channel by gate voltage decreases as channel length reduces means it requires smaller gate voltage to deplete the charge under the gate. So with decrease in gate length, threshold voltage also decreases. While increase in gate length results improved (reduced) subthreshold slope. Here, the change in SS, threshold voltage and DIBL against the varying gate length is smooth in bulk-JLT (10 % for 20-60 nm GL) compared to SOI-JLT (> 57 % for 20-60 nm GL).

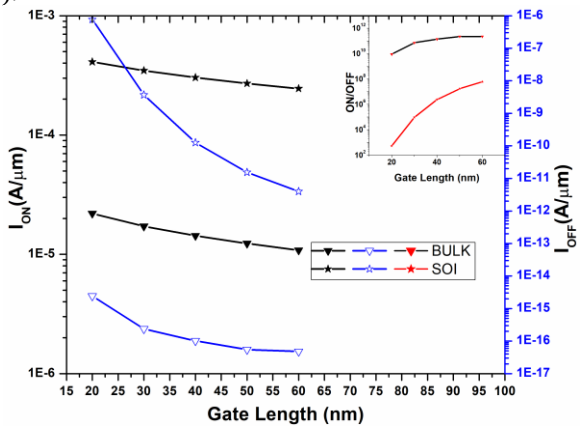
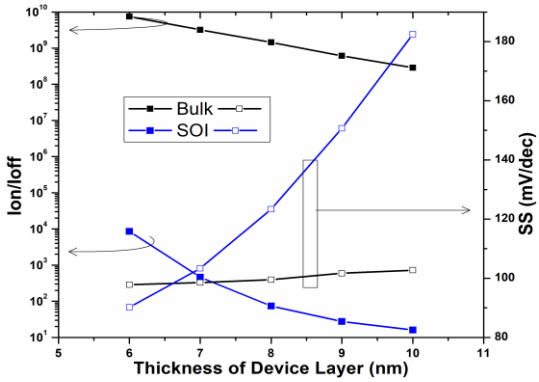


Figure 5. ON-Current and OFF-Current of both JLTs (NU doped bulk-JLT and SOI-JLT) for Gate length for 20 nm to 60 nm (Inset) ON/OFF current ratio of both JLTs against Gate length 20 nm to 60 nm, Thickness of Channel = 10 nm, SD = 3 nm

ii. Impact of Channel Thickness Variation on Device Performance

The effect of scaling of device layer thickness on subthreshold slope (SS) and ON-to-OFF current ratio is plotted in Fig 7. Here non-uniformly doped bulk-JLT and SOI-JLT with thin device layer have higher ON-to-OFF-current ratio. However, JLTs having thick device layer show reduced ON/OFF current ratio, also in bulk-JLT extra depletion due to channel/substrate junction further reduces OFF-state current, hence large ON/OFF current ratio. Here variation of ON/OFF current ratio in SOI-JLT is more compared to bulk-JLT with increasing channel thickness. Also subthreshold slope decreases with decrease in device layer thickness in both bulk-JLT and SOI-JLT but variation of SS with increasing device layer thickness in SOI-JLT is rapid compared to bulk-JLT as the effective device thickness of bulk-JLT is less.



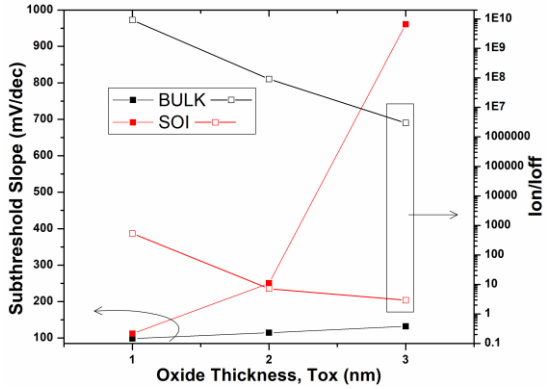
i. Figure 7. ON to OFF current ratio and SS versus thickness of Channel (TSi) with Gate length = 20 nm, TOX=1 nm, VDS

ii. Impact of Oxide Thickness Variation on Device Performance

iii. = 1 V, VGS= 1 V, SD = 4 nm

As the gate capacitance - which depend on oxide capacitance C_{OX} in conventional MOSFET, rely on gate oxide thickness T_{OX}. As we increase oxide thickness T_{OX}, current in conventional MOSFET changes inversely and it affects the subthreshold slope and ON state current.

For non-uniformly doped bulk-JLT and SOI-JLT, it is observed that from Fig. 8 ON to OFF current ratio and subthreshold slope changes as we vary oxide thickness (1 nm to 3 nm). Here ON/OFF current ratio reduces with increase in gate oxide thickness. Also subthreshold slope is deteriorated (increased) with increase in gate oxide thickness T_{OX}. As in Fig 8, non-uniformly doped bulk-JLT with oxide thickness (T_{OX} =1 nm) has ON/OFF current ratio 9.089×10^{9} while bulk-JLT with oxide thickness (T_{OX} =3 nm) has degraded ON/OFF current ratio 2.957×10^{6}. In the case of SOI-JLT ON/OFF current ratio also decreased however it has very poor ON/OFF current ratio. With increasing oxide thickness subthreshold slope is increasing but SS of NU (Gaussian) doped SOI-JLT degraded more than its bulk counterpart.

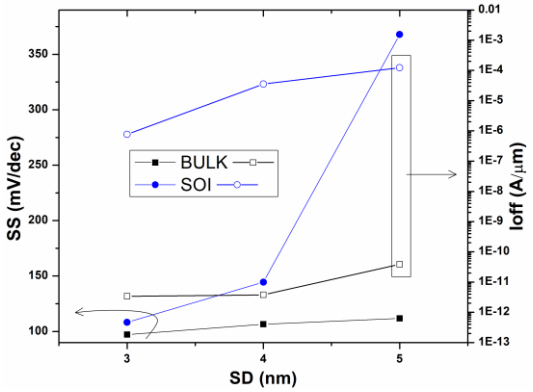


i.

ii. **Figure 8. Variation of Subthreshold Slope and OFF-current against variation of Oxide Thickness (T_{OX}) (Gate length = 20nm, V_{DS}= 1 V, V_{GS}= 1V, Thickness of Channel = 10 nm, SD = 3nm)**

iii. ffect of Standard Deviation Variation on Device Performance

The subthreshold behavior of devices (SOI-JLT & bulk-JLT with NU doping) can be improved by optimizing non-uniform (Gaussian) doping distribution variables. As in Fig. 9, SS and OFF-state current are plotted against standard deviation (**σ**) of Gaussian doping profile. The SS and OFF-state current deteriorated for large value of SD (as more carriers in channel). It also noted that subthreshold slope in SOI-JLT is increasing rapidly compared to non-uniformly doped bulk-JLT.



i. Figure 9. Variation Subthreshold Slope and OFF current against variation of standard deviation (SD) (T_{OX}=1 nm, V_{DS} $ = 1 V, V_{GS}= 1V, Thickness of Channel = 10 nm, Gate length = 20 nm)

B. Effect of device parameters variation on the Electrical Performance of Non-Uniformly Doped Bulk-JLT

i. Impact of Device thickness

The behavior of NU doped bulk-JLT is observed as the effective device layer of bulk-JLT varies with doping (here Gaussian non-uniform doping with different standard deviation). Fig.10 shows change in threshold voltage and subthreshold slope with device layer thickness. It is noticed that with widen in channel thickness (6 nm- 10 nm) controlling of gate decreases. So JLT which have thin channel gives better subthreshold slope (SS). On the other hand, threshold voltage decreases with increase in device layer thickness as thick channel has large numbers of carriers compared to thin channel. It means a less voltage is required to turn on the device. It can be tune by choosing appropriate NU-doping (Gaussian) distribution profile. As shown in Fig. 10, with the change in shape of non-uniform doping profile (standard deviation, σ) in bulk-JLT, we can improve its subthreshold behavior. For lower value of SD (σ), bulk-JLT has improved subthreshold slope while larger SD (σ) gives better (lower) threshold voltage.Fig.11 shows variation in ON-to-OFF current ratio and Drain-induced barrier lowering (DIBL) with device layer thickness. It is noticed that with increase in channel thickness (6 nm- 10 nm) ON-to-OFF current ratio decreases. ON current as well OFF current increases with increase in device layer thickness however rate of increase OFF current is more than that of ON current. It means ON/OFF current ratio decreases with increased channel thickness. Variation of DIBL against the change in device layer thickness suggests that the decrease in channel thickness reduces DIBL. Also, ON/OFF current ratio and DIBL can adjusted to appropriate value by selecting different non-uniform doping distribution (standard deviation, σ), as shown in Fig 11.

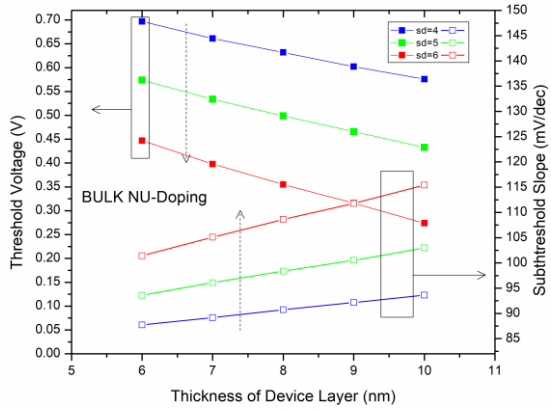


Figure 10. Subthreshold slope and threshold voltage versus Channel Thickness (T_{Si}) with Gate length = 20 nm, T_{OX}=1 nm, V_{DS} = 1 V, V_{GS}= 1

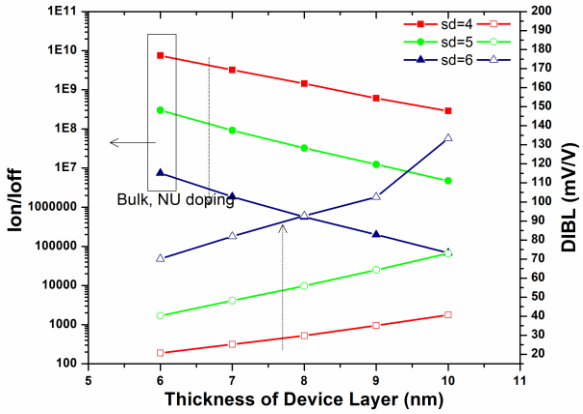


Figure 11. ON to OFF current ratio and DIBL versus Channel Thickness (T_{Si}) with Gate length = 20 nm, T_{OX}=1 nm, V_{DS} = 1 V, V_{GS}= 1V

ii. Effect of Dielectric Constant Variation on Device Performance

In our numerical simulation we have used different dielectric (K= 3.9, 7.5, 25) to study its effect on drain characteristics and ON/OFF current ratio of non-uniformly doped bulk-JLT. From Fig. 12 it is noticed that OFF state current reduces when dielectric constant increases whereas ON state current remains same. As dielectric constant (K) changes, Effective oxide thickness also changes which in turn reduce gate leakage current and tunneling substantially. By changing K, the controllability of gate over the channel can be improved. Also from Fig. 13 we can see that OFF state current and ON-to-OFF current ratio improves as dielectric constant (K) increases. For dielectric constant (K= 3.9) ON/OFF current ratio is 4.093×10^{6} while for K=25 it is 7.596×10^{9}.

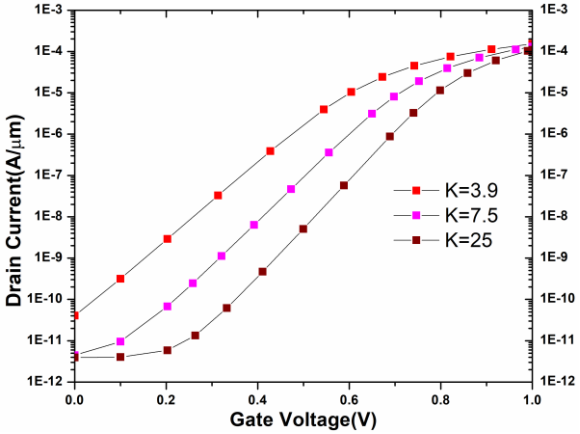


Figure 12. IDS-VGS characteristics of bulk-JLT with NU doping for various Dielectric constant (K) (VDS= 1V, VGS= 1V, Gate Length = 20 nm, Thickness of Channel = 10 nm)

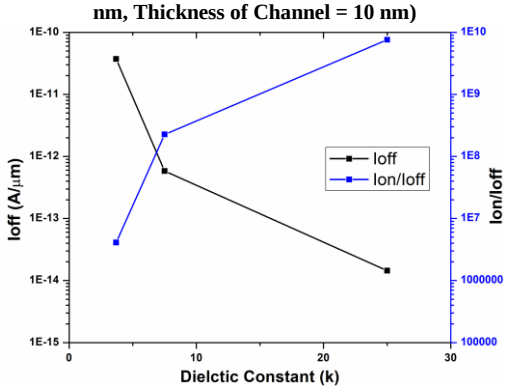


Figure 13. ON and OFF current versus variation of Dielectric constant (K) in bulk-JLT (T_{OX} =1 nm, V_{DS} = 1 V, V_{GS}= 1V)

iii. Effect of Substrate Doping Variation on Device Performance

Device thickness layer is reduced effectively due to depletion of carriers at substrate-channel junction. So, effective thickness of device layer can be controlled by substrate bias and substrate doping. In Fig. 14 it also observed that ON and OFF current decreases with increase in well doping concentration however OFF-state current decreases sharply (channel thickness deplete more with higher well doping) than ON-state current. Also in Fig.15 variation of threshold voltage and subthreshold slope (SS) are plotted against substrate doping. With increase in substrate doping effective thickness of device layer decreases, so, subthreshold slope of bulk-JLT improves (reduces) while threshold voltage increases.

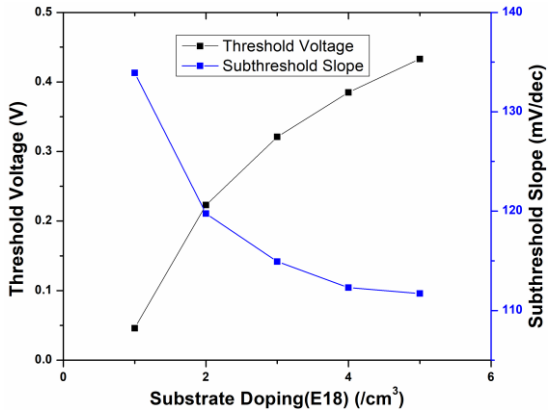


Figure 15. Variation of Threshold Voltage and Subthreshold Slope against variation of Substrate doping (Gate length =20 nm, T_{OX}=1 nm, V_{DS} = 1 V, V_{GS}= 1V)

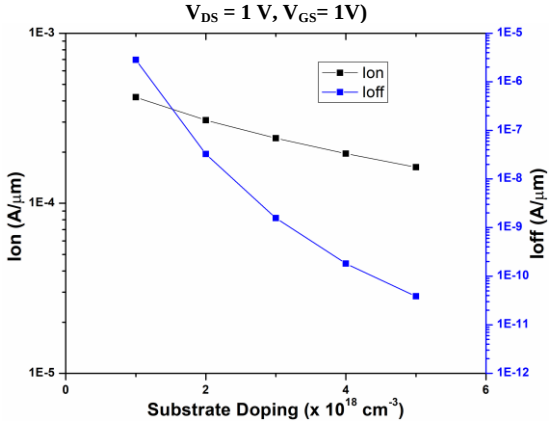


Figure 14. ON and OFF current versus variation of Substrate doping (T_{OX}=1 nm, V_{DS} = 1 V, V_{GS}= 1V)

iv. Effect of Substrate Bias Variation on Device Performance

By varying substrate voltage (well biasing) the electrical performance of non-uniformly doped bulk-JLT can be tuned. The results obtained from our simulation, as shown in Fig 16 and Fig. 17, shows the variability of parameters (I_{ON}, I_{OFF}, SS and threshold voltage) against the variation of substrate bias. From Fig. 16 it also observed that ON and OFF current decreases with decrease in substrate voltage however OFF-state current decreases sharply than ON-state current.
Variation of subthreshold slope and threshold voltage are plotted in Fig. 17. It is observed that with decrease in substrate voltage subthreshold slope gets better (decreases) and threshold voltage increases.

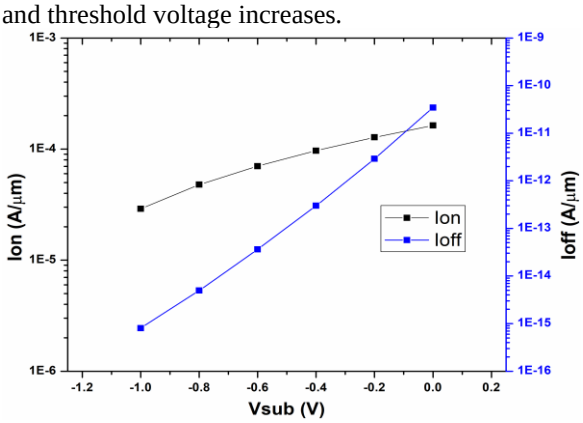


Figure 16. ON and OFF current versus variation of Substrate voltage (T_{OX}=1 nm, V_{DS} = 1 V, V_{GS}= 1V)

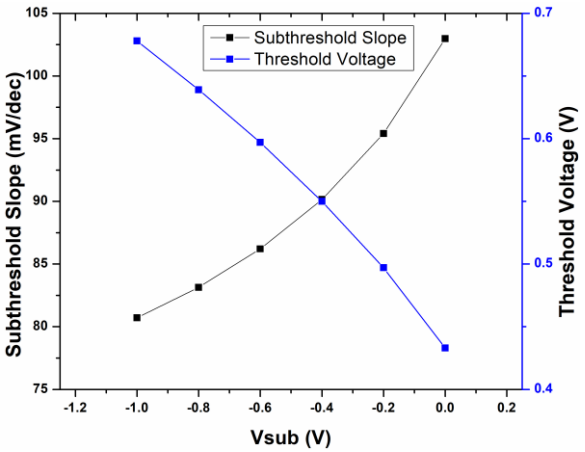


Figure 17. Variation of Subthreshold slope and Threshold voltage against variation of Substrate voltage (Gate length = 20 nm, V_{DS} = 1 V, V_{GS}= 1V)

IV. CONCLUSION

In this paper we engineered channel doping (Gaussian Doping) of JLTs to explore its electrical characteristics numerically. It is shown that non-uniformly doped bulk-JLT has improved electrical behavior (such as lower SS, OFF-current, and higher ON/OFF current ratio) but NU-doped SOI-JLTs are superior in terms of higher ON current and lower Threshold Voltage. Effective Channel thickness largely depends on doping, so Gaussian doping profile (σ, N_0) play an important role to enhance electrical performance of bulk-JLT in low power application, however it has negative impact on ON-current. Also high-k dielectric material has been used to weigh enhanced performance of non-uniformly doped bulk-JLT.

REFERENCES

1. C. Hu, "Device challenges and opportunities," in *VLSI Symp. Tech. Dig.*,Jun. 2004, pp. 4–5
2. C.W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, and J. P. Colinge, "Junctionless multigate field-effect transistor," *Applied PhysicsLetters*, vol. 94, no. 5, pp. 114–116, 2009.
3. J. P. Colinge, C. W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A. M. Kelleher, B. McCarthy, and R. Murphy, Nanowire transistors without junctions," Nature Nanotechnology, vol. 5, no. 3, pp. 225-229, 2010.
4. J. P. Colinge, C. W. Lee, I. Ferain, N. D. Akhavan, R. Yan, P. Razavi, R. Yu, A. N. Nazarov, and R. T. Doria, "Reduced electric field in junctionless transistors," *Applied Physics Letters*, vol. 96, no. 7, pp. 23–26, 2010.
5. J. P. Colinge, A. Kranti, R. Yan, C. W. Lee, I. Ferain, R. Yu, N. D.Akhavan, and P. Razavi, "Junctionless Nanowire Transistor (JNT): Properties and design guidelines," *Solid-State Electronics*, vol. 65-66, no. 1, pp. 33–37, 2011.
6. S. Gundapaneni, S. Ganguly and A. Kottantharayil, "Bulk Planar Junctionless Transistor (BPJLT): An Attractive Device Alternative for Scaling," IEEE Electron Device Letters, vol. 32, no. 3, pp. 261-263, March 2011.
7. M. Han, C. Chang, H. Chen, J. Wu, Y. Cheng and Y. Wu, "Performance Comparison Between Bulk and SOI Junctionless Transistors," IEEE Electron Device Letters, vol. 34, no. 2, pp. 169-171, Feb. 2013.
8. M. Han, C. Chang, H. Chen, Y. Cheng and Y. Wu, "Device and Circuit Performance Estimation of Junctionless Bulk FinFETs," IEEE Transactions on Electron Devices, vol. 60, no. 6, pp. 1807-1813, June 2013.
9. P. Mondal, B. Ghosh, and P. Bal, "Planar junctionless transistor with non-uniform channel doping," *Applied Physics Letters*, vol. 102, no. 13, pp. 3–6, 2013.
10. P. Bal, B. Ghosh, P. Mondal, and M. W. Akram, "A laterally graded junctionless transistor," *Journal of Semiconductors*, vol. 35, no. 3, 2014.
11. Y. Song and X. Li, "Scaling junctionless multigate field-effect transistors by step-doping," *Applied Physics Letters*, vol. 105, no. 22, pp.2012–2015, 2014.
12. P. Mondal, B. Ghosh, P. Bal, M. W. Akram, and A. Salimath, "Effects of non-uniform doping on junctionless transistor," *Applied Physics A: Materials Science and Processing*, vol. 119, no. 1, pp. 127–132, 2015.
13. B. Singh, D. Gola, K. Singh, E. Goel, S. Kumar, and S. Jit, "AnalyticalModeling of Channel Potential and Threshold Voltage of Double GateJunctionless Field Effect Transistor with a Vertical Gaussian- Like Doping Profile," *IEEE Transactions on Electron Devices*, vol. 63, no. 6, pp. 2299–2305, 2016.
14. H. Ferhati, F. Douak, and F. Djeffal, "Role of non-uniform channel doping in improving the nanoscale JL DG MOSFET reliability against the self-heating effects," *Superlattices and Microstructures*, vol. 109, pp. 869–879, 2017.
15. Ferhati, H. & Djeffal, F. J Comput Electron (2018) 17: 129. https://doi.org/10.1007/s10825-017-1052-1
16. V. Kumari, A. Kumar, M. Saxena, and M. Gupta, "Empirical Model for Nonuniformly Doped Symmetric Double-Gate Junctionless Transistor,"*IEEE Transactions on Electron Devices*, vol. 65, no. 1, pp. 314–321,2017
17. Kaundal, S. & Rana, A.K. J Comput Electron (2018) 17: 637. https://doi.org/10.1007/s10825-018-1131-y
18. *Sentaurus TCAD (Version K-2015.06) Manuals*. Mountain View, CA, USA: Synopsys Inc., 2015.