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A Hybrid Energy Efficient Nano Architecture using Memristors Chaos Systems for Secure Communication

Arul C, Omkumar S

Abstract: ***With an advent of IoT (Internet of Things), number of networked devices increases day by day and will reach its peak by the end of 2020. IoT plays an important role in smart automation, medical informatics, computer vision and even in wearable device engineering. Since IoT transfers the huge data from the machine to machines, achieving the compact size, low power and overcoming the security breaches remains the real challenge among the researchers. With the integration of Nanotechnology, IoT has reached its new dimension to meet the above constraints but still requires much more lime light of research. To meet the above criteria, the paper proposes the new algorithm HEENA (Hybrid Energy Efficient Nano Architecture) which uses the memristors based modelling for data encryption process. The proposed system overcomes the existing CMOS /Nano transistor-based modelling and has following contributions 1) Design of memristor based chaotic non -linear system 2) Generation of Initial conditions using ECG waveforms 3) Generation of High complex Cipher Keys using Diffusion process. The test bed has been developed using BCM2578 SoC and the proposed architecture has been evaluated on the above test bed in terms of sensitivity, and entropy Moreover, the energy consumption is calculated at various cases and results shows that the proposed architecture consumes the less power along with the secured data communication.***

Index Terms: ***Nano Technology, Internet of things (IoT), chaotic non-linear systems, Nano Transistor, Sensitivity, Memristors, Diffusion process.***

I. INTRODUCTION

Memristors are generally called as fourth sort of circuit components which is except for the capacitors, conductors, and resistance. It is brought by Chua in the year of 1971 by utilizing the rule of symmetric [1]. In 1976, the theory was applied to memrisitive gadgets [2]. But it generally took very long time to process and produce the hardware model. In 2018 HP has the view of memristor in nanoscale [3]. Hence the memristor having high potential in many applications in the range of fields, and the memristor becoming a hot topic. So, may of the specialists showing their interest towards the memristor [4,5]. The typical non-volatile memory in nanoscale and memristor based synapse in neuromorphic system. There is material implication in logic operations and non-linear dynamics in the chaotic type of system [17]. In terms of power analysis, Dofe et al has analyzed the different power characteristics of memristor based logic gates.

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* Correspondence Author

Arul. C*, Department of Electronics and Communication, SCSVMV University, Kancheepuram, India.

OmKumar. S,Department of Electronics and Communication SCSVMV University, Kancheepuram, India.

Since the Memristor's width decides the power consumption, memristor normally consumes the less power and finds its application on security application.[18]. SauyubCagri et al designed memristor based ultra-lower power DTMOS and simulated in SPICE environment.[19]. In recent years, with fast improvement of memristor models, a few techniques integrate the chaotic systems and memristor model to reduce the power consumption. This kind of models utilized for the applications such as image encryption, dynamic analysis [22].

Chua and Itoh are developed a typical memristor model in 2008[1]. this framework developed some nonlinear oscillators by generally utilizing memristors which is purely based on Chua's oscillator. this memristors based Chua's circuit is tested and investigated by Petra's in [22]. Simply topology based memristor circuits also designed and developed by Chua and Muthuswamy[23]. All the works appeared in above mentioned papers discussed the memristors extinguishing characteristics. It is to be noted that, these circuits are highly depending on parameters of the circuits. Li utilized memristors (HP) for the implementation of chaotic framework [24].

Ma introduced a 3-dimensional chaotic framework by incorporating hyperchaotic (4 wing) structure for the memristor [25]. Dimitrios introduced new memristive 4D disrupted system in combination with hid attractor structure [26].

Wang deals with a memristor models which is transition controlled and built up a 4-D disorganized framework with this model. The numerical and circuit usage simulation verification were led [27].

Considering the above-mentioned specifications, the security system HEENA has been developed based on Memristor Chaotic systems. The proposed system works on the three-tier architecture which involves the following

1. Modelling of Memristor Based Chaotic Systems
2. Generation of Initial Conditions Using ECG Waveforms
3. Permutation Process for generating the Keys used for Encrypting the data stream

The test bed has been developed using the BCM 2578 SoC and MATLAB is used for modelling the memristor. chaotic systems. The various parameter such as sensitivity, entropy and energy consumption are evaluated and compared with the existing algorithms [28].

Theorganization of the paper are as follows as:

Section-II deals with the related works. The preliminary overview about the memristor modelling, chaotic system designs and the proposed architecture along with the integration of ECG Signals has been discussed in Section-III.

Experimental setup and results are discussed Section - IV and Section V. Finally, conclusion is presented in Section-VI.

II. RELATED WORKS

ZdenekHrubos gives memristor based chaotic circuit. The initial segment talks about 'the scientific verification of the proposed framework, including figuring of an eigenvalues, bifurcation chart and biggest Lyapunov examples. Another part manages hardware acknowledgment and the impact of parasitic properties of dynamic components.

The circuit recreations acquired by PSpice condition and the estimation results on a breadboard are exhibited in the last piece of this work the principle point of this work is amemristor which is based on chaotic structure with vitality stockpiling component (direct detached capacitor) and with less complex development in contrast with different circuits. The following commitment comprises in confirmation of structured circuit as for impact of parasitic properties of dynamic components to chaos destruction [29].

Fernando Corintodiscussed memristor-based chaotic circuits for pseudo-irregular generators. Specifically, the least complex memristor-based chaotic circuit is considered. The circuit comprises of just three arrangement components: inductor, capacitor and memristor. The measurable properties of the created pseudo-arbitrary arrangements have been checked by methods for the NIST test. The outcomes demonstrate that the created generator can be utilized in cryptographic applications [30].

Dawei Ding proposed time-postponed criticism controller for the memristor framework to generally control the chaos andHopfbifurcation with time delay. Many conditions which guarantee the presence of the Hopf bifurcation are picked up by dissecting the relating trademark condition. At that point, this work talks about the impact of input gain on the basic estimation of fragmentary request and time delay in the controlled framework. Hypothetical examination demonstrates that the controller is compelling in postponing the Hopf bifurcation basic esteem by means of diminishing the criticism gain. At last, some numerical recreations are displayed to demonstrate the legitimacy of the proposed hypothetical verification and affirm that the time-deferred input controller is legitimate in controlling tumult and Hopf bifurcation in the partial request memristor based framework [31]. *CafagnaDonato*apresented a framework which is basically a fraction order based memristor and it is described by chaotic characteristics. a theoretical examination of the framework element has been delineated in detail. the proposed framework equilibrium point has been found in the stability analysis. in addition, the chaotic attractor acquired q value of 0.965 in the precise numerical simulations. at last the presence of the chaos is affirmed during the 0-1 test [32]. Xiaofang Hu proposed and examines a memristor based chaotic framework by fusing a HP TiO2 memristor into the accepted Chen's confused framework. All the more absolutely, an accuse controlled memristor model of some boundary conditions is presented. the motion of memristor and electric charge connection is presented in detail. The rich dynamical practices of the memristor-based framework are shown by computing the Lyapunov example range and Lyapunov measurement, watching the tumultuous attractors, investigating the bifurcations [33].

Malay Kuleexhibited a memristor-based decoder configuration designed by utilizing the nanoscale architecture. The outcomes and investigation demonstrate that the proposed decoder beats a prior plan as far as the quantity of preparing steps. the proposed system enhances the operating time but at the same time it increases the cost to some extent. The circuit can be utilized as a line or section decoder for nanoscale crossbar circuits [34].

Yuxia Li implemented new design of chaotic based memristors and which replaces the nonlinear resistors in the circuit namely canonical chaos circuits integrated with flux controlled memristors. The presence of the disorder isn't just exhibited by PC simulations, yet in addition checked with Lyapunov types and bifurcation verification. Breadboard circuits also presented for the implementation of the chaotic circuit, b utilizing the capacitor, resistor, inductor and memristor. Diverse chaotic attractors are shown by both numerical simulations and electronic examinations [35]. Yuxia Li presented a chaotic circuit based on memristor, which is from the Chua's circuit. This clamorous circuit utilizes just the four essential circuit components, and has just one negative component notwithstanding the nonlinearity. The presence of the chaos isn't just shown by PC simulations, yet in addition checked with Lyapunov types, bifurcation, Poincare mapping and power range verification [36].

Seda Arik introduced "Field Programmable Analog Array-FPAA", to experimentally test the chaotic based memristor circuit. Based on these types of circuit it is possible to produce various non-linear functions in the hardware without utilizing any kind of emulators. this is the reason, there are 2 circuits which are based on the chaotic memristor circuits were developed and the performances were tested experimentally [37].

Sanju Saini has used a memristor Sanju Saini has used a memristor circuit for the chaotic framework synchronization. For the communication, two separate channels have been utilized. one is generally for sending the sign and the other for synchronizing the drive and reaction circuits. high stability is attained with coinciding attractorsfor systems with coexisting attractors [38].

III. PROPOSED ARCHITECTURE

A. Memristor Based Modelling

The definition of memristor can be given by two nonlinear function by using voltage and current.

$v = S(u)$ (1)

$i = P(\varphi)v$ (2)

where S(u) → non-linear function of memresistance

P(φ) → nonlinear function of mem conductance and they are given as follows

$$S(u) = \frac{d\varphi(u)}{du} \quad (3)$$

$$P(\varphi) = \frac{du(\varphi)}{d\varphi} \quad (4)$$

The flux controlled memristor is presented by the equation (2) in which the current is terminal current. And the voltage is terminal voltage which is given as follows.

$$i(t) = \frac{du}{dt} = \frac{du}{d\varphi}\frac{d\varphi}{dt} = \frac{du}{d\varphi}v(t) = P(\varphi(t))v(t) \quad (5)$$

Zhong characterized the Chua's circuit with the Nonlinear resistor. It infers that the cubic non-linearity of the memristor shows the non-linearity characteristics.[9] The cubic polynomial meaning of memristor is characterized as pursues:

$$u(\varphi) = a\varphi + \beta\varphi^3 \quad (6)$$

The proposed work is based this relation which is given as follows.

$$P(\varphi) = \frac{dq}{d\varphi} = \alpha + \beta\varphi^3 \quad (7)$$

B. Memristor Model for Non-Linear Chaotic System

Memristors dynamical state equations can be described as follows

$$\frac{d\dot{\varphi}(t)}{dt} = \dot{v}_{c_1}(t)$$

$$L\frac{di_L(t)}{dt} = \dot{v}_{c_2}(t) \quad (8)$$

$$C_1\frac{\dot{v}_{c_1}(t)}{dt} = \frac{1}{R}(\dot{v}_{c_2}(t) - \dot{v}_{c_1}(t)) - P(\dot{\varphi}(t))\dot{v}_{c_1}(t) \quad (9)$$

$$C_2\frac{\dot{v}_{c_2}(t)}{dt} = \frac{1}{R}(\dot{v}_{c_1}(t) - \dot{v}_{c_2}(t)) - \dot{i}_L(t)$$

By considering the parameters α, β and other circuit parameter regards from [25], [26] this unscaled structure generally gives up to hundred amps and voltages above kilo volts. In standard activity amp-based executions streams and voltages are scaled about at mA and ten-volt levels [25], [26]. For our CMOS structure we need to diminish much lower than these measurements. Rescaled current and voltages are portrayed as

$$\varphi(t) = \frac{1}{\delta}\dot{\varphi}(t)$$

$$v_{c_1}(t) = \frac{1}{\delta}\frac{1}{\gamma}\dot{v}_{c_1}(t) \quad (10)$$

$$v_{c_2}(t) = \frac{1}{\delta}\frac{1}{\gamma}\dot{v}_{c_2}(t)$$

The above equations are rescaled in accordance to the CMOS designs are given as follows

$$i_L(t) = \frac{1}{\delta}\frac{1}{\gamma}\dot{i}_L(t)\frac{d\varphi(t)}{dt} = \frac{v_{c_1}(t)}{\delta}$$

$$\frac{di_L(t)}{dt} = \frac{v_{c_2}(t)}{L}$$

$$\frac{dv_{c_1}(t)}{dt} = \frac{1}{C_1}\left(\frac{v_{c_2}(t)-v_{c_1}(t)}{R}\right) - (\alpha + 3\beta\varphi^3(t)v_{c_1}(t) \quad (11)$$

$$\frac{dv_{c_2}(t)}{dt} = \frac{1}{C_2}\left(\frac{v_{c_1}(t) - v_{c_2}(t)}{R}\right) - i_L(t)$$

$$\beta = \dot{\beta}\frac{1}{\gamma^2} \quad (12)$$

The above equations are rescaled into an CMOS designs and used for the implementation in the hardware.

C. Generation of Initial Conditions

For the most secured communication and to increase the randomness of the key, the proposed architecture uses the ECG waveforms to generate the initial condition of proposed chaotic system. It is realized that various people will have diverse ECG waveforms and they can have distinctive ECG waveforms for a similar individual at various duration of time which is shown in fig. Since the human body is the complex machine, integration of ECG waveforms as the initial conditions leads to the complex randomness of the key. The paper uses the new cognitive R-R detector for extraction of 'R' waveforms for every time secs and used for the initial conditions.

D. Encryption Process

After cumulating the sequence generated from the integration of the ECG waveforms along with the designed chaotic systems, 'S' vector is formulated as shown in eqn(). The formulated 'S' matrix is then XORed with the input data streams which has been scaled to 256 to yield Y matrix. Since the permutation process deals with the only with the shuffling of the data, to ensure the high randomness in the key, the proposed architecture uses the diffusion process between the key and data.

$Y = [S_i]$ Xor $[D_i]$ where i=0,1,2,3……256 (13)

Before processing into diffusion, all the elements in S matrix should be scaled to 0 to 255 through equation (13) to satisfy the input data transmission time.

The new dynamic constant α has been introduced in the diffusion process and the diffusion operation μ for the input data streams are given in equation (14)

$\alpha = \sum D(i) \bmod 256$

where i=0,1,2,3……256 (14)

$\mu = Yi + \alpha + D(i) \bmod 256$

where 0,1,2, 3……M (15)

where D(i)= Input data streams

The final new cipher data is obtained after the diffusion process between the dynamic keys and the data streams has completed.

E. Complete Encryption Cycle

The complete cycle of the proposed encryption system is detailed by the following steps.

Step 1: Input Data from the IoT Sensor Node is obtained.

Step 2: Divide the Input Data streams into the length eight bytes which are scaled in accordance with the application (Our Case is 256).

Step 3: Modelling of Memristor based Non-Linear Chaotic Systems

Step 4: Generation of initial conditions using the ECG Signal with cognitive R-R Filters

Step 5: Formation of 'S' vector which has been formulated by XORing the Memristor based chaotic system which is then depends on the R-R waveforms.

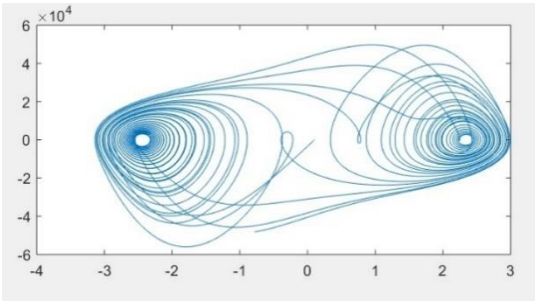
Step 6: Permutation of the Key formulated and arranged in Y matrix which are scaled to 256.

Step 7: Diffusion process is Performed with the key and data streams

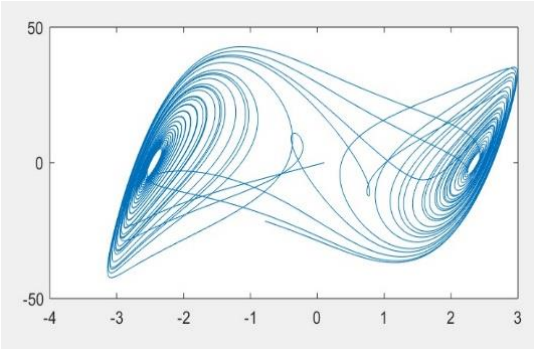
Step 8: New Key is formulated for encryption process.

IV. EXPERIMENTAL SETUP

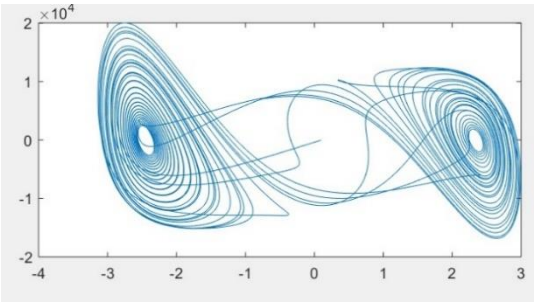
MATLAB Version R2019 is used for the modelling the memristor based chaotic systems, simulating the ECG waveforms and extraction of the R-R intervals to permutate the data streams. The following shows the different process involved in the proposed HEENA architecture which are simulated using MATLAB.



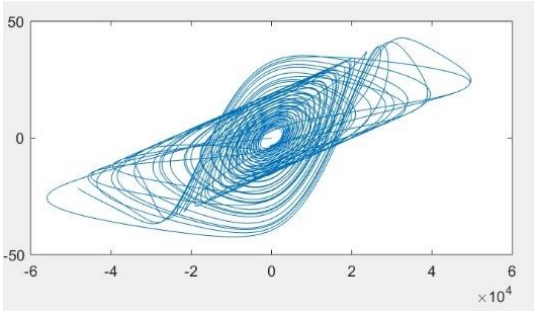
(a)



(b)



(c)



(d)

Fig. 1. Phase Component Analysis of the proposed memristor based Chaotic Systems

As discussed, the ECG Signals are used for the generation of initial conditions, PhysioNET databases were used for simulating the ECG waveforms. The proposed architecture consists of the Class 1 American standard of ECG waveforms from 10 recordings. The ECG waveforms are simulated based on the above specifications are depicted in the following fig

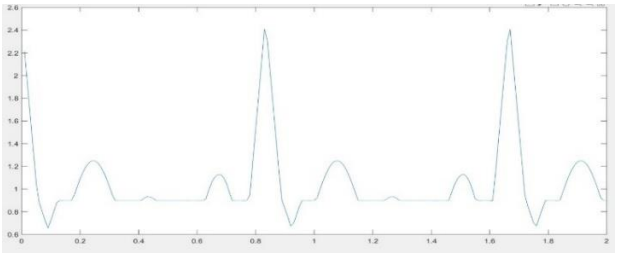


Fig. 2 Simulated Normal ECG Waveforms using the PhysioNET Databases (1 Recording).

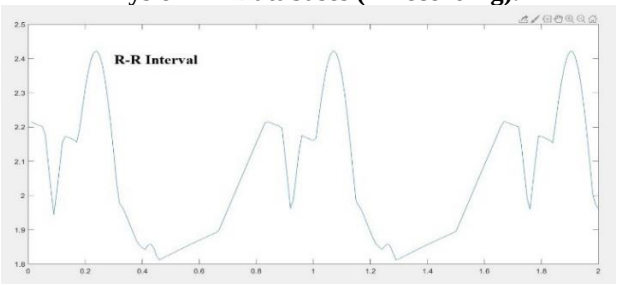


Fig. 3. Simulated Normal ECG Waveforms using the PhysioNET Databases (II Recording).

V. RESULT ANALYSIS

A. Sensitivity Analysis

The proposed HEENA encryption algorithm has been tested with number of negative permutation of data bits such as the changing the input data bits with the gradual change of 5%,10%,15%,20%25%,50%,75% and 100% changes and following parameters such as Number of Pixel Change rate(NPCR) are calculated by the following equation[15]

$$NPCR = \{[\sum_i D(i)]/N\}x100\% \quad (15)$$

Where D(i) is the input data length N = No of negative permutation of Input data bits

The NPCR were calculated by using above equation at the different cases are tabulated in the tableI

Table I Sensitivity Analysis for the Proposed Algorithm with the Changes in the Bit values

Sl.No	Changes in data position bit	NPCR
01	5%	99.6%
02	10%	99.6%
03	15%	99.65%
04	20%	99.6%
05	25%	99.6%
06	50%	99.6%
07	75%	99.6%
08	100%	99.6%

Table I clearly shows that NPCR has been maintained at constant rate of 99.6% even though the bit values are changed at the different proportions

B. Energy Consumption Analysis

The Energy consumption of the proposed HEENA architecture has been evaluated on SoC BCM 2578 and Instruction per cycle (IPC) has been considered for calculating the energy consumption.

IPC has been calculated for every iteration and total energy has been calculated by the following equation (16). The two cases were taken for consideration in which the energy consumption (proposed architecture)and the normal chaotic architecture were calculated and compared. The energy consumption of HEENA architecture is depicted in fig 4

$E_c = V*I*(1/IPC)$ (16)

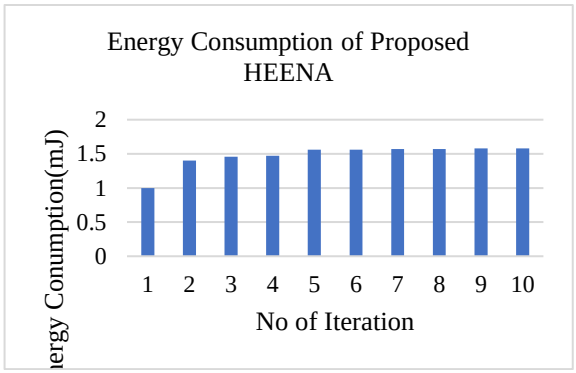


Fig. 4. Energy Consumption of the Proposed HEENA for Total Encryption Mechanism in BCM2578 SoC

Fig.4 shows proposed architecture total energy consumption using BCM2578 SoC. The proposed architecture consumes only 50% of the energy consumed by the normal chaotic systems. The memristor based non-linear system consumes less energy and has high randomness.

VI. CONCLUSION

The proposed architecture replaces the traditional CMOS technique with the Nano based memristor for formation of high complex encryption key with the less energy consumption which is considered to be suitable for the IoT Cloud security system. The proposed architecture employs the design of chaotic systems using the memristor and ECG waveforms were used for the initial conditions. The key is formulated by XORing the input data streams and key. Again, the cipher text is formed by diffusion between the data streams which in turn increases the randomness of the key. The proposed architecture has been implemented and tested on BCM2578 SoC (System on Chip) and performance in terms of sensitivity and energy consumption was calculated. Sensitivity was found to 99.6% and energy consumption is reduced nearly 50% of the normal chaotic systems. Even though the proposed HEENA architecture shows the memristor based encryption is considered to be unique method, but still needs little improvisation for further implementation in chip level designs.

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AUTHORS PROFILE

Tmt. C. Arul. Research Scholar at Sri Chandrasekharendra SaraswathiViswamaha Vidyalaya University, Enathur. Working as a Senior Lecturer in the Department of Electronics and Communication Engineering at Bhaktavatsalam Polytechnic College, Kanchipuram Since 1999. She has completed her studies BE(ECE) at university of Madras and ME (Embedded Systems) at Anna University, Tiruchirappalli. She has published 3 papers in International Journals.

S. Omkumar. He received PhD Degreein the area of Communication andnetworking. His research interests arewireless communication and antennas.He was published around 50 papers inInternational Journals, National andInternational Conferences. He is currentlyworking as Associate professorin the department of Electronics and CommunicationEngineering at Sri Chandrasekharendra SaraswathiViswamaha Vidyalaya University. He also guest editedseveral journal special issues and served in severalinternational conferences as advisory and technicalprogram committee.