International Journal of Engineering and Advanced Technology (IJEAT)
ISSN: 2249-8958 (Online), Volume-8 Issue-6, August, 2019

Wave Pipelined Area Efficient LDPC Encoder

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Abstract: ***This paper present efficient design of Low Density Parity Check (LDPC) Encoder with wave psipeline. Comparing to decoding, LDPC Encoding was relatively more complex. There are several methods to perform encoding. Among all the existing methods to reduce parity check matrix Gauss Elimination method was used. To overcome the cons like latency and area overheads of conventional pipelining, Wave pipelining technique was used. LDPC encoding was designed with different stages of pipeline and the encoding performance is evaluated with wave pipeline. Implementation of this architecture was done on Xilinx FPGA XC2VP100 device. Wave pipeline will reduce the time delay and area overhead which can be proved by synthesis report.***

Index Terms**: *Gauss Elimination, LDPC codes, LDPC encoder, Wave pipelining.***

I. INTRODUCTION

LDPC codes have major attention in research community and accessible for attaining reliable information transmission. LDPC codes are excellent error correcting codes. The major characteristics of this code is the parity check matrix H contains only less number of one's compared to the number of zeros. To reduce the number of 1's we are applying many algorithm and methods. Among them we have used Gaussian elimination which reduces the matrix H by applying elementary row and column operations. To achieve better performance in terms of area, speed and throughput the wave pipelining technique is used.

In a digital system, clock frequency is increased by a design methodology called wave pipeline. This methodology is also named as Maximal Rate Pipelining. Internal clock element was not required in wave pipelining, unlike normal pipelining which results in increase throughput. The difference between shortest and longest path delay provides the logic rate that can propagate through the circuit which doesn't depends delay on the longest path.

In an attempt to get better throughput, pipelining is important. A logical network was divided into number of stages, each pipeline stage was operated upon previously computed data from previous stage this was the working principle of a pipelined system. Registers or latches are inserted in between the partition network. The throughput increases up to M factor if the logic network is pipelined into M stages, which results in significant increase in the power and area consumption. By this increase in consumption, register cycle time as well as the latency is increased. Wave pipelining is an unconventional synchronous circuit that allows overlapped execution of multiple operations without using flip-flops and register within the logic network. Evaluation chart of wave pipelined and different stages of pipelined architecture has been shown. Construction of this paper is as follows. Section II and III gives the general idea about LDPC encoder and its reduction techniques. Section IV discusses about the theory of wave pipelining. Sections V & VI gives the implementation of the LDPC encoder and the different pipelining stages of the encoder operations. Section VII discusses about the synthesis report of the designs and its evaluation and finally section VIII deals with paper conclusion.

LDPC CODES

Low Density Parity Check (LDPC) codes are a type of linear block error correcting code discovered by Gallager in 1962 which is also called as Gallager codes. LDPC codes are characterized by greater flexibility; lower decoding complexity as compared with Turbo codes; parallel capability which facilitates the hardware implementation; in a communication system high speed design of decoding is done with high throughput. There are two different methods to represent LDPC codes. The LDPC codes are represented via matrix and diagrammatical representation.

II. LDPC ENCODER

The encoder of LDPC has two main tasks: Construction of sparse parity check matrix and generation of code word with sparse matrix. Sparsity indicates that each symbol node has few connections to check the nodes in the tanner graph. The parity check matrixes which contain only a few number of 1's is compared to the number of 0's.To reduce the number of 1's we are applying different algorithm and method. Gaussian elimination which reduces the parity check matrix H by applying elementary column and row operations is one of the methods used to reduce the parity check matrix. The generator matrix G is done using the matrix inversion method, where G is given by $G = \{I_k | A^T\}$.

A. Code Matrix H and Generator Matrix G

A bipartite graph is a Tanner graph with r check nodes and n symbol nodes where $n \geq r$.The code matrix $H \in GF(2)^{r,n}$ for this code is the adjacency matrix of the graph; $H_{i,j}$=1 if and only if C_i is connected to S_j .Let $m = (n - r)$. The generator matrix $G \in GF(2)^{m.n}$ is constructed from reduced row-echelon form of H; H can be transformed to $H = \{[P \in GF(2)^{r,m}] | [I \in GF(2)^{r,r}]\}$

Revised Manuscript Received on October 30, 2019.
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via Gaussian elimination and the generator matrix is given $H = \{[I \in GF(2)^{m,m}]|[P^T \in GF(2)^{m,r}]\}$.

B. Gaussian Elimination Method

To reduce the number of 1's we are applying many algorithm and methods. One of the conventional methods LDPC encoding is Gauss elimination where the Generator matrix

represented by G is derivative of H which represents parity-check matrix by Modulo-2 operation. Row permutation, modulo-2 sums of row and also some column variation are done to calculate the unknown G matrix from H matrix. The (n, k) represents codeword and H is given by $H = \{A|I_k\}$. G is given by $G = \{I_k|A^T\}$. By Gaussian Elimination operation, the parity-check matrix H is reduced. Codeword v is obtained from the equation $v = u \times G$. The codeword equation is obtained by matrix multiplication operation. The encoding process consists of normal matrix multiplication and matrix inversion.

$$\begin{bmatrix} a11 & a12 & . & . & a1n \\ a21 & a22 & . & . & a2n \\ . & . & & & . \\ . & . & & & . \\ . & . & & & .. \\ an1 & an2 & . & . & anm \end{bmatrix} \begin{bmatrix} X1 \\ X2 \\ . \\ . \\ . \\ XN \end{bmatrix} = \begin{bmatrix} b1 \\ b2 \\ . \\ . \\ . \\ bn \end{bmatrix}$$

IV. WAVE PIPELINING

In a digital system, clock frequency is increased by a design methodology called wave pipeline. This methodology is also named as Maximal Rate Pipelining. The logical elements are pipelined at a fine grain level. The synchronization of internal operations was obtained by equating inherent RC delay. The difference between shortest and longest path delay provides the logic rate that can transmit all the way through the circuit which doesn't depends delay on the longest path.

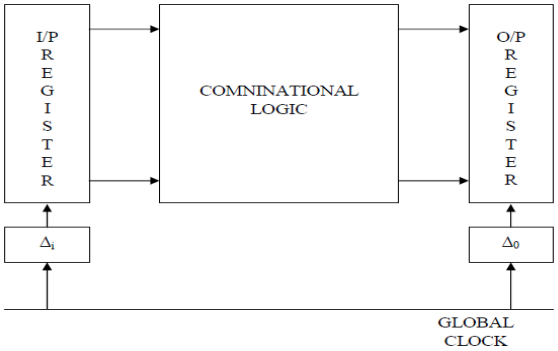

Fig1. Wave pipelining

Wave pipelining is a technique to increase the number of pipeline stage in a logic network without increase the number of flip flops. Figure 1 shows wave pipelined structure. This produces many paths having delays which are much lesser than the critical path delays. The clock speed improves when the non-critical paths remain idle. If the ideal time of paths which are non critical are reduced due to the increase in the clock speed.

V. IMPLEMENTATION

LDPC encoder has been designed with the Gaussian elimination method. In LDPC encoder this algorithm is used to reduce the PCM by reducing number of 1's and placing zeros above the diagonal in the matrix. It uses row permutations, modulo-2 sums of rows and some column permutation. By applying elementary row operations the reduced parity check matrix $H \in GF(2)^{r,n}$ is given by $H = \{A|I_k\}$ and the generator matrix $G \in GF(2)^{m.n}$ for parity check matrix is given by $G = \{I_k|A^T\}$.where I_k is called as identity matrix and A is the parity check matrix.

The block diagram for the LDPC encoder is designed based on the operation involved in normal encoding process. The fig. 2 shows the flow of LDPC encoder.

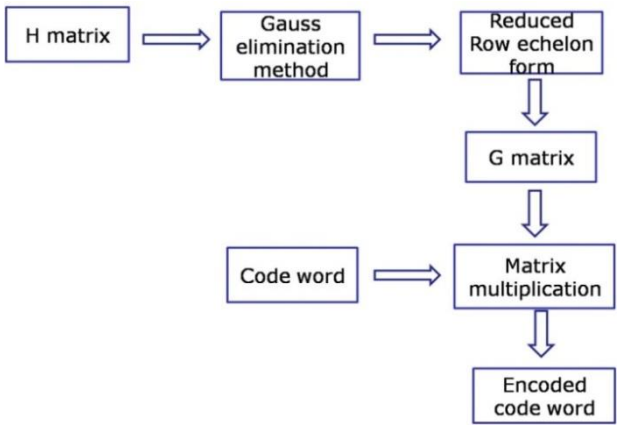

Fig2. Flow of LDPC encoder

A. Steps for H Matrix Reduction

The H matrix of size (5,10) is reduced using the following step. Where H matrix is shown below.

$$H = \begin{bmatrix} 1 & 1 & 0 & 1 & 1 & 1 & 1 & 0 & 1 & 0 \\ 0 & 1 & 1 & 0 & 1 & 1 & 0 & 1 & 1 & 0 \\ 0 & 0 & 0 & 1 & 0 & 1 & 0 & 0 & 1 & 1 \\ 1 & 1 & 0 & 0 & 0 & 0 & 1 & 1 & 0 & 1 \\ 0 & 0 & 1 & 0 & 0 & 1 & 0 & 1 & 0 & 1 \end{bmatrix}$$

For row echelon form(H_r) the following steps are performed in above matrix

i. Ones below diagonal of columns 1 and 2 are removed by modulo 2 additions of rows 1 and 4. The columns 1 and 2 have entities of one on diagonal of H matrix.

ii. Swapping of rows 3 and row 5 is done to have one 0n the diagonal of column 3.

iii. Row echelon (Hrr) form obtained by performing modulo-2 addition of row 5 and row 4 to replace row 5. For reduced row echelon H_{rr} form the following step are done in H_r matrix.

i. The column 1 is already in correct form so in the column 2 ones on top of the diagonal is removed by substituting row 1 by means of the modulo- two addition of the rows 1 and 2.

ii. One present above diagonal of the column 3 is removed by performing modulo-two addition of rows 2 and 3 resultant is replaced on row 2 and row 1 is substitute with modulo-two addition of rows 1 and 3.
iii. In column 4 the first row is changed with the modulo-two addition of rows 1 and 4
iv. The column 5 is cleared by summing row 5 with rows 1, 2 and 4.

The reduced row echelon H_{rr} is forced a matrix inversion to form Generator matrix G which is show below.

$$G=\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 0 \\ 0 & 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 1 & 1 & 0 & 1 \\ 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 1 & 0 \end{bmatrix}$$

Encoding of a code vector C € $GF(2)^m$ yield a valid encode codeword Y € $GF(2)^n$ is performed by $Y = C \times G$.

VI. PIPELINING STAGES

The conventional method to decreasing the clock period of the system is by pipelining the combinational block. Where the combinational block is divided into 2 and the registers are inserted in between them. It leads in the reduction in the critical path.

A. *Two stage pipelining*

The following fig 3 shows the two stage encoder structure.

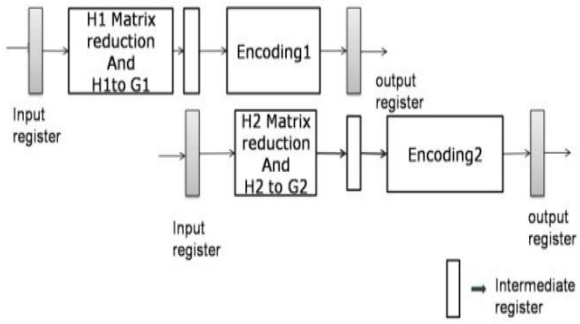

Fig3. Two stage pipelining

As it could be seen, the combinatorial block is split up into two stages and an intermediate latch is included between the blocks.

B. *Three stage pipelining*

The following fig 4 shows the two stage encoder structure

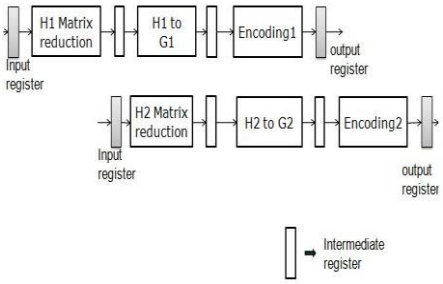

Fig 4. Three stage pipelining

As it could be seen, the combinatorial block is split up into three stages and an intermediate latch is included between the blocks. Because of increase in the intermediate latches the area and the clock used by the latches increases. Thus it can be overcome be using wave pipelining.

VII. SYNTHESIS

The two stages and three stage pipelined architecture have been designed, its functionalities are verified with Modelsim and the synthesis is done using Xilinx 9.2i. Our implementations are on a Xilinx Virtex-ii FPGA XC2VP100 device. Recourse utilization of different stage of pipelined and wave pipelined is given by Xilinx synthesis report. To design a faster performing architecture the concept called delay balancing is performed. Report of wave-pipelined architecture proves the reduction of area utilization of LDPC encoder. Latency is also analyzed between different pipelined structures with wave pipeline, which shows the wave pipelined structure is better. The reduction in number of flip flops, number of slices and number of LUT has been identified because of the concept of delay balancing. In combinational blocks, buffers are inserted. This insertion provides the way to reduce resources in the architecture of input and output blocks. The evaluation involving the stages of pipelining in terms of their device utilization of encoder $(5,10)$ is given in the table I.

Table I. Logic Utilization of LDPC Encoder$(5, 10)$

Logic Utilization \ Stages	2STG	3STG	WAVEPIPE
Number of Slice Flip Flops	330	370	140
Total equivalent gate count for design	4416	7523	1810

The above table provides the evidence of reduction in flip flops count and total equivalent gate design count by using the wave pipelining technique. Increase in stages of pipeline will result in increase in the flip flops count and total equivalent gate design count due to synchronization elements. But in wave pipeline architecture, synchronized elements are reduced so the device logical utilization get reduced.

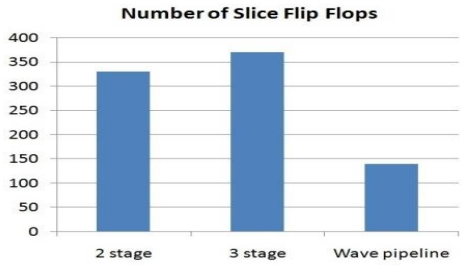

Fig 5. Number of Flip Flops

Table II demonstrate the Latency analysis among the pipelining and the wave pipeline structure. It has been verified that the wave pipeline structure significantly reduces the latency overhead.

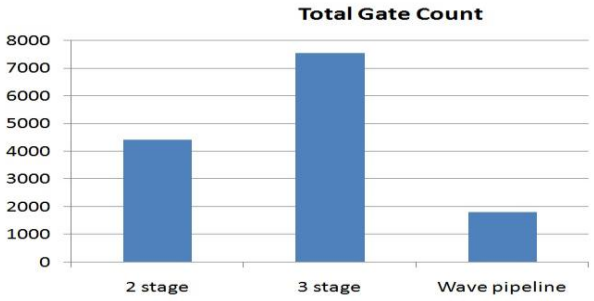

Fig 6. Total Gate Count

Table II Timing Analysis

Pipeline stages	No. of Clock cycles
2stage	5
3stage	6
Wave pipelining	2

VIII. CONCLUSION

The LDPC codes which is of greater attraction towards many application of communication systems. The Low Density Parity Check encoder was realized in Field Programmable Gate Array with pipeline stages. With the structure of wave pipeline architecture, the optimization of the architecture in terms of speed and area can be introduced. This work can be extended towards the power optimization, to design an enhanced Low Density Parity Check (LDPC) Encoder.

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