International Journal of Engineering and Advanced Technology (IJEAT)
ISSN: 2249-8958 (Online), Volume-8 Issue-5S3, July 2019

Optimization of CSA for Low Power and High Speed using MTCMOS and GDI Techniques

Tulasi Radhika Patnala, Sankararao Majji, Gopala Krishna Pasumarthi

Abstract: ***The basic operation involved in any analog, digital, control system, DSP's is addition. Performance and reliability of almost every digital system is depends on performance of adder. Over the decade, many adder architectures are proposed and still research work is going on adder to obtain the best results in power, delay and power delay product (PDP). In this paper we proposed one of the fastest adder architecture called Carry Select adder (CSA) and optimization is done for performance parameters like delay and power using GDI (Gate Diffused Input) and MTCMOS techniques. Implementation has been done in standard gpdk 90nm technology using Cadence tool.***

Index Terms: carry select adder, Gate Diffused input, power delay product and MTCMOS.

I. INTRODUCTION

As portability becomes more prominent and limited battery life time imposes strict demands on overall power consumption in very high density VLSI chip design, there is a need to limit the power consumption (heat dissipation). On the other hand, the influence of supply voltage on power dissipation is limited the speed of operation. As many of the processors contains adders in their critical path. An efficient adder technique can enhance the processing speed by reducing the critical path delay. Several addition techniques are proposed. Out of which Carry select adder (CSA) has simple architecture and fastest in terms of operation speed.

II. CONVENTIONAL METHODS

The way of connecting full adders to add multiple bits defines its architecture. In general architecture defines the computation time of an adder. Several adder architectures are discussed in this section.

A. Ripple Carry Adder

As the name suggest carry ripples from one stage of adder to the next stage via LSB to MSB as shown in Fig.1. In this type of architecture, each full adder must wait for the carry bit from the previous full adder, hence speed of operation is slow and it is worst while going for the addition of more number of bits. RCA suffers from glitching problem which causes extra power dissipation.

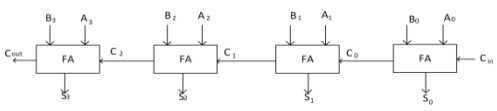

Fig. 1. RCA block diagram

Manuscript published on 30 July 2019.
***** Correspondence Author (s)
Tulasi Radhika Patnala, ECE, Gokaraju Rangaraju Institute of Engineering and Technology, Hyderabad, India.
Sankararao Majji, ECE, Gokaraju Rangaraju Institute of Engineering and Technology, Hyderabad, India.
Gopala Krishna Pasumarthi, IT, Gokaraju Rangaraju Institute of Engineering and Technology, Hyderabad, India.

B. Carry Look ahead Adder

The delay of carry bit in RCA is diminished in Carry Look ahead Adder by estimating the carry bit, based on stream of input data. But it requires some extra hardware to calculate the carry bit in prior. So CLA is least preferable because of its complex hardware and more area on the chip. The primary advantage of CLA is the delay of sum and carry bits are independent of number bits.

C. Prefix Adder

In this type of adder all carry bits are generated parallelly and fast computations are obtained at the expense of power and area. The most favorable type in its kind are Parallel Prefix Adders (PPA), such as Kogge-stone, Brent-kung, Han-Carlson and Ladner-Fischer adders. Today's VLSI chips are mostly rely on faster and reliable arithmetic operations which can be provided by parallel prefix adder (PPA). Due to large fan-out and long interconnecting wires, which causes larger delays, PPAs are not preferable in all applications. We can reduce the fan out and long interconnecting wire problem at the expense of area and power.

D. Carry Select Adder

Carry select adder works on the principle of parallel com-putting [1]. In this method we assume input carry (C_{in}) for both possible values i.e. C_{in} = 0 and C_{in} = 1 and result is evaluated for both the values parallelly. After getting the correct carry bit (C_{in}), the results will be chosen with the help of a 2:1 Multiplexer as shown in Fig.2. In CSA, the input data to the adder is divided into two blocks and for each block sum and carry bits are evaluated for both the cases i.e., for C_{in}=0 and C_{in}=1. The total gate delay is minimum when both the phases of C_{in} are equal. Compared to conventional method of adders, CSA occupies more area but performance is high compared to remain architectures. In this section we proposed GDI technique into the CSA to optimize it for area, power dissipation as well as delay [3]. It is further improved by using modified technique i.e. combination of both GDI and MTCMOS techniques by which we will get significant improvement in Power Delay Product (PDP).

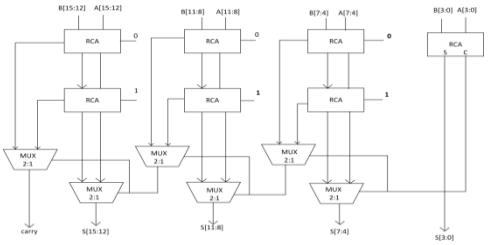

Fig. 2. CSA Block diagram

III. BACKGROUND OVERVIEW

A. The shrink in chip size and growth in chip density, surge the difficulty in high performance and low power design. Hence, leakage power reduction & high performance are emerging as a primary goal of VLSI industry. In this work, we proposed techniques to enhance the performance and to minimize the leakage power. ***MTCMOS technique***

Static power (Leakage power) reduction is emerging challenge in VLSI circuit design. Several low power techniques are proposed and MTCMOS is one of its kind. Compared to all other leakage power reduction techniques, MTCMOS gives better power results. It can achieve a low threshold voltage and therefore higher performance as well as smaller stand by leakage currents. MTCMOS technique uses sleep transistor approach for reducing power dissipation. A set of high threshold sleep transistors i.e. PMOS and NMOS are used. MTCMOS consists of logic network of low threshold voltage and high threshold voltage for NMOS and PMOS sleep transistors.

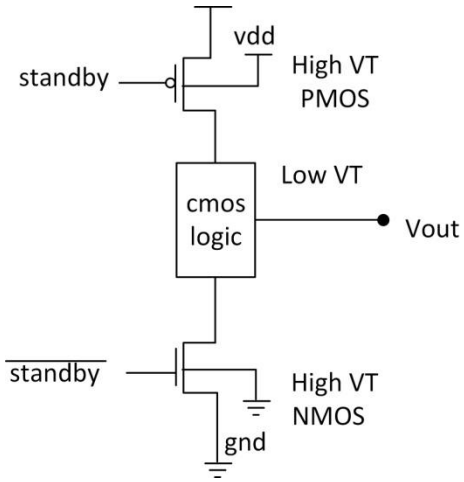

Fig. 3. MTCMOS logic

A. GDI technique

Gate Diffused Input technique is a low power digital circuit design technique. It has almost similar structure as conventional CMOS but occupies lesser area as compared to CMOS. Hence effectively minimizing the number of transistors count. The basic GDI cell shown in Fig.4 and its logic table given in Table.1.

In GDI cell, the sources of PMOS and NMOS are not connected to the VDD and ground respectively. This makes GDI cell has two extra input pins that makes GDI more flexible than usual CMOS design. GDI cell consist of 3 input terminals G, P and N. The various functions that can be implemented with basic GDI cell which consist of only two transistors. The main advantage of GDI is large number of functions can be implemented by using basic GDI cell.

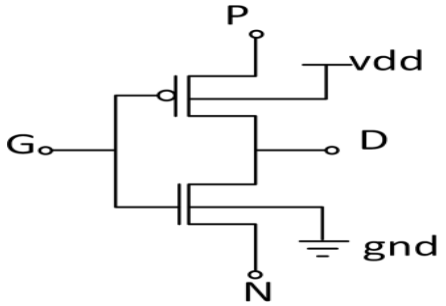

Fig. 4. Basic GDI cell

N	P	G	Out	Function
0	1	A	A’	NOT
B	0	A	AB	AND
1	B	A	A+B	OR
C	B	A	A’B+AC	MUX
B’	B	A	A’B+AB’	XOR

Table.1: GDI logic table

IV.PROPOSED TECHNIQUE

The proposed technique (MTGDI) shown in Fig.5 has combination of both GDI and MTCMOS. By this modified technique we can achieve high performance and leakage power is minimized. In this technique low threshold voltage logic network in MTCMOS is implemented using GDI technique instead of conventional CMOS logic so the transistor count can be reduced.

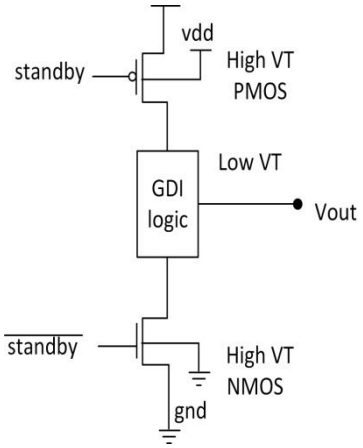

Fig. 5. MTGDI logic

A. 8 bit CSA using proposed technique

This type of CSA architecture consists of Ripple carry adders and multiplexers as shown in Fig.6. For an 8-bit Carry Select Adder, we require three RCA blocks and one 2:1 Multiplexer. Carry- out of the first block of RCA is given to multiplexer as selection line. The output sum bits from the remaining RCAs are given to multiplexer. Based on the Cin bit the output sum will be generated. An 8-bit CSA architecture is shown below.

Retrieval Number: E10620785S319/2019©BEIESP
DOI:10.35940/ijeat.E1062.0785S319
Journal Website: www.ijeat.org

Published By:
Blue Eyes Intelligence Engineering and Sciences Publication (BEIESP)

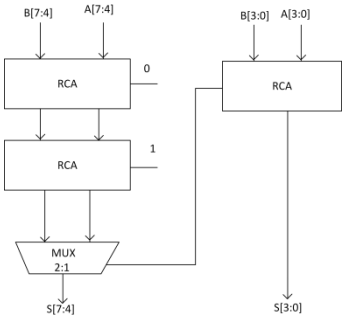

Fig. 6. 8-bit CSA block diagram

A. 16-bit CSA using proposed technique

As shown in Fig.2, the 16-bit CSA architecture consists of seven RCA blocks in two levels and six 2:1 multiplexers. The RCA blocks and multiplexers used in this technique are implemented by using GDI technique so that it occupies less area as compared to conventional CMOS architecture. The parallel computing principle of CSA reduces the delay and introduction of GDI logic further reduces the delay to a significant value. The overall architecture is then implemented with MTCMOS logic. As the MTCMOS technique is used for the reduction of power dissipation, the CSA implemented using both GDI and MTCMOS techniques improves power dissipation to the lowest level. The schematic of the 16- bit CSA architecture implemented by using cadence virtuoso schematic editor is shown below.

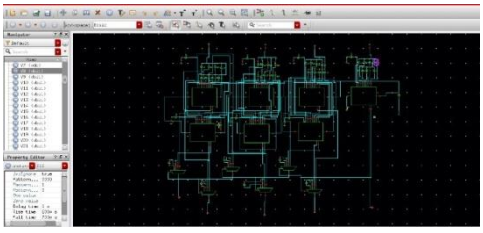

Fig. 7. Schematic of 16-bit CSA

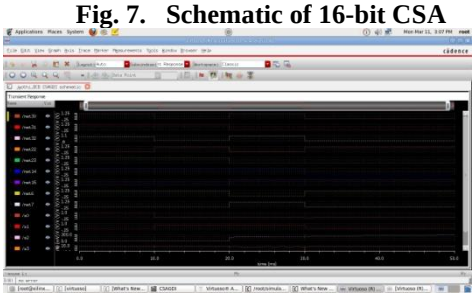

Fig. 8. 16-bit CSA transient response

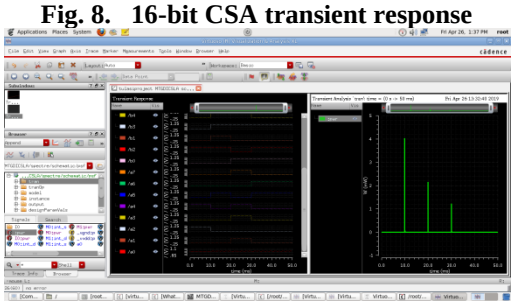

Fig. 9. CSA transient and DC power

B. Simulation And Results

The proposed technique is simulated using cadence standard gpdk90nm technology. The performance parameters such as delay and power dissipation are measured with supply voltage of 1.8 Volts. The length and width of both NMOS and PMOS are 100nm and 120nm respectively. Power and delay results are obtained from the transient analysis and values are tabulated. The power and delay results for the proposed CSA are given in Table.3.

IV. COMPARISONS

Carry Select Adder (CSA) is compared for power and delay by using various techniques like GDI, MTCMOS and combination of both. Transistor count is reduced drastically by using GDI logic and the count for different bit size are tabulated as shown in table.2. Schematic results of CSA for the above mentioned techniques are shown in simulation results among all architectures, combination of GDI and MTCMOS gives better results in terms of power, performance and area occupied on the chip. Transistor count is improved by 63.52% using proposed technique compared to conventional CMOS logic.

Type of adder	**CMOS**	***GDI***	***MTGDI***
8-bit CSA	360	126	128
16-bit CSA	806	292	294

Table.2: Transistor count

	8-bit CSA		16-bit CSA	
Type of power	GDI	MTGDI	GDI	MTGDI
Leakage power(µW)	0.039	0.009	0.045	0.002
Dynamic power(µW)	0.1	0.083	0.09	0.04
Peak power(µW)	9.04	4.30	44.10	5.13
Delay (nS)	78.09	84.12	199.0	203.19

Table.3: Power & Delay results of CSA

V. CONCLUSION

The carry select adder (CSA) proposed in this paper is optimized for low power as well as high performance by using proposed technique. Overall power delay product (PDP) of CSA is improved by a large extent by using proposed technique. It has been observed that the combination of MTCMOS and GDI produces low leakage power and delay is optimized by the large extent. Transistor count is reduced by using MTGDI technique hence chip area is optimized.

REFERENCES

1. A.Mitra; A.Bakshi; B.Sharma; N.Didwania" Design of a High Speed Adder" International journal of Scientific & Engineering Research, 2015.
2. Abba, Akhila; K.Amarendar" Improved Power Gating Technique for Leakage Power Reduction", IJES, 2014.
3. B.Ramkumar; Kittur; M, Harish" Low Power and Area-Efficient carry select adder, IEEE Transactions on Very Large Scale Integration Systems,2012.
4. Kumre, Laxmi; Ajay.S, Ganga agnihotry" Analysis of GDI technique for Digital circuit Design, International journal of Computer Applications, 2013.
5. Liu, Feng; Song, Xiaoyu; Tan, Qingping; Chen, Gang" Formal Analysis of Hybrid Prefix/Carry -Select Arthimetic Systems. The Computer Journal, 2011.
6. Morgenshtein, Arkadiy; Isreal, and Alexander Fish" Gate-Diffusion Input (GDI)-A Technique for Low Power Design of Digital Circuits: Analysis and Characterization", IEEE, 2000.
7. Sangeetha Parshionikar, Dr Deepak V.Bhior" Leakage Power Reduction Using Multi Threshold CMOS Technique", IJSER, 2013.
8. Verma, Pooja; Machandana, Rachna" Review Of Various GDI for Low Power Digital Circuits", IJAETAE, 2014.

9. Y.Wang; C.Pai; X.Song" The Design of Hybrid Carry Select Adder", IEEE Transactions on Circuits and Systems: Analog and Digital Signal Processing, 2012.
10. Saxena, Pallavi; Purohit, Urvashi; Joshi, Priyanka" Analysis of Low Power, Area Efficient and High speed Fast Adder", International Journal of Advanced Research on Computer and Communication Engineering, 2013.
11. Kiat-Seng Yeo, Kaushik Roy, "Low-Voltage, Low-Power VLSI Subsystems", Indian edition.
12. A. P. Chandrakasan, R. W. Brodersen, "Minimizing Power Consumption in Digital CMOS Circuits", Proceedings of the IEEE, vol. 83, no. 4, pp. 498-523, April 1995.

AUTHORS PROFILE

Tulasi Radhika Patnala is pursuing Master's degree in VLSI design in the Dept. of ECE, GRIET, Hyderabad. She has 4 years industry experience as UI Developer. Her area of interest includes Low power VLSI design and Mixed signal design.

Sankararao Majji is working as Assistant Professor in the Dept. of ECE, GRIET, Hyderabad. He has a teaching experience of about 5 years. He has presented papers in several International & National conferences. His research interests are Low power VLSI design, Analog design and mixed signal design.

Gopala Krishna Pasumarthi is working as Dean of Publicity & Alumni Affairs & Associate Professor in the Dept. of IT, GRIET, Hyderabad. He has a teaching experience of about 15 years in various prominent educational institutes. He has presented & published papers in several International & National conferences & Journals.