Implementation of Controller Structures in FPGA Platform

S Meena, K.Chitra, T Ramkumar, G Richie Roberts

Abstract: *Field Programmable Gate Arrays are recently replacing general purpose microcontrollers in implementation of digital control systems. This paper includes the proposal of implementing complex controller structures in a Field Programmable Gate Array (FPGA). Till recent, PID controllers are implemented in FPGA Platform. PID controllers are simple, reliable, versatile feedback mechanisms used in most control systems. To reduce various undesirable effects on the output such as overshoot, some variants in the conventional PID controllers, such as the I-PD and IMC are also used. Here all these control controller structures are implemented in MATLAB, compared for best performance and run in the FPGA.*

Index Terms: PID controller, I-PD controller, IMC controller, FPGA, Xilinx ISE 14.7 Design tools.

I. INTRODUCTION

FPGA-based controllers are widely used for their elevated speed, power efficiency and advanced functions. Digital feedback systems like magnetic bearings, PWM inverters, induction motors, AC/DC converters, variable-speed drives, and anti-windup compensation of controllers are already in use in FPGA Platform. FPGA-based platforms can do concurrent operations. Hence, simultaneous design of digital controllers can be made.
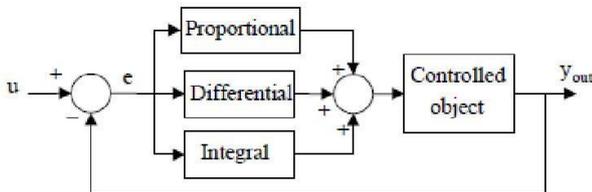

Fig 1.1 PID Controller

A PID controller evaluates the difference between a fixed set point and the process variable and computes the error values. By using a manipulated variable, which is proportional to the computed error signal the PID controller controls the output of a system thereby minimizing the error[2].
Proportional along with integral and derivative values is involved in a PID controller. They are denoted as simply P,I and D. In aspects of time, these can be understood that P is based on the present error, I is based on already available errors and D anticipates any probable future occurrence of errors, based on present behaviour[2]. With these three actions the final control element such as opening or closing valves, damper, or the amount of power supply, etc.,

Previously, the implementation of FPGA was based on the usage of numerous multipliers and adders and was not focused on optimized usage of hardware and hence was not efficient. It required a numerous multipliers and adders. In the old multiplier-based controllers the blocks take up to 64% usage of the chip.

A new idea of implementing the I-PD and also IMC control structures in an FPGA. It is made into application after passing through these general phases: 1) Software Modelling Phase where the design of digital control systems is carried out in software like Matlab / Simulink, 2) Hardware Implementation, to obtain real-time observation. Using modules, the design can be ported into environments such as the Matlab / Simulink, thus greatly reducing the developing time for designers.

The Integral – Proportional and Differential controller is an improvisation of a PID controller which is developed so as to minimize the effect of sudden change in the set point on the controller output. Internal Model Control (IMC) provides a procedure for design in accordance with many modern control techniques, the Q-parameterization concept. This made IMC controllers particularly popular in all industrial applications. Also, the IMC showed greater performance than all controllers. This showed greatly reduced oscillations than the conventional models of controller structures.
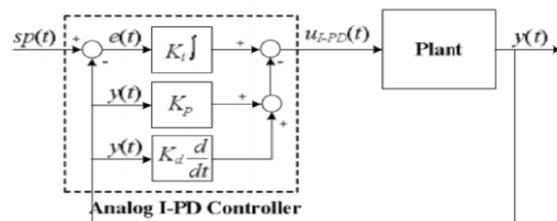

Fig 1.2 I-PD controller

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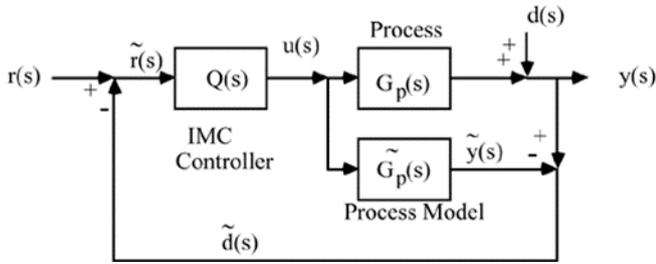

Fig 1.3 IMC Controller

IMC is also helpful in assessing the fundamental necessities associated with feedback control, such as determination of the effect of non-minimum phase elements on achievable control performance. Since the complication of the IMC controller depends on which order the model belongs to, and other performance requirements, the IMC design procedure is helpful in determining when simple feedback control structures (such as PID controllers) are enough.

II. IMPLEMENTATION OF TEST FUNCTIONS IN MATLAB

The two processes considered for analysis are stable second order and a boiler drum level process. Both the processes are tested with the various structures such as PID, I-PD and IMC based PID. The time domain specifications and the performance indices are compared and the optimized values are identified.

2.(a). Example 1:

A stable second order system is considered.

$$y1 = \frac{2e^{-1s}}{50s^2+15s+1} \qquad (1)$$

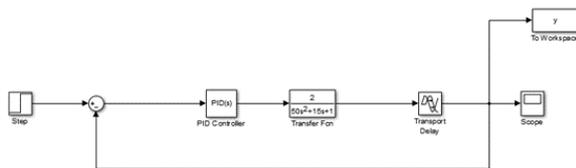The above said process is implemented in all PID, I-PD and IMC control structures.

Fig 1.4 Simulink of T.F 1

The performance measures are tabulated in the table 1.1 and the corresponding responses are are given in fig 1.5 .

y1	PARAMETERS	PID	I-PD	IMC PID
	RISETIME	34.6728	220.9701	283.0108
	PEAK TIME	111	971	1001
$\frac{2*e^{-s}}{(10s+1)(5s+1)}$	SETTLING TIME	423.6338	431.0857	532.4004
	ISE	9.1919	8.598	12.8209
	IAE	15.4481	12.89	25.5214
	ITAE	232.7793	138.3	663.0983

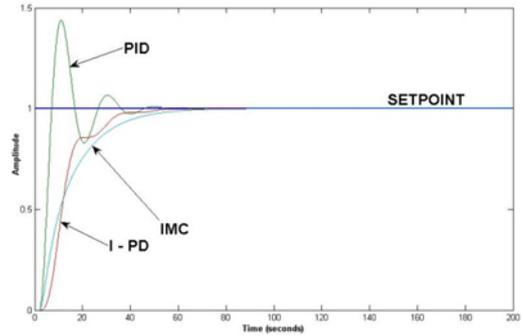**Table 1.1 Parameters of response**

Fig 1.5 Responses of PID, I-PD and IMC

For the example transfer function-1 taken, it is inferred that the IMC control strategy is more optimised comparing with the other control strategies.

III. IMPLEMENTATION OF REALTIME PROCESS

For research purposes, a two-tank interacting system commonly used in food processing industries to obtain accurate proportions of mixture is taken. To understand the effect of interaction, we have considered a two-tank system in experiment. The second tank affects the rate of change of level in first tank and vice-versa. The flow through R1 depends on the difference between h1 and h2. The analysis started by writing mass balance on the tank. Both the balances of the tanks are the same. The flow head relationship for tank 1 is $q_2 = (h_1-h_2)/R_1$

The mass balance equation of tank 1 is
$$(q_1 - q_2) = A_1.\frac{dh_1}{dt} \qquad (2)$$
And for tank 2,
$$(q_2 - q_3) = A_2.\frac{dh_2}{dt} \qquad (3)$$
The flow head relationships for the two linear resistances are $q_2 = \frac{h_1}{R_1}$ and $q_3 = \frac{h_2}{R_2}$ (5)

At steady state, the flow equation is $(q_{1s} - q_{2s}) = 0$, $(q_{2s} - q_{3s}) = 0$. (6)

By solving all the above equations using Laplace transform, the transfer function can be written as,

$$\frac{H_2(s)}{Q_1(s)} = \frac{R_2}{(\tau_1\tau_2 S^2+1(\tau_1+\tau_2+A_1R_2)S+1)} \qquad (7)$$

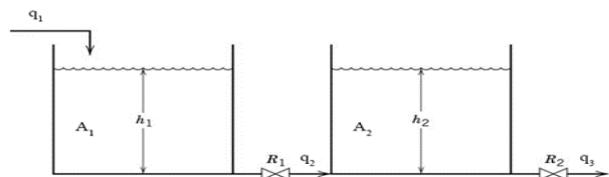**Experimental Setup : Two tank interacting system**

Fig 1.8 Two-tank Interacting System

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By substituting the calculated values from the observed data, equation 7 can be written as the overall transfer function and is given by,

$$\frac{H_2(s)}{Q_1(s)} = \frac{0.0462}{25.28S^2 + 14.5363S + 1}$$

(8)

A. IMPLEMENTATION IN MATLAB

The below transfer function which is obtained for two-tank interacting system is taken.

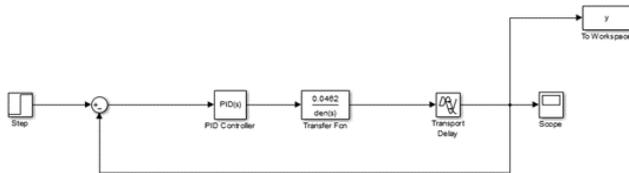$$T.F = \frac{0.0462}{25.28S^2 + 14.5363S + 1}$$

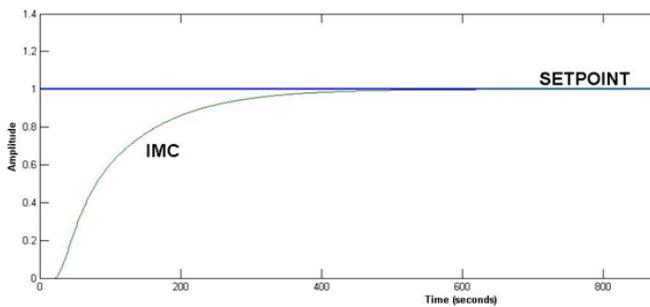**Fig 1.9 Simulink of IMC for Two-tank Interacting System**

Fig 1.10 Response of IMC

B. IMPLEMENTATION IN FPGA

FPGA software and hardware integration

FPGAs are supported by development software which convert hardware designs into programming bits which determine the actions of interconnects and Configurable Logic Blocks. The ISE Design Suite Embedded Development Kit includes <u>Platform Studio</u> (XPS), <u>Development Kit</u> (SDK), plug and play IP s.
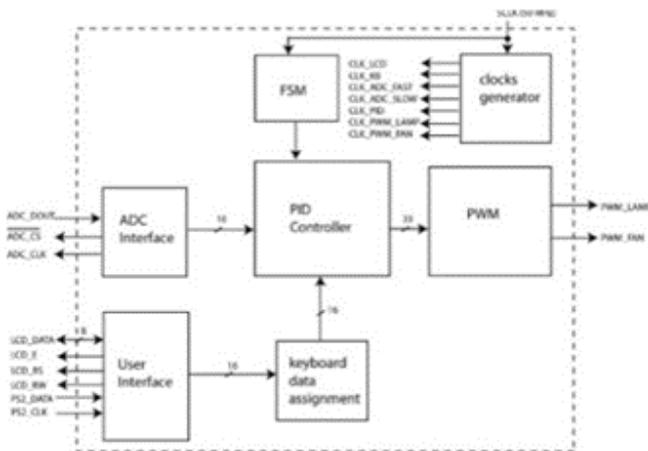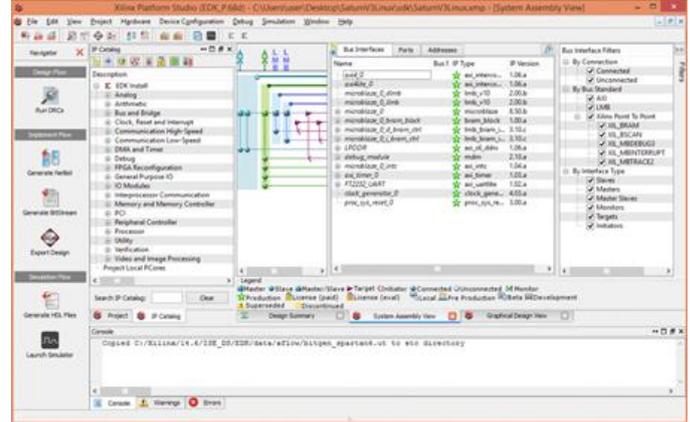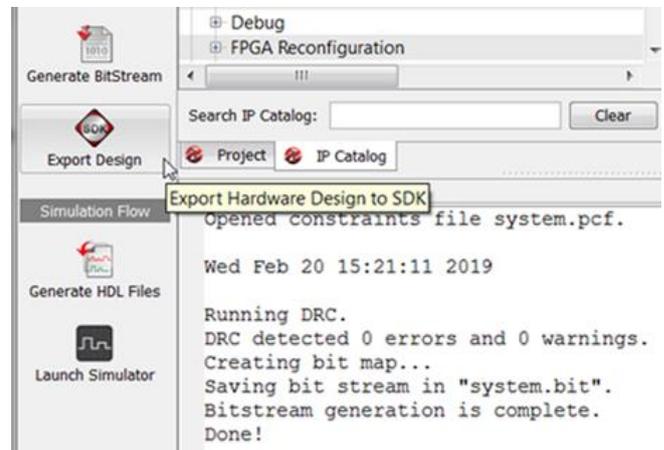

Fig 1 .11 Hardware Architecture of FPGA

The Xilinx Software Development Kit (SDK), which is a Development Environment (IDE), used for embedded software applications.

Parallel design of Hardware platform with software development is facilitated. SDK update of hardware platform specification when pointed to a different version is also supported.
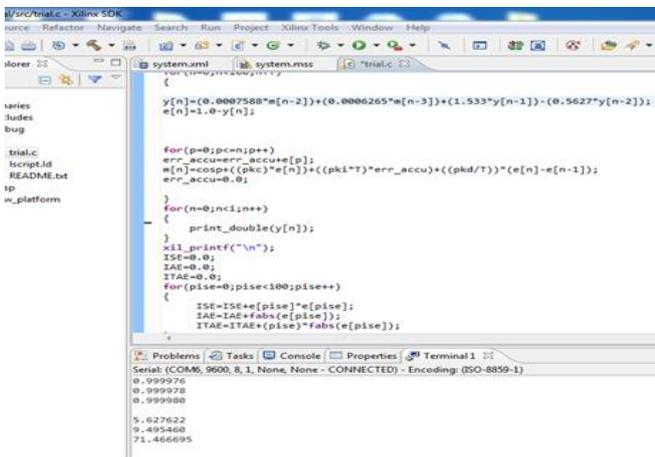

The information for FPGA is programmed as bitstream and the hardware designer provides bitstream and it has been generated in the embedded platform .Programming is the integrating a bitstream into FPGA. In this phase, the FPGA programming is carried out using menu options in SDK, transfering the bitstream to the FPGA.The non-volatile memory has bitstream , and hardware will program FPGA when turned on.

Programming the FPGA

- Select **Xilinx Tools > Program FPGA**.
- **Bitstream** and **BMM File** will be filled by itself. If necessary, those files need to be specified to upload bitstream to the FPGA
- SDK finds processors, automatically. In **Software Configuration,** select the executable (.elf) file.
  select **BootLoop** from drop-down menu or **Browse** any ELF file.
- Click **Program.**

Thus the real time process which was implemented in MATLAB has been converted into FPGA compatible language, integrated with XPS (Xilinx Platform Studio) & implemented SDK (Software Development Kit) of FPGA platform. Thus the real time process which was implemented in MATLAB has been converted into FPGA compatible language, integrated with XPS (Xilinx Platform Studio) & implemented SDK (Software Development Kit) of FPGA platform.

IV. CONCLUSION

For research purposes, we have taken two test transfer functions and they were successfully implemented in MATLAB for PID, I-PD and IMC control. And it is inferred from the experiments that the IMC control strategy provides better results than other controllers such as lesser rise time, lesser peak time, lesser settling time and lower overshoot. Therefore, The IMC control strategy was taken and implemented for any industrial process (Two-tank interacting system) in FPGA platform successfully. It is also inferred that we can obtain higher quality solution with better computational efficiency in FPGA

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AUTHORS PROFILE

Mrs. S Meena has completed her B.E in National Engineering College, Kovilpatti and her M.E from Sathyabama University with specialization in Electronics & Control. She has 13 years of experience in teaching. Her areas of research are Process control and embedded systems.

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