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Design and Evaluation of Ultra Gain Isolated DC-DC Converter for Photovoltaic System

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Abstract*: *New single switching device converter is proposed here for extracting maximum power from multiple PV array configurations with an isolated output port. It is capable to extract maximum electrical energy from serial, parallel connected PV modules. Equivalent circuit model is derived for serial and parallel connected solar PV cell with different internal performance parameters. Different PV configuration with identical and non-identical modules is analysed. Improved P&O algorithm is developed for the proposed System. A prototype model is designed with C2000 DSP controller; a control algorithm realized in it to validate the proposed converter. Experimental results are compared with theoretical results, and its performance shows superiority of the proposed system.

Index Terms*: *Series and Parallel Connected PV array; MPPT algorithms; High gain DC to DC converter.

I. INTRODUCTION

Standalone renewable energy system has been used to fulfil the rural area power requirement. Researchers are more concentrating on improving the efficiency and reliability of energy conversion, Storage and utilization system. Photovoltaic Modules (PVM) are major dominating to provide energy needs in the standalone system. Many industry and domestic loads need alternating current (AC), but unfortunately, major renewable generation systems are generating variable direct current (DC).The drawback of the PVM system is high capital cost and low energy conversion efficiency. Well designed, DC/DC and DC/AC converters provide better efficiency and reliability. The efficiency of the converter depends on a number of switching devices, passive components, and the conversion stage.PVM system output current depends on solar irradiation level and voltage with module temperature. The main drawback of the PVM system is the temperature and light intensity variable on climatic conditions. Maximum Power Point Tracking (MPPT) is used to extract maximum power from PVM. Voltage and Current characteristics of PVM are discussed with their mathematical model [1, 2].Properly connected circuit's components like bypass diode, etc. can avoid partially shaded serially connected solar PVMs hot-spot phenomena caused due do unequal current [3]. Voltage, Current and Power rating of PVM's is based on the physical property of manufacturing materials. Modelling of PVM with physical property is used to find the PVM parameters without complex calculations [4]. PVMs are connected series and parallel to improve the power rating. The different structure of converter is available for solar power generation, most of the system used individual boost converter for each PVM. The existing system directly affects the cost and efficiency with a complex control algorithm [5-11]. Some converters achieve high efficiency using complex algorithms .PV system should operate in maximum power point to improve the efficiency of PVM. Many MPPT algorithms are used in the industry based on applications and control variable. Perturb and Observe algorithm is used here due to advantages over the MPPT's. The proposed high gain DC-DC converter is shown in Figure 1.1. An isolated converter is introduced for better MPPT in Parallel PV system and efficiency enhancement. A proposed converter having only one switch, the serial and parallel combination of PVM is connected through the inductor. Real time parameters of proposed converters like Vmpp, Impp, and Pmpp of PV modules are analysed to vary the duty cycle to develop good MPPT. This paper is organised as follows. System configuration and operational principle of proposed converters analysed in Section-II, Serial and parallel-connected PVM equivalent parameters are analysed in Section-III. Section -IV present a design consideration of proposed converter. MPPT algorithm for serial and parallel PV configuration is discussed in Section-V, Hardware realization is deliberated in section-VI and valid remarks are given in section-VII.

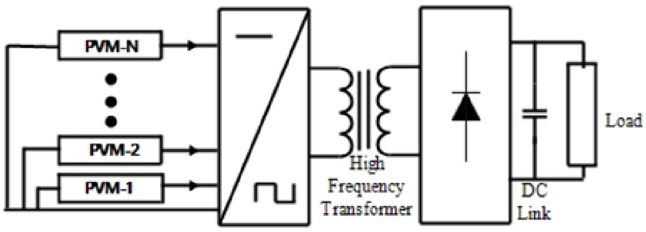

Figure1.1. Block Diagram of Proposed Ultra Gain Isolated DC-DC Converter

II. SYSTEM CONFIGURATION AND OPERATING MODES

The proposed Ultra gain isolated DC-DC converter is revealed in Figure 2.1. PVM is connected in primary of high frequency transformer through boost converter and buffer capacitor C_B. DC Load is connected secondary of the transformer through the rectifier. Transformers core is made by ferrite core for high frequency operation.

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The turns ratio of the transformer is defined by n=Ns/Np, where Ns is a number of secondary chances and Np is a number of primary chances. C_B acts as a buffer capacitor, it store energy in state-I operation and release in state-II operation, C_B is charged and discharged frequently to make bi-directional current flow in primary of the transformer. PVM is associated to primary of the transformer through boost inductor L_1, Reverse blocking diode $D_1$is prevents reverse current flow through PVM. C_1 is source side capacitor, it is used to store the PVM harvested energy in State-II and smoothening the solar PV voltage from random variation. Two states of operation possible in the proposed converter. The equivalent circuits of operating State-1 and State-2 are shown in Figure 2.2(a) and Figure 2.2(b).State-1 operation covers the period with switch S is ON. The correspondent circuit of State-I operation is exposed in Figure 2.2. State-2 operation covers the period with switch S is OFF.

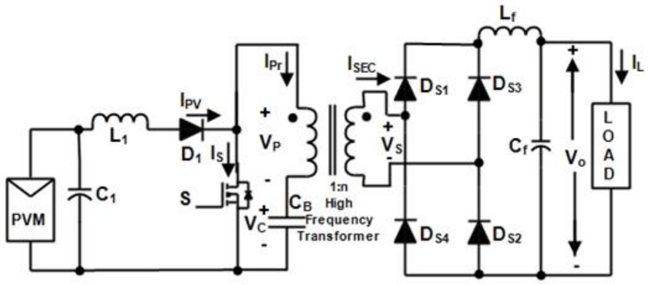

Figure.2.1 Circuit Configuration of Proposed Single Switch Isolated DC-DC Converter

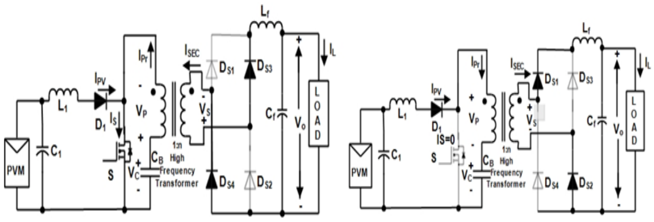

Figure.2.2 Equivalent Circuit of operating States. (a) Operating States-1 (b) Operating State-2

2.1 State-1 Boost Operation (t_0<ts<t_1) During this operating state, the switch S is ON at t=t_0, PVM transfer harvested power to respective inductor L_1. Buffer capacitor C_B with stowed energy in the previous cycle is removed to load through high frequency transformer. The voltage across C_B appears as transformer primary voltage. The voltage across the primary (V_P) and current flowing through the primary (I_P) of Transformer are negative. Transformer secondary side Diodes D_{S3} and D_{S4} are forward bias and transfer secondary power to load through Lf and Cf. The current through the switch is equal to the sum of PVM (I_{PVM}) current and High Frequency Transformer (HFT) primary current.

2.2 State-2 Energy Transfer Operation (t1<ts<t2) During this operation state, the switch S is turned OFF at t=t1, PVM_1, PVM_2...PVM_N currents are flowing through respective inductors L_1, Primary of transformer and Buffer capacitor C_B. Part of the energy transferred to load through the transformer and remaining energy stored in C_B for next cycle. The sum of the voltage across PVM and Boost inductor L_1appears across primary of transformer and C_B. V_P and I_P are positive. High frequency transformer secondary side diode D_{S1} and D_{S2} are forward bias and transfer secondary power to load. No current flowing through switchS.

III. HIGH GAIN ISOLATED CONVERTER FOR SERIES AND PARALLEL CONNECTED PVM

Normally same power and output voltage PVMs are used to make inter connections to achieve desired output power and voltage. Based on the voltage and power rating of PVM, six different PVM interconnections are possible. They are identical power and voltage rated PVM in series and parallel, Different power and identical voltage rated PVM in Parallel and series, Different and power voltage rated PVM in series and parallel. Normally same power and voltage rated PVM in series and parallel configuration is preferred for the classical converter to achieve the desired output. In addition with the same power and voltage rated PVM in series and parallel configuration, projected converter is accomplished of achieving high efficiency, High gain and MPPT in different power and voltage rated PVM parallel configuration

Identical voltage and power PVMs are connected in the proposed converter is shown in Figure 3.1. Reverse blocking diode (D_1, D_2...D_N) is used to avoid circulating current between PVMs. The buffer capacitor (C_1, C_2...C_N) is connected parallel with each PVM to avoid power fluctuation due to sudden environmental changes and partially shadow conditions. In instruction to decrease the cost of the proposed system and increase the effectiveness, single boost inductor (L) is used. The design of the basic components explained in Section 5.

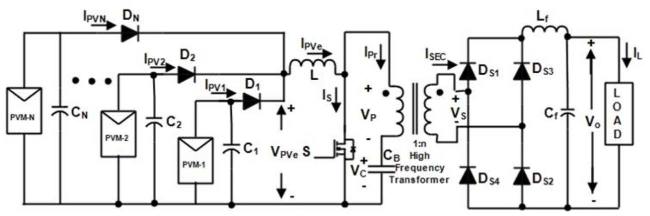

Fig.3.1 Proposed topology for Identical PVMs are connected in Parallel

Identical PVMs are associated in series with a proposed converter is publicized in Figure 3.2.Identical PVMs are having the same current and equal to *IPVe.* During the absence of irradiation, reverse blocking diode (D) is blocking the reverse current flowing through PVMs. Single boost inductor (L) is used.The bypass diodes (DBY_1-DBY_N) are connected with serially connected PVMs to prevent the currents flow from good, well unprotected to sunlight solar PVMs burning and overheating out partially shaded solar PVMs by providing a current path around the bad PVM. Bypass diodes in solar modules are associated in parallel and reverse bias with PVMs to bypass the current init. Whereas blocking diode (D) is associated in series with the PVMs to precludereturn current flow.

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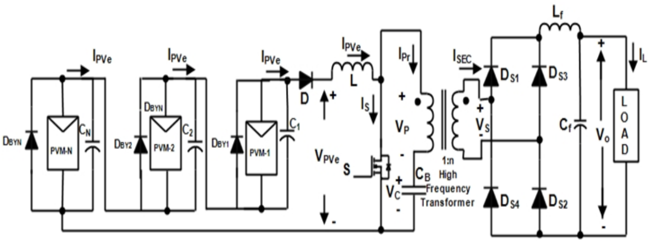

Fig.3.2 Identical PVMs are connected in Serial

The circuit configuration of different rated PVMs are associated in parallel with a proposed converter is shown in Figure 3.3.Each PVM having different voltage and power rating. Different boost inductor (L_1, L_2...L_N) are used to interconnect with a single switch. The resultant PVMs output voltage (VPVMe) is equal to the algebraic sum of individual PVM voltages. Total output power (PPVMe) is equal to the summation of individual PVM power.

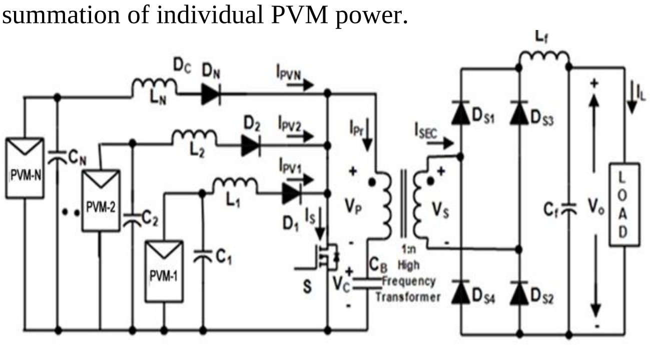

Figure 3.3 Different Rated voltage and Power PVMs are connected in Parallel

IV. MPPT FOR HIGH GAIN ISOLATED CONVERTER WITH SERIAL AND PARALLEL PVM CONFIGURATION

PV module output voltage VPVMe and current IPVMe are dignified to develop P&O MPPT algorithm for serial and parallel connected PV system. MPPT tracing is achieved by varying duty cycle. Dual operation with a single switch is performed in a proposed converter. The flow chart for MPPT algorithm is shown in Figure 4.1.The input of the algorithm is the Minimum value of duty cycle (Dmin), Maximum value of duty cycle (Dmax) and duty cycle step (ΔD). Value of duty cycle is calculated based on the passive components of the projected converter.

Normally P&O algorithm is continuously tracing maximum power point. The algorithm is structured based on iteration. Each iteration compare power in current iteration (nth iteration) with previous iteration (n-1 iteration) power and voltage, based on the error ΔD is adding or subtracting with nth iteration duty cycle. Low and High value of duty cycle directly affects the power transfer to load in State-I and State-II operation.

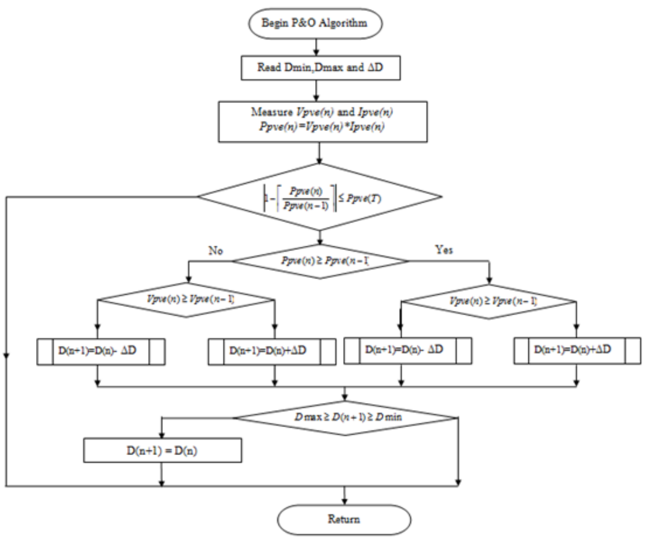

Figure 4.1 Proposed MPPT P&O algorithm flow chart

V. DESIGN CONSIDERATION

In The basic components design of a converter is very important to achieve high efficiency and reliability. These include PV module connection configuration, turns radio of transformer, inductor L, L_1, L_2...L_N, Buffer Capacitor C_B, Lf, and Cf.PV module configuration is selected based on PVMs output voltage and current ratings.. Series and parallel PVMconfiguration reduced series inductor to one and L is selected Thevenin's equivalent of L_1, L_2...L_N.L and C value are reduced significantly based on the highswitching frequency of the converter. High frequency ferrite core transformer with transformation ratio n is used to avoid saturation effect.

PV output voltage (V_{PVM1},V_{PVM2}...V_{PVM}m and V_{PVM}e) ,output current (I_{PVM1},I_{PVM2}...I_{PVMM} and I_{PVMe}),switching frequency(fs) and duty radio (Ds) are considered to calculate L_1,L_2,L_3,....L_m and C_1,C_2,C_3,....C_m.

The series inductor

$$L_M = \frac{(V_{PVMM}.D_S)}{(f_S.\Delta I_{PVMM})} Hentry \;\; (Where \;\; M = 1, 2, 3...N) \tag{1}$$

Ripple current

$$\Delta I_{PVMM} = C_M \frac{(\Delta V_{PVMM})}{(D_M.T_S)} Amps \;\; (Where \;\; M = 1, 2, 3...N) \tag{2}$$

And parallel capacitor

$$C_M = \frac{(\Delta I_{PVMM}.D_M.T_S)}{(\Delta V_{PVMM})} = \frac{(\Delta I_{PVMM}.D_M)}{(f_S.\Delta V_{PVMM})} Farad \;\; (Where \;\; M = 1, 2, 3...N) \tag{3}$$

Buffer capacitor Cb has stored energy in half of the cycle and released. All PV energy is accumulated in C_B. During the state-II operation, all the source current is flowing through capacitor C_B.

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Current in buffer capacitor

$$I_B = \sum_{M=1}^{N} I_M \ \ Amps \tag{4}$$

And Buffer capacitor

$$C_B = \frac{\sum_{M=1}^{N} I_{PVMM}(1-D_S)}{f_S \Delta V_{CS}} \ \ F \tag{5}$$

Secondary inductor Lf and Cf are based on the output voltage (V_O) and current (Io). Lf and Cf are used to reduce the voltage ripple.

The voltage across inductor Lf is

$$V_{Lf} \approx Vs - Vo = (V_P * n - V_{dc}) \tag{6}$$

$$L_f \approx V_{Lf} * \frac{D1.Ts}{\Delta I_f} = \frac{(V_P * n - V_{dc}) * D_S}{f_S * \Delta I_f} \ \ H$$

Filter Inductor (7)

Lmin is calculated using the lowest value of Ds and L is selected greater than Lmin.

Filter Capacitor

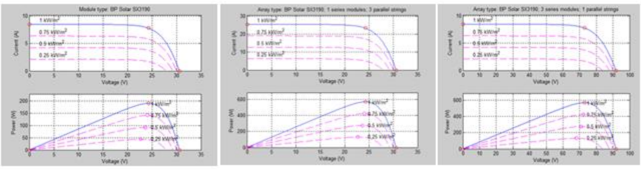
$$C_f \approx I_{Cf} * \frac{D1.Ts}{\Delta V_f} = \frac{\Delta I_O * D_S}{f_S * \Delta V_f} \ \ F \tag{8}$$

Cf value is calculated using the maximum value of Ds.

During State-I operation, the current flowin the Switch S is near twice the total source current. Switch S is selected for the higher value of twice the source current and rated source voltage.

VI. RESULTS AND DISCUSSION

Based on the design and analysis of previous sections, proposed converter MATLAB simulation and experimental was done and results are validated for Series and parallel configuration equivalent circuit model with proposed convert. Figure 6.1 shows V-I characteristics of BP Solar SX3190 model with different connection configuration. The rated output power, current and voltage of each model at Maximum power is 24.3 Volts,7.83 Amps, and 190 Watts. Figure 6.1(a) shows V-I characteristics of single PVM. Figure 4.1(b) and Figure 4.1(c) are shows V-I characteristics of1 series and 3 parallel PVM and 3 series and 1parallel PVM.V-I Characteristics curve clearly shows output voltage and current of each PVM array is equal to V_{PVMe} and I_{PVMe}.



a b c

(a) Figure 6.1 V-I Characteristics of BP Solar SX3190 model (a) Single Module (b) 1 Series and 3 Parallel Module (c) 3 Series and 1 Parallel Module

MATLAB Simulation is carried out with 3500 watts resistive load. BP Solar SX3190 PVM model (3 series and 7 parallel connected PVM, 72 Vmpp, 4000 Watts), turns radio of High Frequency transformer is 10 and 144mH boost inductor are used. Results are shown in Figure6.2 (a-f) solar input power and output power are shown in Figure 6.2 (a). During the transient period Buffer capacitor store energy and voltage across the capacitor are varying with reverence to time and reach stable state value is shown in Figure 6.2 (b). During the on time of switch 'S' buffer capacitor voltage is appeared across primary of the high frequency transformer and Vp is negative. During the negative half cycle, the voltage diagonally the buffer capacitor only desired the output voltage. During the period of 'S' is off, the PVMs energy is transferred to buffer capacitor through primary of the transformer and PVMs voltage appeared across primary of transformer and capacitor. During S off, the Vp is positive. Vp is shown in Figure6.2 (c) and Secondary voltage shown in Figure6.3(d).PV input voltage and load voltage is shown in Figure6.2(e), during the transient period, PVM voltage is reached steady state, when the capacitor voltage reaches to a maximum. Percentage of duty ratio shown in Figure 6.2 (f). The duty ratio D is based on PVM output power using proposed P&O algorithm to achieve MPPT. The minimum and maximum value of D is varying between0.4 to 0.7. Initially load consuming low power and a duty ratio of S is desired lower range. Minimum and maximum values of D are fixed to get stable output voltage. During the normal load, condition D is reach up to 70%.

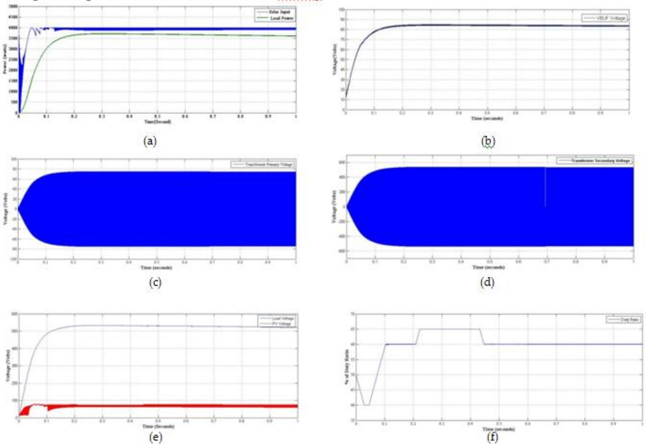


Fig.6.2(a) Input Power and Output Power (b) Buffer Capacitor Voltage (c) HFT Primary Voltage (d) HFT Secondary Voltage (e) PV and Load Voltage (f) MPPT Duty Ratio

Parallel connection of nonidentical voltage and power rated PVM results are shown inFigure 7.4. Three sets of serially connected Kyocera KD135GX-LP PVM model is connected with four sets of serially connected BP Solar SX3190 PVM model.

Kyocera KD135GX-LP model having Vmpp is equal to 17.7 V, Impp Value is 7.62959A and power rating of each module at maximum power point is 135 Watts. TotalVmpp, Impp are equal to 53.1V and 22.88 A. Bp Solar SX3190 model having Vmpp is equal to 24.3 V, Impp Value is 7.82945A and power rating of each module at maximum power point is 190 Watts. Total Vmpp, Impp are equal to 72.9V and 31.32 A. Kyocera KD135GX-LP Model connected to switch S through 200mH inductor and Bp Solar SX3190 connected to switch S through 300 mH inductor.

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Inductors values are calculated using Equation (14) using the values of Switching frequency is equal to 50KHz and Change in PVM current is equal to 3 Amps. PVMs are capable to generate up to 3500Watts power.

Input and output powers of converters are shown in Figure 6.4 (a). PVM_1 and PVM_2 are sharing the load power. The sharing power is comparative to Vmpp. When the load is operated by a full load, PVM_1 and PVM_2 are feed the maximum power. Figure 6.4 (b) shows PVM_1 and PVM_2 current. The currents are identical in nature and proportional to the Impp. The currents are equal to Impp of individual PVM. When the PVM_1 and PVM_2 are feed maximum power, Current in PVM_1 and PVM_2 are equal to Impp of individual PVM. MPPT duty ratio is shown in Figure 6.4 (c), the Duty ratio is fixed at 0.6 by Modified P&O for extracting maximum power from PVM1 and PVM2.Figure 6.4 (d) shows the output voltage of the projected converter. A constant output voltage is maintaining across a load.

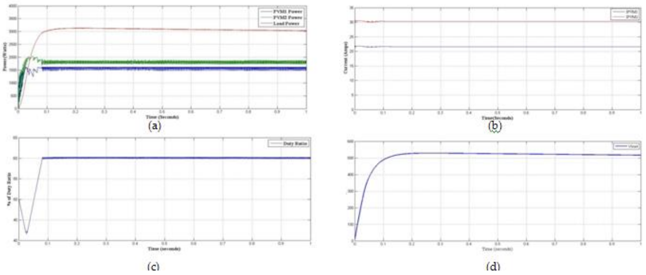


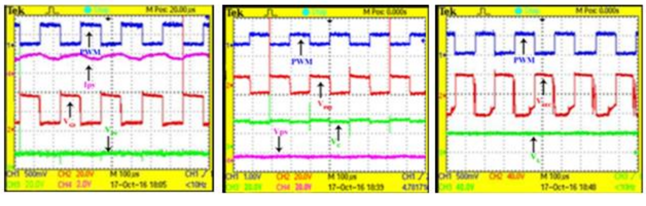
Figure 6.4 (a) Input Power and Output Power (b) PVM1 and PVM2 Current (c) Load Voltage (d) MPPT Duty Ratio

Reduced rated experimental setup is made with C2000 DSP controller with necessary hardware components listed in Table 6.1 for validate proposed converter. The results are shown in Figure 6.3.

Table.6.1 Hardware components and its ratings

S.No	Particulars	IC name/Value
1.	MOSFET	IRF P 250N
2.	Gate Driver	TLP250
3.	Capacitor (C1)	420uF, 36 Volts
4.	Inductor (L)	10mH
5.	HF Transformer	N1:N2=1:10
6.	Capacitor (Cb)	1000 µF, 64 Volts
7.	PV Module	12V, 120 Watts
8.	Diode D1, Ds1-Ds4	FR304 MC
9.	Load Resistance R_L	50 Ohms
10.	Switching Frequency	5 KHz

Input PVM voltage (Vpvm),PV current (Ipvm),MOSFET Gate-Source Voltage V_{GS} and PWM signal are shown in Figure 6.3. PWM pulse is produced in C2000 microcontroller and applied to TLP250 MOSFET driver.TLP 250 MOSFET driver is having inbuilt isolation and driver circuit. PWM signalsfrom the C2000 controller is inverted and fed to TLP250.Isolated DC voltage is applied across gate and source voltage (V_{GS}) and it is controlled through TLP250...PWM signal,PVM current I_{PV}, PVM voltage $V_{PV}$and voltage across gate and source (V_{GS}) are shown in Figure 6.3 (a).It shows that the voltage and current of PVM is stable. StableHigh Frequency transformer primary Voltage (V_{PRI}) and Voltage across buffer capacitor (V_C) and PV input voltages are shown in Figure 6.3 (b)V_{PRI} is a square wave in nature due to V_{PV} and V_C appeared across it. When S is On V_{PRI} is positive and S is OFF, V_{PRI} is negative.V_C is provided a major contribution to the stable output voltage and its allowable voltage variation of V_C is less than 2% of total voltage across it. Vpv is stable for continuous operation. High frequency transformer secondary voltage (VSEC) and Load voltage (VL) is shown in Fig.6.3 (c).V_{SEC} is identical to V_{PRI} and rectified secondary voltage has appeared across load VL.



(a) (b) (c)

Fig.6.3 Experimental Result of Proposed Converter (a) PVM voltage, PVM Current, VGS and PWM signal (b) HF Transformer Primary Voltage, Voltage across the Capacitor (Vc)(c) HF Transformer Secondary and Load Voltage

VII. CONCLUSION

A high gain isolated multiport DC-DC converter for multiple PV array configuration has been proposed with a single switch for extracting power. Improved P&O MPPT control technique is used to achieve better MPPT tracking. Simulation outcomes are shown based on the operation of the proposed converter. Texas Instrument C2000 DSP controller based prototype is developed to validate the suggested converter. Experimental results are confirmed with its simulation outcomes. The proposed high ultra gain DC-DC converter is simple topology, a good MPPT tackling, and high voltage gain with electrical isolation.

REFERENCES

1. 1.Y. Mahmoud, W. Xiao, and H. H. Zeineldin, “A Simple Approach to Modeling and Simulation of Photovoltaic Modules,” IEEE Transaction of Sustain Energy, vol. 3, no. 1, pp. 185-186, Jan. 2012.
2. 2.Li Hong Idris Lim; Zhen Ye; Jiaying Ye; Dazhi Yang; Hui Du "A Linear Identification of Diode Models from Single I– V Characteristics of PV Panels "IEEE Transactions on Industrial Electronics, Vol: 62, issue: 7, pp: 4181 – 4193, July 2015.
3. 3. A. Bidram, A. Davoudi, and R. S. Balog, “Control and Circuit Techniques to Mitigate Partial Shading Effects in Photovoltaic Arrays,” IEEE J. Photovolt., vol. 2, no. 4, pp. 532-546, Oct. 2012.
4. 4. Shah Arifur Rahman, Rajiv K. Varma and Tim Vanderheide “Generalised model of a photovoltaic panel” IET Renewable Power Generation, 2014, Vol. 8, Iss. 3, pp. 217–229
5. 5. Jianwu Zeng, Wei Qiao Liyan Qu and Yanping Jiao "An Isolated Multiport DC-DC Converter for Simultaneous Power Management of Multiple Different Renewable Energy Sources" IEEE journal of emerging and selected topics in power electronics, vol. 2, no. 1, March 2014.
6. 6.Poornima Mazumdar, Prasad N. Enjeti and Robert S. Balog “Analysis and Design of Smart PV Modules” IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 2, Issue. 3, pp.451-459 Dec. 2013.
7. 7. Woo-Young Choi "High-Efficiency DC-DC Converter With Fast Dynamic Response for Low-Voltage Photovoltaic Sources" IEEE Transactions on Power Electronics, vol. 28, Issue. 2, pp.706-716 June. 2012.

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8. 8. Mohammed S. Agamy, Song Chi, Ahmed Elasser, Maja Harfman-Todorovic, Yan Jiang, Frank Mueller and Fengfeng Tao "A High-Power-Density DC-DC Converter for Distributed PV Architectures" IEEE Journal of Photovoltaics, vol. 3, Issue. 2, pp.791-798 Dec. 2012.
9. 9. Antoneta Iuliana Bratcu, Iulian Munteanu, Seddik Bacha, Damien Picault and Bertrand Raison "Cascaded DC-DC Converter Photovoltaic Systems: Power Optimization Issues" IEEE Transactions on Industrial Electronics, vol. 58, Issue. 2, pp.403-411 Feb. 2010.
10. 10. Dong Cao, Shuai Jiang, Xianhao Yu and Fang Zheng Peng "Low-Cost Semi-Z-source Inverter for Single-Phase Photovoltaic Systems" IEEE Transactions on Power Electronics, vol. 26, Issue. 12, pp.3514-3523 May 2011.
11. 11. Moumita Das and Vivek Agarwal "Novel High-Performance Stand-Alone Solar PV System With High-Gain High-Efficiency DC-DC Converter Power Stages" IEEE Transactions on Industry Applications, vol. 51, Issue. 6, pp. 4718-4728, Dec. 2015.

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