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Performance of MLGNR, SWCNT and Copper as Interconnects for Nanometer Technologies

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Abstract: Performance of multilayer graphene nanoribbon (MLGNR), single wall carbon nanotube (SWCNT), and copper as interconnects for different lengths at nanometer technologies (32nm, 22nm, and 16nm) for signal latency and product of power and delay(PDP) is presented. Impedance parameters of MLGNR are discussed by deducing its equivalent single conductor (ESC) model. It is discussed that resistance of MLGNR offers less compared to SWCNT and copper. The performance of MLGNR, SWCNT and copper is estimated with Tanner tool and a comparative investigation is done for the estimated performance of all the materials for signal delay and PDP for three different technologies. It is analyzed from outcomes that delay and PDP of all the three interconnects increases with increase in interconnect length from 500–2000µm for all the technologies. Further, it is also observed that delay and PDP of MLGNR is lesser in comparison to SWCNT and copper for each technology (32nm, 22nm, and 16nm).

Index Terms: Delay, Interconnect, MLGNR, Nanometer Technologies, PDP.

I. INTRODUCTION

Copper is widely used as interconnects in on-chip integrated circuits (ICs). However, with the advancement of technologies such as decrease in cross-sectional dimensions and increase in current density, copper face stuffy problems [1–3], which affects its overall conductivity. As a consequence, researchers are looking for an alternative material in contrast to copper. Carbon nanomaterials (Graphene nanoribbons and carbon nanotubes) are better alternative solution to conventional copper based on their electrical, mechanical, and thermal properties [4–6].

Carbon nanotube (CNT) is the cylindrical form of graphene whereas graphene nanoribbon (GNR) is considered as horizontal planer form sheet. GNR gain potential over CNT depending on its planar nature, controllability and easy fabrication technology [7–8]. Graphene nanoribbons are obtained by arranging graphene that is made of a thin sheet of carbon atoms and is used to structure the CNTs [9]. Based on the chirality, GNRs are classified into zig-zag (zz) GNR and armchair (ac) GNR. zz-GNRs exhibits metallic properties whereas ac-GNRs exhibits metallic as well as semiconducting properties [10]. Further, GNRs are separated into single layer GNR (SLGNR) and multilayer GNR (MLGNR), considering the significance of layers. It is also reported in literature that SLGNR has high resistance so MLGNR is proposed as VLSI interconnect material.[10]In this paper, the comparative analysis between MLGNR, single wall CNT (SWCNT), and copper interconnects from performance parameters (delay and PDP) for variable interconnect lengths for 32nm, 22nm, and 16nm technologies has been carried out. The paper has five sections: In Section II, circuit modeling of MLGNR has been presented. Section III, presents the parasitic of MLGNR, SWCNT, and copper interconnects. Section IV, presents the performance comparative analysis of interconnects for variable interconnect lengths at 32nm, 22nm and 16nm technologies. In Section V, outcomes of the paper are concluded.

II. ELECTRICAL MODELING OF THE MLGNR INTERCONNECT

In the current section, electrical modeling of MLGNR is discussed. Fig. 1 (a) shows the structure of SLGNR, where *w* signifies width and *d* signifies distance between the ground plane and GNR.

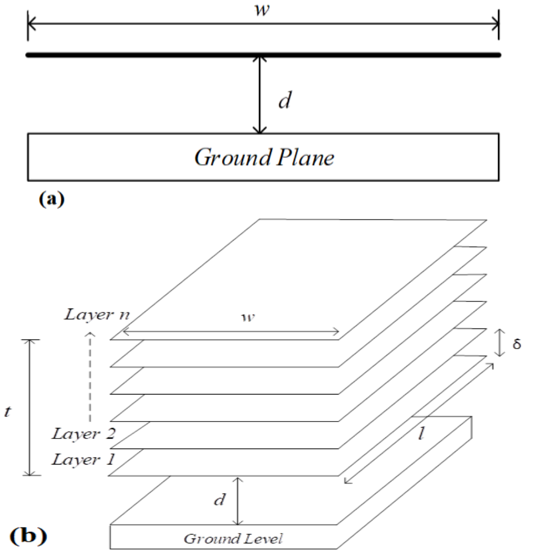

Fig. 1 (a) SLGNR (b) MLGNR bundle

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When GNRs are stacked one over the other as shown in Fig. 1 (b) constitute MLGNR bundle, where t signifies thickness and δ is the Van der Waal's spacing between the GNR layers. The MLGNR layers (n) in a bundle can be calculated as[10],

$$n = 1 + Integer\left[\frac{t}{\delta}\right] \tag{1}$$

Every layer of MLGNR consists of contact resistance (R_c), quantum resistance (R_q) and scattering resistance (r_s). The contact resistance has smaller value in few hundred ohms. The quantum resistance is there when GNR interconnect length (l) is not greater than its mean free path (λ_f) of electrons [10] and calculated by,

$$R_q = \frac{12.9}{N_{ch}} \ (\text{k}\Omega) \quad [l < \lambda_f] \tag{2}$$

where N_{ch} signifies the number of conducting channels of GNR and expressed as [10],

$$N_{ch} = \alpha w E_f \,, \qquad for\ w > 10\text{nm} \tag{3}$$

where E_f signifies Fermi energy and it should be greater than equal to 0.1eV. When the l of the GNR is greater than λ_f then the impact of scattering resistance (r_s) occurs and r_s calculated in per unit length (p.u.l) by,

$$r_s = \frac{12.9K\Omega}{N_{ch}\lambda_f} \tag{4}$$

From the Matthiessen's rule, the λ_f can be determined by [10],

$$\lambda_f = \left(\lambda_s^{-1} + \lambda_p^{-1}\right)^{-1} \tag{5}$$

where λ_s signifies mean free path (MFP) due to the defects and MFP due to edge roughness is denoted by λ_p. The MFP of single graphene layer is 1μm but shrinks to 419nm for MLGNR interconnect due to intersheet electron hopping. The MFP because of λ_p is calculated by [10],

$$\lambda_p = \frac{w}{1-m}\sqrt{\left(\frac{2wE_f}{rhv_f}\right) - 1} \tag{6}$$

where, h signifies Planck's constant, v_f signifies Fermi velocity with a value of 8 $\times 10^5$ m/s and m signifies specularity of edges. The value of m fluctuates between 0 and 1. In this study, on the whole specular edges of MLGNR is considered and total resistance (p.u.l) at longer interconnects of MLGNR is calculated by (10),

$$R_{MLGNR} = \frac{12.9}{nN_{ch}}\left(1 + \frac{l}{\lambda_s}\right) \tag{7}$$

The MLGNR also consists of other parasitic such as inductance and capacitance. The inductance of GNR is further of two types kinetic (l_k) and magnetic (l_e) inductance. The (p.u.l) l_k and l_e are calculated by [10],

$$l_k = \frac{8nH}{N_{ch}} (\mu\text{m}) \tag{8}$$

$$l_e = \frac{\mu_o d}{w} (\mu\text{m}) \tag{9}$$

where μ_o is the magnetic permeability of free space.

The MLGNR has electrostatic and quantum capacitance given by (10) and (11) in (p.u.l) respectively,

$$C_e = \frac{\varepsilon_o w}{d} \tag{10}$$

$$C_q = \frac{4e^2 N_{ch} n}{hv_f} \tag{11}$$

where ε_o is the relative permittivity of free space. Every two layers of MLGNR behave as capacitor (parallel plate). Therefore, MLGNR has coupling inductance and capacitance between the layers given by (12) and (13) respectively [10],

$$l_m = \mu_o \delta / w \tag{12}$$

$$C_m = \varepsilon_o w / \delta \tag{13}$$

Based on the above mentioned study MLGNR can be modeled into equivalent single conductor (ESC) model (Fig. 2). The equivalent single conductor parasitic of MLGNR are given by (14)-(16)

$$R_{ESC} = R_{MLGNR} = \frac{12.9}{nN_{ch}}\left(1 + \frac{l}{\lambda_s}\right) \tag{14}$$

$$L_{ESC} = l_k + l_e \tag{15}$$

$$C_{ESC} = (C_q^{-1} + C_e^{-1})^{-1} \tag{16}$$

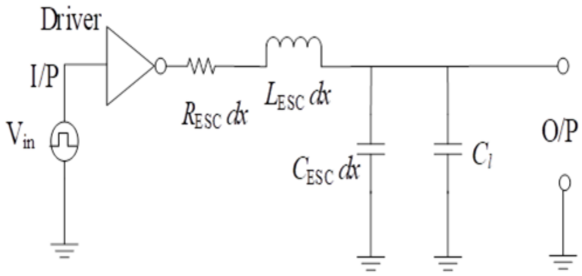
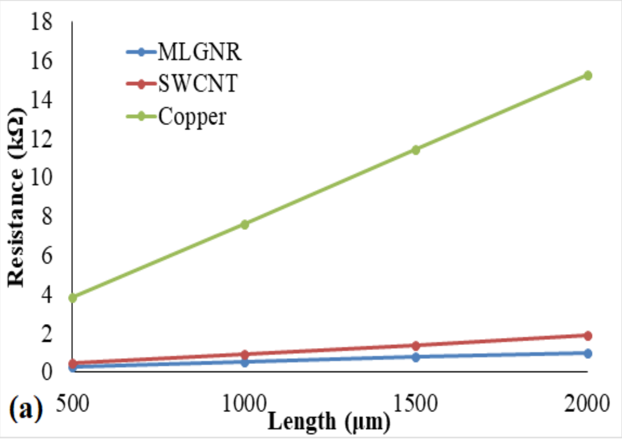


Fig.2: ESC model of MLGNR Interconnect

III. IMPEDANCE ANALYSIS

In the current section, equivalent resistance of MLGNR, SWCNT, and copper interconnects is discussed. The equivalent resistance of MLGNR for three different technologies is calculated from (1)–(7). The value of equivalent resistance is coded in MATLAB tool as per the data of ITRS-2013 [as shown in Table 1].



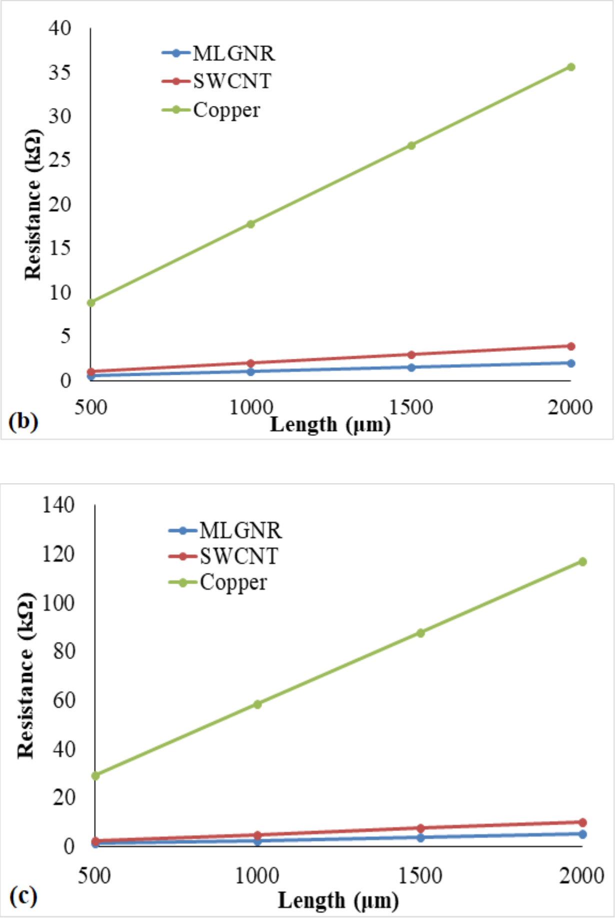


Fig. 3: The resistance of MLGNR, SWCNT and copper interconnects for 500µm-2000µm interconnect lengths at (a) 32nm, (b) 22nm, and (c) 16nm technologies

It is shown in Fig. 3 that the resistance is increasing for all the materials with increase in their interconnect length from 500µm to 2000µm for all three technologies. Further, it is also seen in the results that the rate of increase in resistance of MLGNR and SWCNT is less than copper.

Table 1: Simulation parameters as per ITRS-2013 version [5]

Interconnect Parameters	Technology Node		
	32nm	22nm	16nm
Width of interconnect	40nm	28nm	18nm
Height of interconnect	120nm	84nm	54nm
Thickness of Oxide	93.6nm	65.5nm	40nm
Aspect ratio (A/R)	3	3	3
Voltage (V_{dd})	0.9V	0.8V	0.7V
Dielectric constant (ε)	2.77	2.59	2.31
Resistivity for copper	3.66 $\mu\Omega$-cm	4.2 $\mu\Omega$-cm	5.69 $\mu\Omega$-cm

IV. PERFORMANCE ANALYSIS

The investigation of copper, MLGNR and SWCNT as interconnects for performance parameters (delay and PDP) at variable interconnect length for 32nm, 22nm and 16nm technology is discussed. The ESC model (Fig. 2) driven by CMOS inverter is considered to evaluate the performance of different interconnects using predictive technology model (PTM) [11]. The Tanner tool is used to simulate the performance of various interconnects.

A. *Signal delay analysis*

In the present section, MLGNR, SWCNT and copper interconnects performance is analyzed from signal delay at longer interconnects for 32nm, 22nm, and 16nm technologies. The propagation delay for different interconnect materials is shown in Fig. 4 and it can be observed from the results that with increase in length, the delay also rises for all the three interconnects.

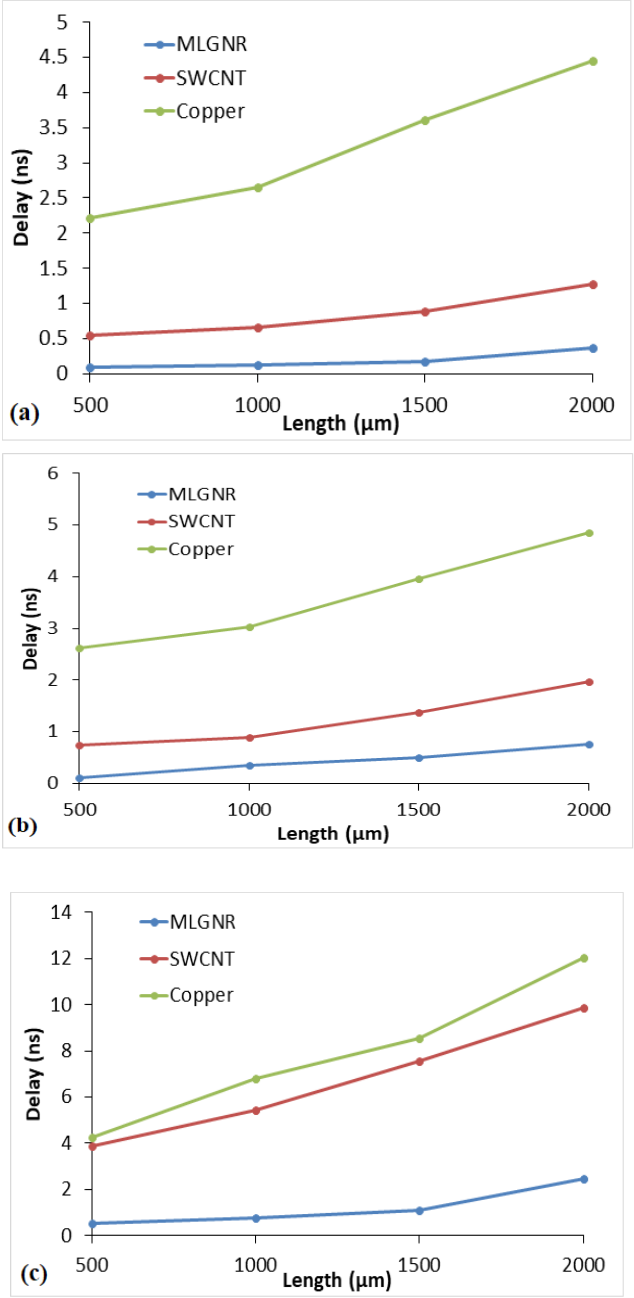


Fig. 4: Propagation delay of copper, MLGNR & SWCNT interconnects at variable lengths for (a) 32nm, (b) 22nm, and (c) 16nm technologies respectively.

Further, results also reveal that the delay of MLGNR is very less compare to SWCNT and copper interconnects 32nm, 22nm and 16nm technologies. Therefore, it is determined from results that MLGNR performance is better in comparison to SWCNT and copper interconnects at global levels for all the three technologies considered for the work.

B. *PDP analysis*

With the development of on-chip interconnects power dissipation also has a crucial role to play along with signal delay for the fabrication of ICs. Therefore, the overall performance of an interconnect depends upon the product of signal delay and power (PDP). The PDP of copper, MLGNR & SWCNT as interconnects is presented in Fig. 5.

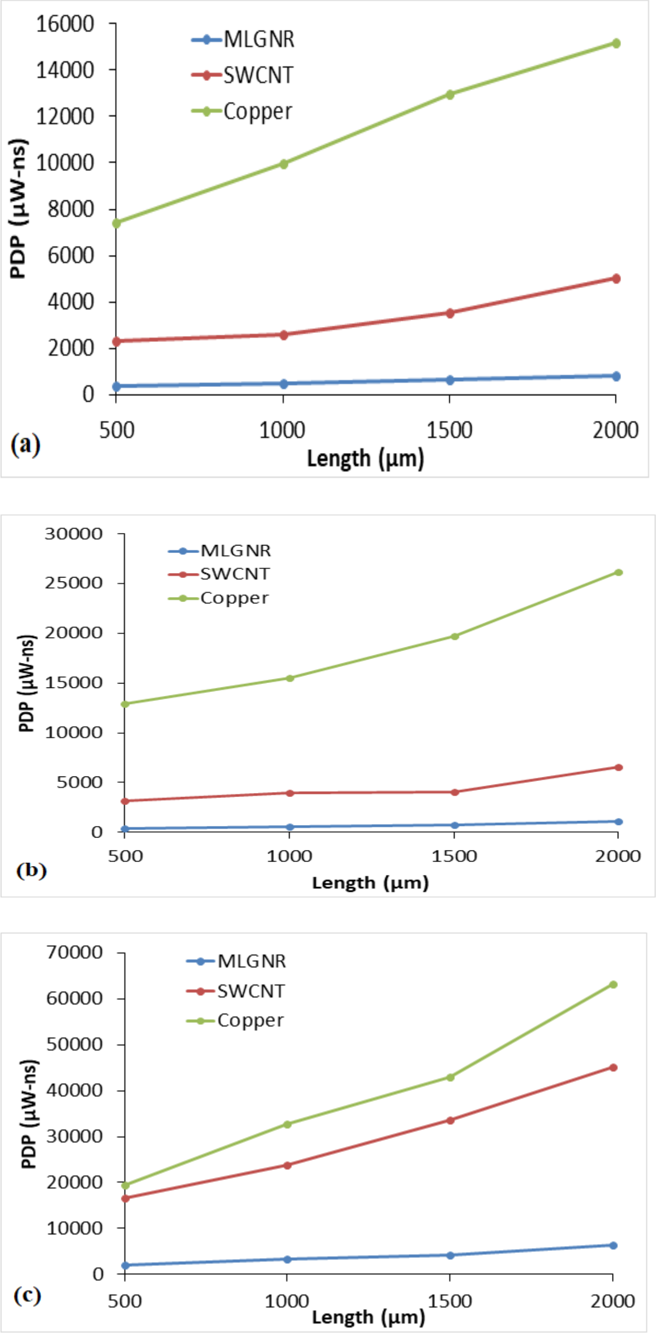


Fig. 5: PDP of copper, MLGNR and SWCNT interconnects at 500-2000µm length for (a) 32nm (b) 22nm, and 16nm technologies

The results show that the PDP of MLGNR is lesser in comparison to SWCNT and copper interconnects for all three technologies for variable interconnect lengths ranging from 500-2000µm. Hence, MLGNR is more suitable candidate as interconnect material at global interconnect for nanometer technologies to replace SWCNT and conventional copper interconnect. Therefore, to fabricate high speed and low power ICs, MLGNR can be considered as alternative option to replace copper as interconnect material.

V. CONCLUSION

The performance of copper, MLGNR and SWCNT interconnect for propagation latency and PDP at *500–2000µm* lengths for three technologies (32nm, 22nm, and 16nm) is presented. The parasitic of copper, MLGNR and SWCNT are calculated using the interconnect parameters predicted by ITRS. It is observed that the equivalent resistance of MLGNR is far better from SWCNT and copper. The performance of different interconnects is evaluated using Tanner tool. It is revealed from the results that the performance of MLGNR as interconnect is far superior to SWCNT and copper for delay and PDP. As a result, MLGNR achieves confidence of interest because of its outstanding performance and becomes protruding material in on-chip interconnects for nano-electronics IC fabrications.

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Karmjit Sandha received his B.E. and M.Tech in Electronics and Communication Engineering in 1999 and 2007 respectively. He received Ph.D. degrees in MWCNT based VLSI Interconnects from TIET, Patiala in 2015. He has been serving as Assistant Professor in ECE department of TIET Patiala since 2009. He is actively working in the field of Carbon Nanotubes (SWCNT and MWCNT bundle), Graphene and its applications as VLSI interconnects at nanometer technologies. He is supervising PhD and M.Tech students in the same field for their research work. From his research work, he has published 22 articles indifferent SCI/SCIE/SCOPUS indexed peer reviewed journals and 11 articles in International/National Conferences held in India and abroad.

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