Impact of Variable Interconnect length on the performance of MWCNT as VLSI Interconnect for Nanometer Integrated Circuit Design

Karmjit Singh Sandha, Gurleen Dhillon

Abstract: The impact of variable interconnects length on the performance of Multiwalled Carbon nanotubes (MWCNT) as very large scale integration (VLSI) interconnect at nanometer technologies is analyzed in the paper. The parasitic of MWCNT are calculated using electrical equivalent model for different interconnect lengths. The calculated parasitic are simulated to evaluate the delay and power delay product (PDP) of MWCNT at variable interconnect length (500µm to 2000µm) using SPICE simulation tool at nanometers technologies. Further, a comparable analysis is performed for traditional copper interconnect and obtained results are compared with MWCNT as interconnects. It is shown in the results that the performance in terms of resistance, delay and PDP is better for MWCNT as compared to copper for all the interconnects lengths and technology nodes considered in this paper. As a result, MWCNTs can be considered as a substitute to copper as upcoming interconnect material for integrated circuit (IC) design for nanometer technologies.

Index Terms: Delay, Integrated Circuit, Interconnects, Impedance parameters, Nanometer Technologies

I. INTRODUCTION

Interconnects are the conducting wires used in Integrated Circuits (IC) to establish the electrical connection between active devices of the circuits. With scaled down technology nodes, the dimensions and feature size of active devices and supply voltages of ICs are also scaled down. The density of active devices increases for VLSI-IC fabrication.[1-2] The large number and long interconnects are to be required to interface millions of such active devices within an IC. Therefore, interconnect cross-sectional dimensions are also required to be scaled down with the advanced technology nodes. With advancement of technology nodes, a large number of functionalities are to be incorporated in VLSI chip design. Thus, the requirement of long interconnects is exponentially increasing which connect millions of active devices in an IC. The impedance parameters of interconnects increase linearly as interconnects length increases and hence the performance of an interconnect becomes more important as compared to device performance for nanometer technologies. [3-5]. Different materials have been used as interconnects in IC design. Due to shortcomings of any existing material at certain technology node, traditional materials are to be replaced by other new materials. The present research, explores the possibilities to replace the traditional copper interconnects because its deficiencies like grain boundary, surface boundary and electromigration at nano-scaled technology nodes. Due to large electrical and thermal conductivity of Carbon Nanotubes (CNTs), CNT have been considered as alternative material for long VLSI-IC design. CNTs are hollow tubes made from a sheet of carbon graphene by rolling it up. [6-8]. These cylindrical shaped carbon molecules have attractive thermal and electrical properties which make it more suitable in the field of electronics, nanotechnology, optics, material science and other fields of technology. CNTs are classified as Single-walled CNT (SWCNT) and Multi-walled CNT (MWCNT) on the basis of its structure. SWCNTs are hollow tube rolled up from graphene sheets with similar diameter and SWCNT bundle consists of many such SWCNT tubes. When more than two hollow tubes with variable diameters are concentrically inserted to each other are known as Multi-Walled CNT (MWCNT). [9-10]

The cross-sectional view of MWCNT on ground plane is shown in Fig. 1.

Fig. 1: MWCNT on ground plane

Fig. 1 shows that diameters of different shells of MWCNT are different and vary from few nanometers to tens of nanometers. The conductivity (semiconductor or metal) of SWCNT is depends upon its chirality, where MWCNTs are always metallic in nature and easy to fabricate as well. Due to these advantages of MWCNT, the researchers are interesting to analyze the performance of MWCNT based interconnects for nanometer technologies for high speed integrated circuits. The paper presents an electrical equivalent circuit model and its performance for MWCNT bundle as interconnect for different interconnects lengths from 500µm to 2000µm at different technologies (32, 22 and 16nm).

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The paper starts with brief introduction to interconnects and its importance in an IC at deep sub-micron technology nodes. The paper summarizes the literature and presents research to be done in Section I. Section II presents the electrical equivalent circuit model and its calculation for MWCNT and copper as interconnect. In Section III, a comparative analysis of MWCNT and copper interconnect in term delay and PDP has been carried out. The obtained outcomes of the paper are concluded in section IV.

II. IMPEDANCE MODELS AND PERFORMANCE PARAMETERS

MWCNT bundle as VLSI interconnects is shown in Fig. 2 (a). In a MWCNT bundle, three MWCNT are stacked in parallel as shown in Fig. 2 (a). Each MWCNT is concentrically nested with many shells of different diameters one inside the other, as shown in Fig. 2 (b). The different shells of the MWCNT bundle have different diameters and these are depending on the technology nodes. The diameters of largest and smallest shell of MWCNT bundle are $D_{\text{max}}$ and $D_{\text{min}}$ respectively.\[1,\, 11]\] The center of MWCNT bundle is above the ground plane with a distance $h$. Spacing between two adjacent shells MWCNT bundle may vary from $0.3\text{nm}$ to $0.4\text{nm}$ for different configurations. The small adjacent distance leads towards increase inter-shell capacitance which may effects the average power consumption of interconnects, whereas the large inter-shell distance increases the overall resistance of the bundle and effects the propagation delay. The work presents in the paper has considered the distance of adjacent shells is equal to $\delta=0.34\text{nm}$.\[3,\, 9,\, 10]\]

![Fig. 2: (a) MWCNT bundle as VLSI interconnect (b) Enlarge view of MWCNT on ground plane.](image)

A. Number of shells and conducting channels in MWCNT

As discussed, MWCNT is having many shells of different diameters and these shells are counted as $l\ldots i\ldots n$ from outermost shell to innermost shell. The number of shells in a bundle depends upon the outermost diameter and diameter ratio of the bundle, where diameter ratio is the ratio between diameter of outermost shell to innermost shell of MWCNT bundle and given as $D_{\text{min}}/D_{\text{max}}$.

The outermost shell of MWCNT bundle is technology dependent parameter and diameter ratio ($D_{\text{min}}/D_{\text{max}}$) may vary from 0.35-0.8 depending upon fabrication process. Therefore, total $n$ number of shells in a bundle can be calculated as

\[n = 1 + \text{int} \left[ \frac{D_{\text{max}} - D_{\text{min}}}{2\delta} \right] \quad (1)\]

where $\text{int} \{\cdot\}$ represents the integer part which is to be considered for evaluation. Each shell of MWCNT has different diameter, hence diameter of any $i^{\text{th}}$ shell can be calculated as\[9]\]

\[D_i = D_{\text{max}} - 2\delta(i - 1), \text{ for } 1 \leq i \leq n \quad (2)\]

Every shell of MWCNT has different number of conducting channels and these conducting channels are diameter dependent. If the diameter of any $i^{\text{th}}$ shell is less than $3\text{nm}$, then the number of conducting channel will be considered as $2$ and for all shells with diameters more than $3\text{nm}$ can be calculated as\[11]\]

\[N_{\text{chan/\text{shell}}} \approx a_iD_i + b_i, \text{ for } D_i > 3\text{nm} \quad (3)\]

Where $D_i$ is the diameter of any $i^{\text{th}}$ shell, $a_i=6.12\times 10^4 \text{1/(nmK)}$ and $b_i=1.275$ The total number of conducting channels ($N_{\text{chan/bundle}}$) in a bundle is the sum of all the conducting channels ($N_{\text{chan/\text{shell}}}$) of all the shells and given by

\[N_{\text{chan/bundle}} = \sum_{i=1}^{n} N_{\text{chan/\text{shell}}}/i^{\text{th}}\text{ shell} \quad (4)\]

B. Parasitic of a shell of MWCNT

This sub-section emphasis on the parasitic of an individual shell i.e. resistance, inductance, capacitance and its equivalent impedance model.

The resistance of any $i^{\text{th}}$ shell of MWCNT bundle is divided into three parts: scattering dependent resistance ($R_{\text{scatt}}$) (if $l < \lambda$), quantum resistance ($R_{\text{quant}}$) and metal contact resistance ($R_{\text{mc}}$). The metal contact resistance ($R_{\text{mc}}$) is due to the contact of metal electrodes with MWCNT and depends upon the fabricating process. Therefore, metal contact resistance ($R_{\text{mc}}$) is fixed and assumed equal to $2k\Omega$ for each shell of MWCNT as given in\[10\]. The total resistance for an individual shell is given by

\[R_{\text{shell}} = R_{\text{mc}} + R_{\text{quant}} + R_{\text{scatt}}L \quad (5)\]

\[R_{\text{shell}} = 2k\Omega + \frac{h}{2e^2N} + \frac{h}{2e^2N} \cdot \frac{L}{\lambda}\]

where $h/2e^2=12.9k\Omega$, $N$, $L$ and $\lambda$ are the number of conducting channels, length and diameter dependent MFP of each shell of MWCNT respectively.\[11-16\]. It is shown in (5) that for long interconnect lengths the total resistance is directly proportional to the length and inversely proportionial to MFP of the shell. The shells of MWCNT is having large diameter as compare to SWCNT and hence will have large MFP as well. The inductance in MWCNT is of two types: magnetic inductance and kinetic inductance per unit length (p.u.l).
The magnetic inductance is due to the current flowing through MWCNT shell and stored as total magnetic energy in the shell. The magnetic inductance for an individual $i^{th}$ shell is given by

$$L_m = \left(\frac{\mu}{2\pi}\right) \cosh^{-1}\left(\frac{2\gamma}{D}\right)$$  \hspace{1cm} (6)

where $\mu$ is mobility of electron, $h_i$ is the distance between center of the bundle and ground as shown in Fig. 2 (b). The kinetic inductance is due to each conducting channel of MWCNT shell stored in the form of kinetic energy when shell conducts and given as [10]

$$L_{k/channel} = \frac{h}{2 \times 2 \sqrt{\nu_f}} e^{-\gamma}$$  \hspace{1cm} (7)

$$L_k/\text{shell} = L_{k/channel} / N_i$$  \hspace{1cm} (8)

The capacitance in MWCNT bundle is classified as quantum capacitance ($C_q$) and electrostatic capacitance ($C_s$). The capacitance is due to quantum electrostatic charge stored in be shells when current flow through it, is known as quantum capacitance ($C_q$) [6,9]. The quantum capacitance for a shell is given by

$$C_q/\text{channel} = \frac{2 \times 2 \sqrt{\nu_f} \approx 193aF / \mu m}{h}$$  \hspace{1cm} (9)

$$C_q/\text{shell} = C_q/\text{channel} N_i$$  \hspace{1cm} (10)

The electrostatic capacitance ($C_s$) appears due to charge stored by the outermost shell of MWCNT bundle having diameter $D_{max}$ at a distance $h_0$ from ground level as shown in Fig. 2 (b). Hence, the electrostatic capacitance p.u.l. of shell is given by

$$C_e = \frac{2 \pi e}{\cosh^{-1}\left(\frac{2\gamma}{D_{\text{outer}}\right)$$  \hspace{1cm} (11)

Due to different potentials of difference of MWCNT shells, inter-shell coupling capacitance ($C_s$) is there and it can be obtained by using the same equation which can be used for coaxial capacitance and given by

$$C_s = \frac{2 \pi e}{\ln\left(\frac{D_{\text{out}}}{D_{\text{in}}\right)} - \left[\frac{2 \pi e}{m(D_{\text{out}}/D_{\text{in}} - 2\delta)}\right]$$  \hspace{1cm} (12)

where $D_{\text{in}}$ and $D_{\text{out}}$ are the diameters for inner and outer adjacent shells of MWCNT bundle respectively and $\delta=0.34nm$. On the basis of parasitic defined in (5) - (12), the equivalent impedance parameter model of any $i^{th}$ shell is shown in Fig. 3.

\[\text{Fig. 3: Impedance parameter model of } i^{th} \text{ shell of MWCNT}\]

C. Equivalent Circuit Model of MWCNT Bundle Interconnects

An individual shell of MWCNT has very high resistance hence it cannot be used as individual tube for interconnects. So, concentrically nested several CNTs are used in parallel to form MWCNT bundle resulting in net reduction of overall resistance. Therefore, by considering all the shells in parallel and parasitic discussed in the preceding sub-sections, an equivalent impedance model for MWCNT bundle interconnects is presented in Fig. 4. [9,10]

\[\text{Fig. 4: Equivalent parasitic model of MWCNT bundle as interconnects.}\]

D. Impedance parameters of copper

The impedance equivalent circuit of copper as interconnects material is presented in this sub-section. The electrical equivalent analytical model is presented to evaluate the equivalent impedance parameters such as resistance; inductance and capacitance for a copper interconnect. [10] The resistivity of copper plays an important role to calculate the resistance for rectangular cross-sections interconnects. Therefore, the resistance of copper interconnect depends upon the resistivity and technology dependent cross-sectional dimensions as given below

$$R_{cu} = \frac{\rho L}{WJ} = \frac{\rho_s + \rho_d L}{WJ}$$  \hspace{1cm} (13)

where, $\rho$ is resistivity of copper and resistivity $\rho$ divided into two parts and given as phonon surface scattering ($\rho_s$) and defect ($\rho_d$) and given as

$$\rho = \rho_s + \rho_d$$  \hspace{1cm} (14)

$$\rho = \rho_0 \left[1 + 0.00401(T - 300)\right]$$  \hspace{1cm} (15)

where $\rho_0$ is technology dependent resistivity of copper at 300K. The inductance and capacitance of copper interconnects can be expressed as

$$L_{cu} = \frac{\mu_d L}{2\pi} \left[\ln\left(\frac{2L}{W + t}\right) + \frac{1}{2} + \frac{0.22(W + t)}{L}\right]$$  \hspace{1cm} (16)

Where $L$ and $\mu_d$ are length of interconnect and permeability ($\mu_0=4\pi \times 10^7 \text{ H/m}$), respectively. [9, 10]

The capacitances of copper ($C_{cu}$), as interconnect occur due to its placement over the ground generating fringing flux which is called ground capacitance ($C_g$). Coupling capacitance ($C_s$) exists as a result of coupling between nearby interconnect, these can be calculated by

$$C_{cu} = 2(C_g + C_s)L$$  \hspace{1cm} (17)
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\[ C_s = \varepsilon \left( \frac{W}{h} + 2.22 \left( \frac{s}{s + 0.7h} \right)^{1.19} + 1.17 \left( \frac{s}{s + 1.5h} \right)^{0.76} \right) \frac{t}{t + 5.53h} \]  

\[ C_s = \varepsilon \left[ 1.14 \left( \frac{t}{s + 2.06x} \right)^{0.09} + 0.74 \left( \frac{w}{w + 1.59s} \right)^{1.14} \right] \]  

\[ + 1.16 \left( \frac{w}{w + 1.875} \right)^{0.16} \left( \frac{t}{t + 0.98s} \right)^{1.18} \]  

\[ \varepsilon_C = \varepsilon + \varepsilon_t + \varepsilon_{\text{oxide}} \]

Where \( t \) and \( s \) are thickness of oxide and separation between the two interconnect, respectively. The dielectric constant (\( \varepsilon \)) of copper is technology dependent as shown in Table I.

### III. RESULT AND DISCUSSION

All the impedance parameters of different materials have been calculated by using the analytical models presented in the section II. The parasitic of MWCNT and copper have been evaluated by using (1-12) and (13-19) respectively at 32, 22 and 16nm technology nodes for 500, 1000, 1500 and 2000\(\mu\)m interconnect length. The MATLAB is used to write the codes for different equations to calculate the impedance parameters of different materials. The interconnect parameters used to calculate the parasitic with the help of equations for different material are taken from ITRS 2013 [11,12] and shown in Table I.

**Table I:** Interconnect parameters for global level interconnect length as per ITRS 2013 [12]

<table>
<thead>
<tr>
<th>Interconnect Parameters</th>
<th>Technology Node</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>32nm</td>
</tr>
<tr>
<td>Width of interconnect</td>
<td>40nm</td>
</tr>
<tr>
<td>Height of interconnect</td>
<td>120nm</td>
</tr>
<tr>
<td>Thickness of Oxide</td>
<td>93.6nm</td>
</tr>
<tr>
<td>Aspect ratio (A/R)</td>
<td>3</td>
</tr>
<tr>
<td>( V_{dd} )</td>
<td>0.9V</td>
</tr>
<tr>
<td>Dielectric constant (( \varepsilon ))</td>
<td>2.77</td>
</tr>
<tr>
<td>Resistivity for copper</td>
<td>3.66 ( \mu \Omega \cdot \text{cm} )</td>
</tr>
</tbody>
</table>

The calculated resistances for different materials at 32, 22 and 16 nm technology nodes for 500, 1000, 1500 and 2000\(\mu\)m length are shown in Table II.

**Table II:** Comparative analysis in term of resistance between SWCNT, MWCNT and copper interconnects for interconnect length 500, 1000, 1500 and 2000\(\mu\)m at 32nm, 22nm and 16nm technologies.

<table>
<thead>
<tr>
<th>Length ((\mu)m)</th>
<th>Technology Nodes</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>32nm</td>
</tr>
<tr>
<td>Copper</td>
<td>MWCNT</td>
</tr>
<tr>
<td>500</td>
<td>3812.3</td>
</tr>
<tr>
<td>1000</td>
<td>7625</td>
</tr>
<tr>
<td>1500</td>
<td>11437.5</td>
</tr>
<tr>
<td>2000</td>
<td>15250</td>
</tr>
</tbody>
</table>

It can be well interpreted from the values shown in Table II that for 32nm technology node and below, because of certain issues prevailing in copper like electromigration and other scattering effects as mentioned in the previous sections, there is a sharp rise in its value of resistance and this value gets significantly large as technology nodes are scaled down from 32nm to 16nm. The MWCNT bundle shows the lesser values of resistances for 500, 1000, 1500 and 2000\(\mu\)m interconnect length and are introduced because of their extraordinary good conduction properties making them highly applicable as VLSI interconnect material.

For the comparative analysis, the evaluated results for 1000\(\mu\)m interconnects length are plotted in Fig. 5 for better understanding of the results.

**Fig. 5:** Comparison of resistance between Copper and MWCNT interconnects for 1000\(\mu\)m length at 32, 22 and 16nm technologies.

It is revealed from the results shown in Fig. 5 that the gap between copper and CNTs is sharply increasing with scaled down technologies i.e. from 32nm to 16nm, which is due to the scattering mechanism effects and electromigration. The calculated parasitic are used to simulate the delay and PDP. The HSPICE simulations tool is used for Copper and MWCNT at interconnect length 500\(\mu\)m to 2000\(\mu\)m at different nanometer technology nodes to study their propagation delays.
Fig. 6: Comparison of delay between copper and MWCNT interconnects length from 500μm-2000μm at (a) 32nm, (b) 22nm (c) 16nm technologies and (d) Combined comparative analysis for all three technologies.

The simulation results for copper and MWCNT as interconnects material for interconnect length 500μm to 2000μm are shown in Fig. 6 (a)-(c) at 32nm, 22nm and 16nm technologies respectively and Fig. 6 (d) Combined comparative analysis for all three technologies. It is clearly depicted from the results shown in Fig. 6 (a)-(c) that delay of circuit rises with the increase in the length of interconnects. As observed from the results shown in Fig. 6 (d), MWCNT show the lesser value of propagation delay than copper which suffers from electromigration and surface scattering effects which leads to increased resistivity and decreased mean free path at global lengths at scaled future technology nodes.

Further, the paper presents the graphs of performance parameter and figure of merit i.e. PDP (power delay product) of copper and MWCNT for 500 μm to 2000 μm shown in Fig. 7.

Fig. 7: Comparison of PDP between copper and MWCNT interconnects for interconnect length 500μm-2000μm length at (a) 32nm, (b) 22nm (c) 16nm technology nodes and (d) Combined comparative analysis for all three technologies.

It is clearly evident from the results shown in Fig. 7 (a)-(c) that the value of the PDP parameter of CNT is again lowest as compared to copper. As observed from Fig. 7 (d) that with the further scaling of technology node, the gap between PDP of MWCNT with respect to copper is increasing sharply for all the interconnects lengths. Therefore, it is revealed from the results that the improved performance in favor of MWCNT which is due to decreased MFP and fatal issues faced by copper at nanometer technology nodes for global lengths of interconnect. Clearly, MWCNT can outperform the existing interconnect materials for next generation VLSI technology nodes particularly for long interconnect length.
III. CONCLUSION

This paper presented the deficiencies of copper as interconnect at nanometer technologies for variable interconnect length and advantages of MWCNTs as interconnects are highlighted and improvement in the performance is established. The electrical equivalent circuit models for MWCNT and copper interconnect are presented. The impedance parameters on the basis of electrical equivalent circuit models are evaluated for variable interconnect lengths (500-1000μm) at 32nm, 22nm and 16nm technologies. By using Tanner EDA tool, simulations are performed for variable interconnect lengths and results show that MWCNT undoubtedly show better performance than copper in terms of propagation delay and power-delay product (PDP) which suffers from several issues like decreased MFP and surface scattering effects at nanometer technology nodes and this improvement in results gets better with the further scaling of technology nodes.

REFERENCES


AUTHORS PROFILE

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