Design & Implementation of Compact-Integrated Solar-PV Symmetric Multilevel Inverter Topology for RES Applications

Ch. Punya Sekhar, P. V. Ramana Rao, M. Uma Vani

Abstract*: Multi-level inverter (MLI) engages the incredible recognition for high power-medium voltage apparatus and highly suitable for distributed-generation by utilizing renewable energy sources. In general multilevel inverter topologies acts as feasible substitute of formal 2-level inverters; there has been vital interest in the development of novel inverter structures. Several MLI structures incorporate the more switching devices which increases the complex design due to increased number of operating levels. This paper explores the novel single phase symmetric 5-level inverter topology is proposed and driving by both voltage pulse method/multi carrier pulse width modulation (PWM) technique. The proposed novel compact symmetric 5-level inverter topology offers fewer switches, gate drive circuits, reduced size, low cost, low harmonic profile, low switch stress and high efficiency over the formal topologies. The detailed simulation analysis of proposed 5-level inverter performance is conceded by MATLAB/SIMULINK software and feasibility has been evaluated by hardware-prototype model, results are illustrated.

***Index Terms*: Distributed Generation, Multilevel Inverter, Simplified Multi Carrier PWM, Renewable Energy Sources, Solar-Photovoltaic, Total Harmonic Distortions**

I. INTRODUCTION

Recent days, the Distribution Generation (DG) plays a vital role in remote areas to acquire the power demand by utilizing renewable energy sources where utility grid is non-presence [1]. Renewable energy sources (RES) have immense development due to increased energy demand, clean energy, and reduced fossil fuels. Several renewable energy sources are solar-photo-voltaic (SPV) systems; fuel cell and wind energy are directly interfaced to grid or load by utilizing power conditioning units [2]. These power conditioning unit's acts as mediation such as, front-end DC-DC converter, DC-AC inverter topology, etc. The DC-AC inverters are most significant in modern set-up of Distributed Generation (DG) scheme and also used in many high power medium voltage applications. The DC-AC inverter structure is appointed by smart power-semiconductor switches/diodes; commonly MOSFETs and IGBTs are used and controlled by gate-drive circuitry.

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The schematic block diagram of renewable energy conversion scheme is depicted inFig.1. Based on nature of outcome voltage waveform, inverters can be categorized as square wave, quasi-squarewave inverter. This square-wave or quasi-square wave inverters have more harmonic distortions at output voltage waveform, which affects the grid code standards and requires high range filter circuitry, greater switching stress, etc.

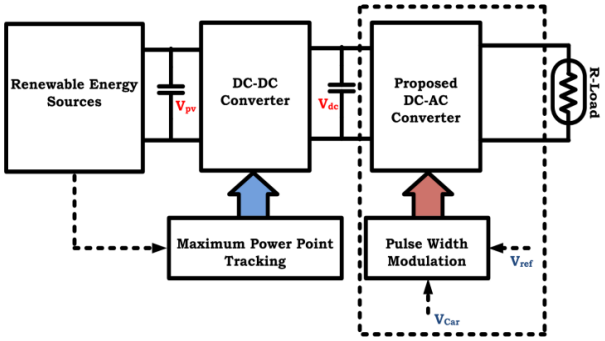


Fig.1 Block Diagram Representation of Renewable Energy Conversion System

With the emergence of modern power-electronic devices, multilevel inverter (MLIs) are getting more popular resolution to enhance the performance of DG based renewable power generation scheme and also other futuristic power semi-conductor utilities in high-power medium voltage applications. Generally, MLI topology plays a key role in many domestic and industrial applications such as induction motor drive systems [5], [6], micro-grid applications [7], [8], and FACTS controllers [9], [10], so on. These inverters furnishes the stair-case outcomes with respect to superior quality of RMS voltage/current waveform under the desired spectrum, low THD content, minimized voltage stress over the switches, low electro-magnetic compatibility, incredible efficiency, etc. The acquired outcome voltage is unification by significant switching of various DC-link voltages, which deals to reduce the dv/dt stress on switches and enhances the quality waveform [11].Traditionally, MLI topologies are categorized as diode-clamped type [12], flying capacitor type [13], as well as cascaded H-bridge MLI type [14], which can be comprised of dual strategies such as symmetrical and asymmetrical topologies. Over the other MLI topologies, the cascaded H-Bridge MLI is sovereign by many years for several industrial and commercial applications.

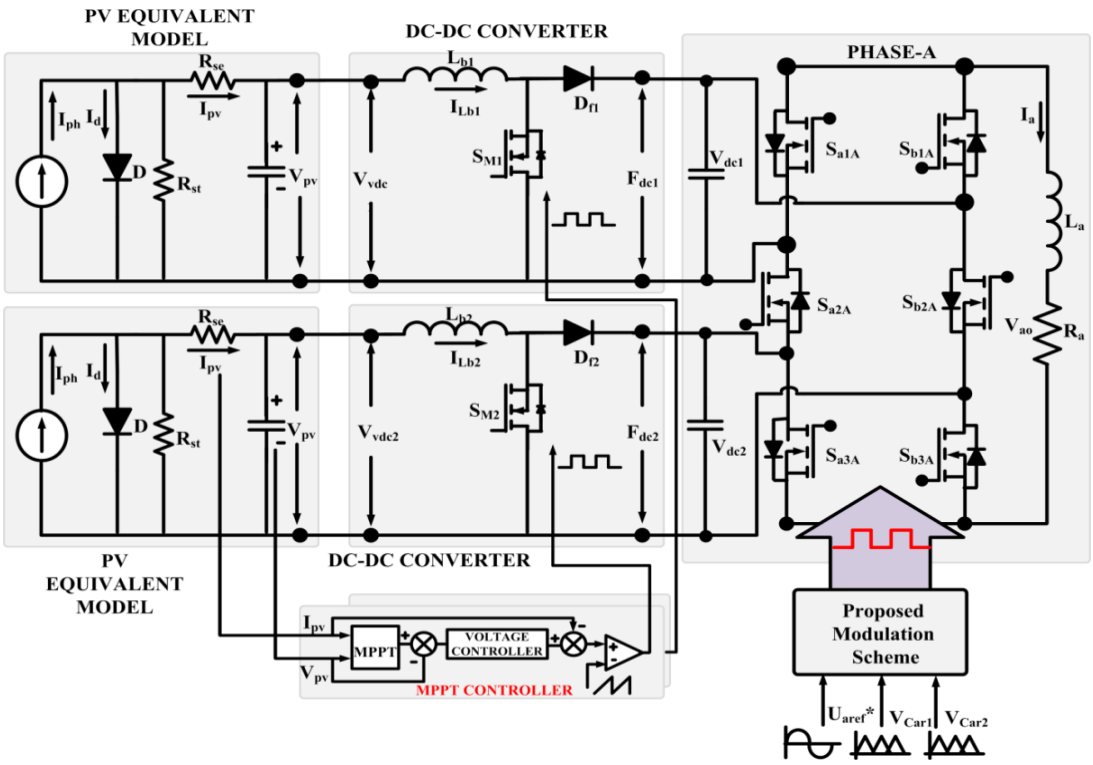


Fig.2 Schematic Diagram of Proposed Single-Phase 5-Level Symmetric MLI Topology for DG Application

Moreover, the traditional CHB-MLI is un-popular due to requirement of more switching devices for greater number of voltage levels, cost effective, bulky size, complex circuitry, influences the low efficiency and reliability. Along with the anatomy of the traditional MLI topologies, several researchers render the prominent effort to evolve novel MLI topologies with low number of switches with good harmonic profile. A novel multilevel inverter is introduced by E. Najafi and A.H.M. Yatim [15], based on Reverse-Voltage (RV) technique which is widely used for high-power medium-voltage applications. This RV technique requires ((N-1)+4) switches, ((N-1)/2) DC sources, greatly preferred for higher voltage levels which reduces the requirement of carrier-signal generation, complexity, over-all cost, space requirement. S. N. Rao et al. [16], proposes a new multi-level DC-link inverter designed as series/parallel conversion scheme by utilizing several sub-cell modules and H-bridge topology. This topology also requires ((N-1)+4) switches, ((N-1)/2) DC sources over the traditional MLI topologies. R. S. Alishah et al. [17], proposes the hybrid multilevel inverter based on series/parallel formation by utilizing sub-module cells. It consists of DC-link source, switch and diodes for generation of output voltage levels operated as series integration scheme. It can generate more number of voltage levels with low operating switches and gate-drive circuits, requires ((N-1)+2) switches, ((N-1)/2) DC sources and diodes over the traditional MLI topologies. Moreover the above-studied topologies pre-requisites of basic building modules which are integrated as series formation, requires more switching elements and gate-drive circuits over the newly proposed topology. A newly proposed MLI topology treated as symmetrical structure since all input DC-link voltages are equal. The symmetric structure is very modular & compact, that makes them easy to extend/design for greater number of voltage levels. Typically, MLI topologies are driving by both vital switching frequency and great switching frequency [18], [19]. The multi-carrier modulation techniques are used to acquire the qualitated RMS voltage/current waveform with the requirement of low rated filter units, low total harmonic distortions (THD). In this paper, a novel symmetric 5-level single phase MLI topology is studied and validated by both voltage pulse method and multi-carrier pulse-width modulation techniques. The proposed asymmetric inverter topology have attractive features such as fewer switching elements, low gate drive circuits, reduced size, low cost, low switch stress and high efficiency can be attained over the formal inverter topologies. The detailed simulation analysis of proposed 5-level inverter performance is evaluated by using computer Simulink tool. The feasibility of proposed 5-level compact inverter topology has been evaluated experimentally by using DSP prototype model, results are conferred with comparisons.

II.PROPOSED MULTILEVEL INVERTER TOPOLOGY

The proposed 5-level symmetric MLI topology is comprised of six MOSFET switches, two equal DC sources, switching sequences and one resistive/resistive-inductive load. The proposed 5-level topology requires equal DC-link voltage as (V_{dc1}=V_{dc2}), ultimately the final outcome voltage is attained by series action of two DC-link voltages as (V_{dc}=V_{dc1}+V_{dc2}). The schematic diagram of proposed single phase 5-level symmetric MLI topology for DG Application is depicted in Fig.2.

Table.1 Switching Sequences are for Proposed 5-Level Symmetric MLI Topology

Voltage Levels	S_{a1}	S_{a2}	S_{a3}	S_{b1}	S_{b2}	S_{b3}
0V_{dc}	F	F	F	N	N	N

V_{dc}	N	F	F	F	N	N
$2V_{dc}$	N	F	N	F	N	F
$-V_{dc}$	F	N	N	N	F	F
$-2V_{dc}$	F	N	F	N	F	N

The definite DC voltage is transformed to the output terminals and the required five output voltage levels ($0V_{dc}$, V_{dc}, $2V_{dc}$, $-V_{dc}$, and $-2V_{dc}$) are generated by switching the appropriate switches as a certain manner. Appropriate 5-level AC output voltage is acquired at load with respect to gate drive pulses, the switching sequences are clearly illustrated in Table.1. In Table.1, the "N" represents the ON-state of respective switch and "F" represents the OFF-state of switch, the operating modes of proposed symmetric 5-level MLI topology is illustrated in Fig.3.

A. *Operating Modes*

To produce a voltage level of V_0=0, the switches S_{b1}, S_{b2} and S_{b3} are turned ON and the voltage across the load terminals is zero due to short-path. The Fig.3 (a) depicts the operating mode of 0-level. To produce a voltage level of V_0=Vdc, S_{a1}, S_{b3} and S_{b2} are turned ON at the positive (+ve) half-cycle by providing the switching states with the help of proposed modulation scheme.

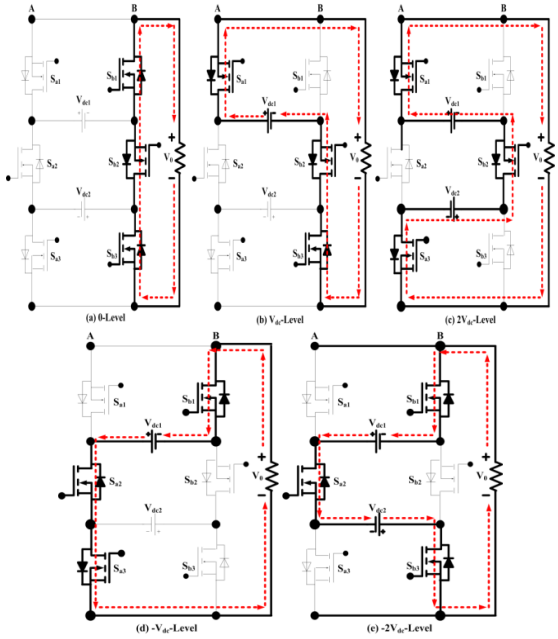


Fig.3 Operating Modes of Proposed 5-level MLI Topology

The pertained voltage is furnished by the V_0=V_{dc1} and the voltage across the load terminal is V_{dc}. The Fig.3 (b) depicts the operating mode of V_{dc}-level. To produce a voltage level of V_0=$2V_{dc}$, S_{a1}, S_{b2} and S_{a3} are turned ON at the +ve half-cycle by providing the switching states with the help of proposed modulation scheme. The pertained voltage is furnished by the V_0= (V_{dc1}+V_{dc2}) and the voltage across the load terminal is $2V_{dc}$. The Fig.3 (c) depicts the operating mode of $2V_{dc}$-level. To produce a voltage level of V_0=-Vdc, S_{a2}, S_{a3} and S_{b1} are turned ON at the negative -ve half-cycle by providing the switching states with the help of proposed modulation scheme. The pertained voltage is furnished by the V_0= V_{dc1} and the voltage across the load terminal is $-V_{dc}$. The Fig.3 (d) depicts the operating mode of $-V_{dc}$-level. To produce a voltage level of V_0=$-2V_{dc}$, S_{a2}, S_{b3} and S_{b1} are turned ON at the -ve half-cycle by providing the switching states with the help of proposed modulation scheme. The pertained voltage is furnished by the V_0= (V_{dc1}+V_{dc2}) and the voltage across the load terminal is $-2V_{dc}$. The Fig.3 (e) depicts the operating mode of $-2V_{dc}$-level.

III. PROPOSED SIMPLIFIED PWM TECHNIQUE

Several modulation strategies are used in multi-level inverters for several applications to control the output voltage waveform. Generally, PWM strategies are comprised into two objectives, such as fundamental switching frequency PWM technique, multi-carrier based PWM technique. Out of all, the multi-carrier based PWM techniques are more popular because of low complex function when the more number of output voltage levels. Several multi-carrier pulse-width modulation techniques are sinusoidal reference based phase-shifted modulation (PS-PWM) technique [19], level-shifted modulation (LS-PWM) technique [20] and space vector pulse width modulation (SVPWM) technique [21] are reviewed by so many literatures to control the MLI output waveform. This paper employs the new simplified multi-carrier based sinusoidal PWM technique consisted of one reference signal U_{aref}* is compared with a dual carrier signals (V_{car1}, V_{car2}). All the carriers have equal & high switching frequency with a little difference in peak magnitude and disposed vertically. The carrier signals are compared with dual carrier signals to create the switching states A and B. These switching states A and B are controlled by additional pulse generated switching state C. The generation of optimal pulses to the proper switches is defined by mathematical notation which is depicted in Eqn. (1). The switching pattern of the proposed 5-level symmetric MLI is depicted in Fig.4.

$$\begin{aligned} Sa1 &= \bar{A}C + \bar{C} \\ Sa2 &= C \\ Sa3 &= \bar{B}C + \bar{A}\bar{C} + B\bar{C} \quad \ldots\ldots(1) \\ Sb1 &= AC \\ Sb2 &= \bar{C}A \\ Sb3 &= BC \end{aligned}$$

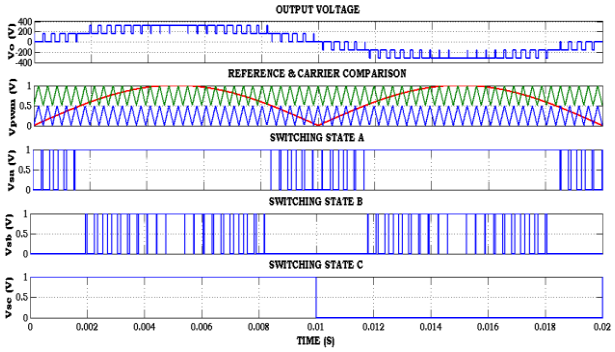


Fig.4 Simplified Switching Pattern

IV. MATLAB/SIMULINK RESULTS

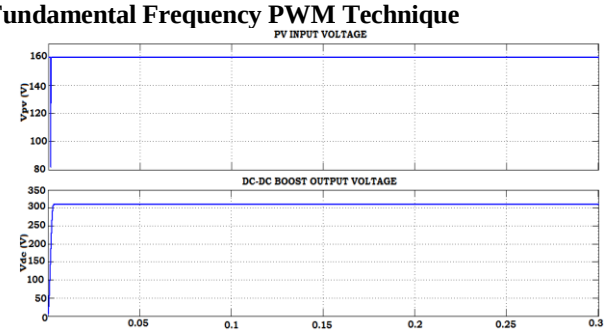
Table.2Operating Specifications

S.No	Parameters	Values
01	PV Input Voltage	150 V
02	PV Output Power	2.5 KW
03	DC-Link Voltage	V_{dc1}= V_{dc2}=160V

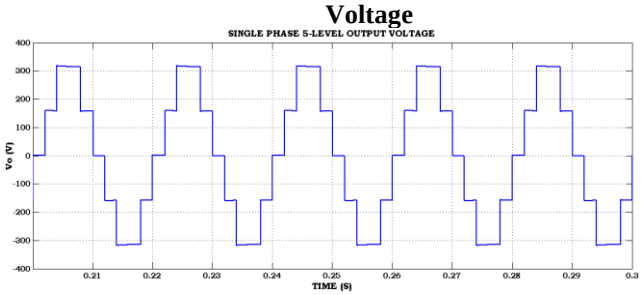
04	Switching Frequency	5KHz
05	Resistive-Inductive Load	R-18Ω, L-20mH

The simulation analysis is carried-out by proposed single phase phased 5-Level symmetric MLI topology under RL-load. The proposed topology is verified by using fundamental switching frequency PWM and multi-carrier PWM techniques with the help of computer-simulation tool. Based on the simulation analysis, an experimental prototype model also implemented and results are conferred with comparisons, the system specifications are illustrated in Table.2.

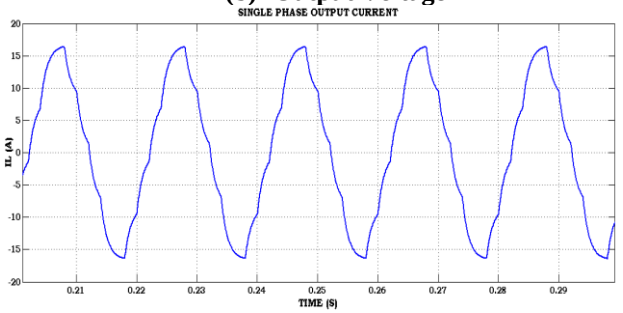
A. Proposed 5-Level Single Phase Symmetric MLI under Fundamental Frequency PWM Technique



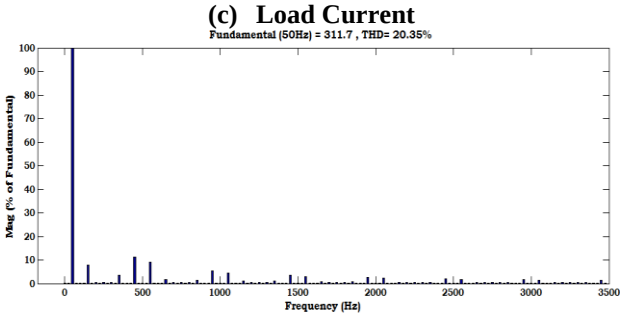
(a) PV Output Voltage & DC-DC Boost Converter Voltage



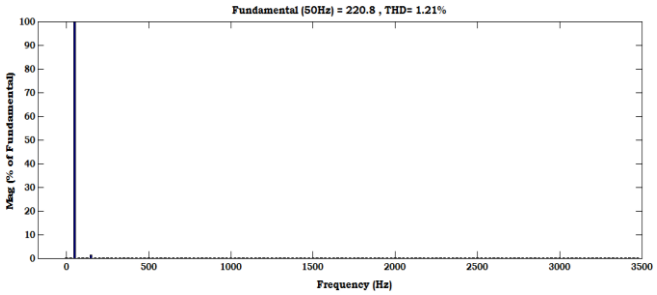
(b) Output Voltage



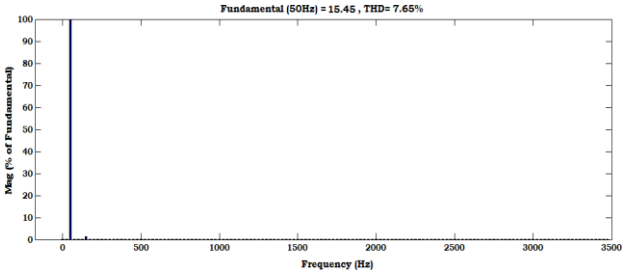
(c) Load Current



(d) THD Analysis of Output Voltage



(e) THD Analysis of Output Voltage with Second-Order Filter

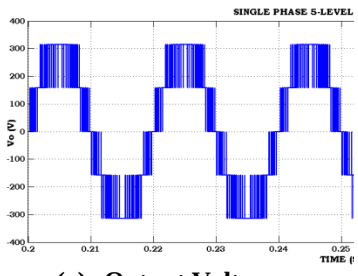


(f) THD Analysis of Load Current

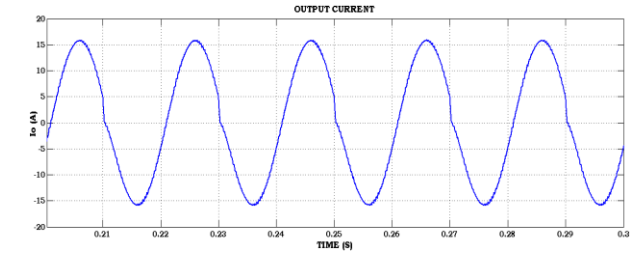
Fig.5 Simulation Results of Proposed Single-Phase Symmetric 5-Level MLI Topology under RL-Load using Fundamental Frequency PWM Technique

The simulation results of proposed single-phase symmetric 5-level mli topology under RL-load using fundamental frequency PWM technique are illustrated in Fig.5. In that, (a) PV & DC-DC Boost Output Voltage, (b) Output Voltage, (c) Load current, (d) THD Analysis of output voltage, (e) THD analysis of output voltage with second-order filter, (f) THD analysis of load current, respectively. A single-diode technique PV model is developed and attaining very-low voltages, the PV-model is operated under constant temperature and irradiation levels. The DC-DC converter interface converts the low-level PV voltage into high-level required voltage for achieving RL-load. The output voltage shows the desired 5-level voltage by utilizing 6 switches instead of 8 switches over the traditional MLI topologies. The stair-case output voltage is acquired by operating the respective switches in proposed MLI topology, THD analysis of output voltage is 20.35%. The output stair-case voltage is re-transformed into pure sinusoidal RMS voltage by utilizing second-order filter, THD analysis of output voltage with second-order filter is 1.21%. The output load current also acquiring the near sinusoidal RMS current wave-shape, the THD analysis of load current is 7.65%, these are comply with the IEEE-519 standard limits. The proposed 5-level MLI topology is powered by fundamental switching frequency technique, but it is used while the MLI topology is attaining operating characteristics rather than real-time control.

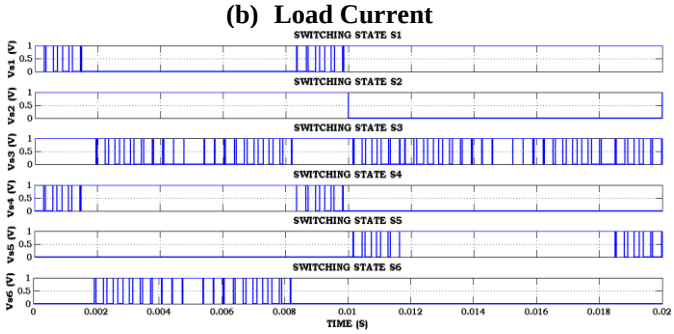
B. Proposed 5-Level Single Phase Symmetric MLI under Multi-Carrier PWM Technique



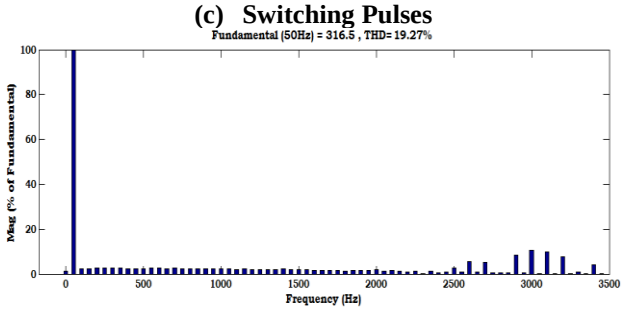
(a) Output Voltage



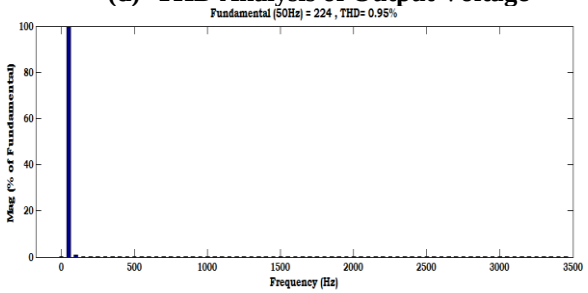
(b) Load Current



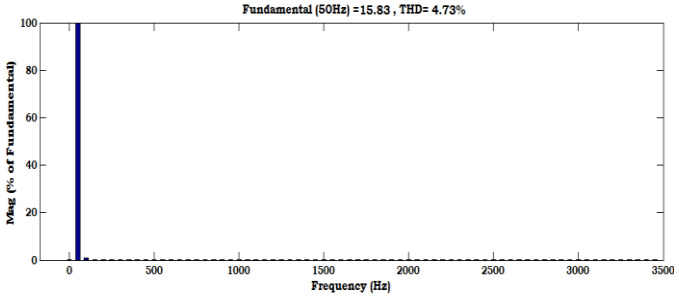
(c) Switching Pulses



(d) THD Analysis of Output Voltage



(e) THD Analysis of Output Voltage with Second-Order Filter



(f) THD Analysis of Load Current

Fig.6 Simulation Results of Proposed Single-Phase Symmetric 5-Level MLI Topology under RL-Load using Proposed Simplified Multi-Carrier PWM Technique

The simulation results of proposed single-phase symmetric 5-level mli topology under RL-load using proposed-simplified PWM technique are illustrated in Fig.6. In that, (a) PV & DC-DC Boost Output Voltage, (b) Output Voltage, (c) Load current, (d) THD Analysis of output voltage, (e) THD analysis of output voltage with second-order filter, (f) THD analysis of load current, respectively. The output voltage shows the desired 5-level voltage by utilizing 6 switches instead of 8 switches over the traditional MLI topologies. The stair-case output voltage is acquired by operating the respective switches in proposed MLI topology driven by proposed simplified PWM technique. This proposed PWM technique requires only single sinusoidal reference signal and two triangular carrier signals for generation of optimal switching states with good quality of RMS voltage wave-shape with low THD profile, THD analysis of output voltage is 19.27%. By using high range carrier frequency, the harmonics are shifted from low-order to high order influences the minimizing the load side filter size and attains high efficiency. The output stair-case voltage is re-transformed into pure sinusoidal RMS voltage by utilizing second-order filter, THD analysis of output voltage with second-order filter is 0.95%. The output load current also acquiring the near sinusoidal RMS current wave-shape, the THD analysis of load current is 4.73%, these are greatly comply with the IEEE-519 standard limits. The proposed 5-level MLI topology is powered by proposed simplified PWM technique offers many domestic & industrial applications. The THD comparison of proposed MLI topology under fundamental frequency and proposed simplified PWM techniques are clearly illustrated in Table.3. Over the fundamental technique, the proposed simplified PWM technique has reduced harmonic profile and attains highly qualitated RMS voltage and load current wave-shapes and represented graphical view in Fig.7. The feasibility of the proposed 5-level symmetric MLI topology is implemented in hardware prototype model and results are conferred.

Table.3 THD Comparative Analysis of Proposed MLI Topology under Fundamental Frequency & Proposed Simplified PWM Techniques

	With Fundamental Frequency PWM Technique	With Proposed Simplified PWM Technique
Output Voltage	20.35%	19.27%
Output Voltage with Filter	1.21%	0.95%
Load Current	7.65%	4.73%

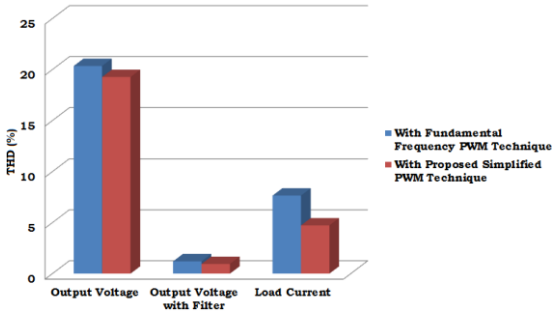


Fig.7 Graphical View-THD values of Output Voltage, Output Voltage with Second-Order Filter and Load Currentunder Fundamental Frequency & Proposed Simplified PWM Techniques

C. Hardware Implementation Results

The hardware implementation is congregated with supply source, microcontroller board, gate drive supply, load, DC link, controller supply. The vital section of the control circuit is the Propeller µcontroller; is programmed to produce the pulsing signals for the six transistors to give out 5-level

output. ATMEL's AT89S52 microcontroller is used to produce gate pulses to proposed inverter topology. The AT89S52 is a high performance, low-voltage CMOS eight-bit µcomputer with 4K bytes of flash programmable memory. In addition, the design of AT89S52 is allowed to support two power saving modes which are software selectable. While the RAM, counters and timers are functioning, then the idle Mode will stop the CPU.

Table.4 Comparison of Traditional & Proposed MLI Topologies under Different Aspects

	Cascade H-Bridge [14]	Diode clamped [12]	Flying Capacitor [14]	Reverse-Voltage MLI [15]	Series-Parallel-1 [16]	Series-Parallel-2 [17]	Proposed Topology
Input DC Sources	2	1	1	2	2	2	2
Clamping Capacitors	0	0	6	0	0	0	0
Diodes	0	12	0	0	0	2	0
Generalized formula for switch count	$2(N-1)$			$(N-1)+4$		$(N-1)+2$	
Power switches	8	8	8	8	8	6	6

Six MOSFET's are used in the proposed topology and the MOSFET's used are Si4850BDY TrenchFET Gen IV power MOSFET with SO-8 single configuration. Drain-source voltage is 60V and gate-source voltage is ±20V with maximum power dissipation of 4.5 W at 25^0C. The hardware proto-type model of proposed 5-level MLI topology is illustrated in Fig.8.

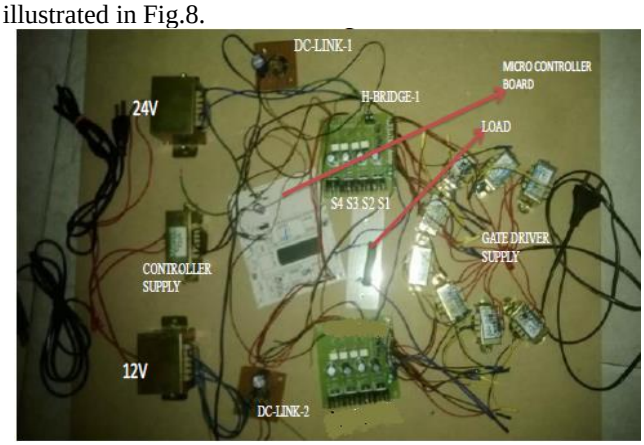
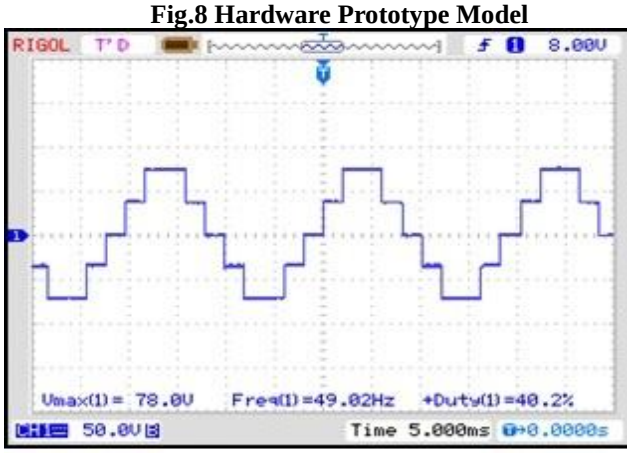
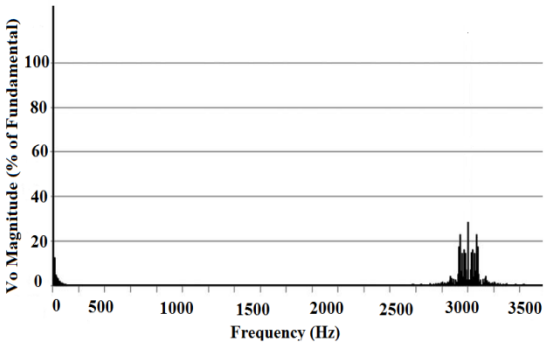


Fig.8 Hardware Prototype Model



(a) 5-Level Output Voltage Using Fundamental Frequency PWM Technique

The hardware results of proposed MLI- are depicted in Fig.9. In that, (a) 5-Level Output Voltage, (b) THD Analysis of Output Voltage. The 5-level stair-case output voltage is acquired by operating the respective switches in proposed MLI topology driven by proposed simplified PWM technique. The THD analysis of output voltage is greatly comply with the IEEE-519 standard limits, because of high switching frequency based simplified PWM technique and requires low-range filter units, increases the overall efficiency of the topology.



(b) THD Analysis of Output Voltage

Fig.9Hardware Results of Proposed MLI Topology

The comparison of traditional & proposed MLI topologies under different aspects is clearly illustrated in Table.4. The traditional MLI topologies require greater switching elements, DC sources, clamping diodes, balancing capacitors, over the proposed MLI topology. In general, this RV-topology requires 8 switches and 2 DC sources and non-utilization of any diodes and clamping capacitors. As well as, the both series-parallel formation topologies requires variant switches, the topology-1 requires 8 switches and 2 DC sources and topology-2 requires only 6 switches and 2 DC sources because the switches are replaced by diodes. Over all the topologies, the proposed MLI-topology requires 6 switches, 2 DC sources and non-requirement

of any additional diodes and balancing capacitors. Thus, it is most familiar in MLI-family and highly used in many high-power medium-voltage applications and best suited for DG applications, the proposed topology is technically and commercially so perfect.

V. CONCLUSION

This paper proposes the novel symmetric single 5-level MLI topology which is highly offered high-power medium-voltage renewable energy based DG applications. The performance of proposed topology is verified by both fundamental frequency PWM and proposed simplified PWM techniques, in that the proposed PWM technique has good operating characteristics. The proposed MLI requires only 6 six switches for generation of 5-level voltage over the classical MLI topologies. The characterization of symmetric 5-level MLI topology is driving by introducing a new simplified PWM technique which requires only two carriers instead of four carriers, then requires a low complex control gate drive circuitry. Proposed 5-level symmetric MLI offers fewer switches, gate drive circuits, reduced size, low cost, low switch stress and high efficiency can be attained over the traditional MLI topologies. The detailed simulation analysis of proposed 5-level MLI topology is validated by using computer Simulation tool and results are illustrated with proper comparisons. The feasibility of proposed 5-level compact MLI topology has been evaluated experimentally, results are presented. It is most familiar topology in MLI-family and highly used in many high-power medium-voltage applications and best suited for DG applications, the proposed topology is technically and commercially so perfect. In further recommendations, the proposed topology is designed for higher-levels with the requirement of fewer switching elements; likely same topology is defined as Asymmetrical formation.

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