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Magnetic Tunnel Junctions Design in Magnetoresistive Random Access Memory [MRAM] for FPGA Architecture

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Abstract*: An MTJ-MRAM circuit has been designed to function as Non-Volatile memory circuit using CMOS 45nm and 90nm Technology. The other existing memory circuits like SRAM and Flash are designed in 45nm and 90nm CMOS Technology and their output behavioral characteristic, power and delay parameters are obtained in order to compare with the performance of MTJ-MRAM. MRAM behavioral characteristics are compared with existing volatile and non-volatile memory circuits. The design has been carried out using Cadence Virtuoso – Electronic Design Automation (EDA) Software Tool. In Analog Design Environment (ADE), the advanced design and simulation is performed in virtuoso platform. The schematic for MTJ-MRAM is designed and simulations are carried out in 45nm and 90nm Technology using a test environment. The purpose of the research is to design memory circuit that gives non-volatility which can be implemented for FPGA architecture. Present FPGA architectures which are non-volatile based, have limitations and demands for a better non-volatile memory to be integrated within. The research demonstrates, MTJ-MRAM with better performance than existing flash based and anti-fuse based types of FPGAs. The paper compares power dissipation and delay of MTJ based MRAM with existing volatile SRAM and non-volatile Flash memories that are currently used in FPGA architecture. MTJ-MRAM shows non-volatile behavioral characteristics and also shows significant power and delay reduction when compared to non-volatile flash memory and SRAM volatile memory circuit.

Index Terms: Magnetic Tunnel Junction [MTJ], MRAM, SRAM, Non-volatility, Flash Memory, EDA, ADE

1. INTRODUCTION

In the era of growing technology and fast computation there is constant demand for computing systems to insists multiple computations to take place in which memory place a dominant role. Memory devices are basically classified as volatile and non-volatile memories. In volatile memory data is stored only till the power is on and it loses its data when powered off. While non-volatile memory stores the data even when the system is powered off.

SRAM is a class of memory which is volatile in nature as it loses its data when powered off [2,9]. Flash is a class of memory which is non-volatile in nature and it retains the data even after power off. FPGAs are basically classified based on the memory technology. SRAM based FPGAs are of volatile type while Flash based and Anti-fuse based FPGAs are of non-volatile type. Anti-fuse based FPGAs are only one time configurable and are not only for some specific application and hence Flash based is more advantageous among the non-volatile types but still is not more preferred than SRAM based as it offers more advantages than non-volatile types and still offers a disadvantage of volatility. This creates demand for new non-volatile memory type to be integrated to FPGA for better performance [12].Magneto-resistive Random Access Memory (MRAM) is a class of memory which gives the advantages of non-volatility. MRAM existed since long time and there are many variations in the construction of MRAM types.

There are two foremost characteristics of an electron namely 'charge' and 'spin' and the magnetism is due to the spin character of the electron. Spins in semiconductors offer a new approach towards integration of information storage and processing in a single material. Such devices in which both the electronic charge and as well as its magnetic moment (spin) are studied together are called as spintronic devices or spin electronics devices [1, 2].

Tunneling is a nano-scale phenomenon where under the right conditions, electrons can tunnel to very thin insulating materials causing load resistance, such structures are called Magnetic Tunnel Junction [MTJ] or Tunneling Magneto Resistance [TMR]. MTJ is the fundamental part of Magneto Random Access Memory and switching in MRAM occurs mainly due to MTJ. MTJ is a spin based device showing non-volatile characteristics working with principle of Magnetoresistance [MR]. MTJ basically is two layers of ferromagnets – one fixed and other is free layer as shown in figure 1 [5-8]. TMR is an effect that occurs in MTJ in which charges tunnel from one layer to other. Magnetoresistance is a phenomenon in which the property of the material will change its electrical resistance of a material to change the value of its electrical resistance when an external magnetic field is applied to it. MR effect is basically the property of materials causing resistance change due to magnetic field and it occurs in materials like magnetic, semiconducting and insulating materials. MR operates without any physical contact and can be used in sensors, hard disk drives and measuring electric current [4, 9].

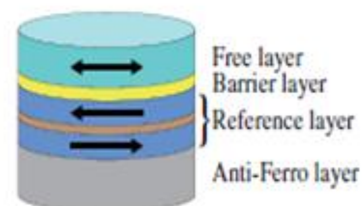

Figure 1: Magnetic Tunnel Junction [8]

One of the first generation MTJ is Field-Induced Magnetic Switching (FIMS) type which used Synthetic Anti-Ferromagnetic layers in MTJ [16]. The next generation MTJ is Thermally Assisted Switching (TAS) type junction which used an additional anti-ferromagnetic layer along with ferromagnetic layer as its

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MTJ [14,15]. In TAS when heated the cell, the current changes across the ferromagnetic and anti-ferromagnetic layers. TAS offered advantages like lower power, higher density and lower switching disturbance compared to FIMS type. But had bottleneck of switching speed which is limited by heating and cooling duration of TAS. Next type of implementation of MTJ is STT. STT is an effect in which the spin of the carriers in MTJ can be changed by applying spin polarized current [3, 17, 18].The next generation MTJ is combination of TAS and STT in which an additional anti-ferromagnetic layer is required to heat up the MTJ[13]. The next generation MTJ is implemented using Spin Hall Effect Spin Transfer Torque i.e. combination of SHE and STT [10,11].In this type the MTJ device is constructed using STT which was deposited on a heavy metal resulting in a three terminal device.

II. BACKGROUND AND MOTIVATION

FPGA performance is constrained by its volatile memory technology. Data configuration of SRAM FPGA is volatile and can be reconfigured in-circuit. In ANTI-FUSE based FPGA the configuration is set by "burning" internal fuses, the configuration is non-volatile but cannot be changed i.e. one time programmable. While FLASH based configuration is nonvolatile and is configured off-board but has increased internal leakage power. Due to the volatile nature of FPGA, the data is needed to be loaded each time on the device and the configuration time of the data on device increases due to iterations. The efficiency of the FPGA device is hindered hence the device demands non volatility with increased configuration speed. Novel non-volatile memory (NVM) based FPGAs need to be designed in order to improve the overall performance of the FPGA device. This is achieved by reducing configuration time and the power required to configure the data on the device by making the memory of the device non-volatile. It is described in this paper the construction of a non-volatile MTJ based MRAM for FPGA architecture. Starting from the modeling of basic MTJ cell a non-volatile memory circuit is demonstrated and compared with existing volatile and non-volatile FPGA memories. Also the power dissipation and access times of designed MRAM circuit is compared with existing FPGA memories.

III. MODELING MAGNETIC TUNNEL JUNCTION

An MTJ is basically the fundamental part of MRAM memory circuit and the switching of the memory circuit is dependent on the MTJ integrated with memory circuit. An MTJ changes its resistance depending upon change in magnetic orientation of “free” and “fixed” layer. In order to realize this resistance and make a memory circuit, switching element is required. CMOS transistor is one of the choices for switching purpose. The programming of the element is done mainly by current sink. The current pulse through the switching element and Bit line provide magnetic field to MTJ and changes the resistance across the MTJ. The pulse is more than enough to flip the orientation of MTJ layers and store bits. Depending on the supply voltage the pulse is generated and the value of the resistance that MTJ offers changes accordingly [4,5].

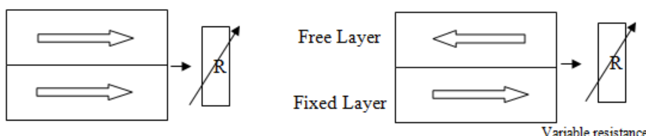
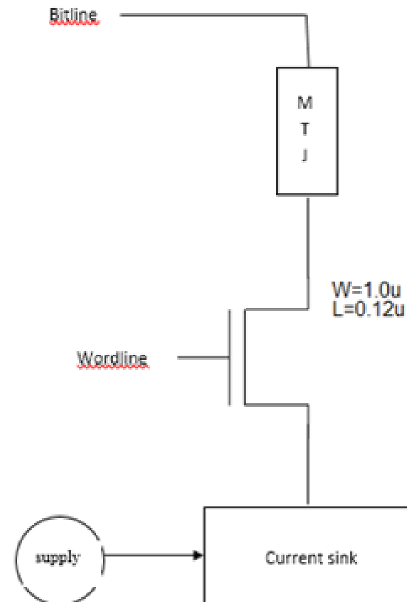


Figure 2: Resistive Element from MTJ

IV. DEVELOPMENT OF MTJ BASED MAGNETIC RANDOM ACCESS MEMORY

One of the main functionality of the memory is characterized as its data saving capability and through which the memory is classified as either volatile or non-volatile type. One such non-volatile characteristic is obtained by Magnetic Tunnel Junction (MTJ). The orientation of layers in MTJ offers two states to MTJ namely Parallel and Anti-parallel states. As the carriers in the layers orient, they result in parallel and anti-parallel states. Each state offers some resistance and hence the MTJ can be modeled as a Resistive element offering high and low resistance depending on the state the MTJ is offering. Various methods are employed to model MTJ. The proposed method uses a current source to generate current pulse, which forces to change the orientation of charges in MTJ and hence the alignment of the layers in MTJ structure.



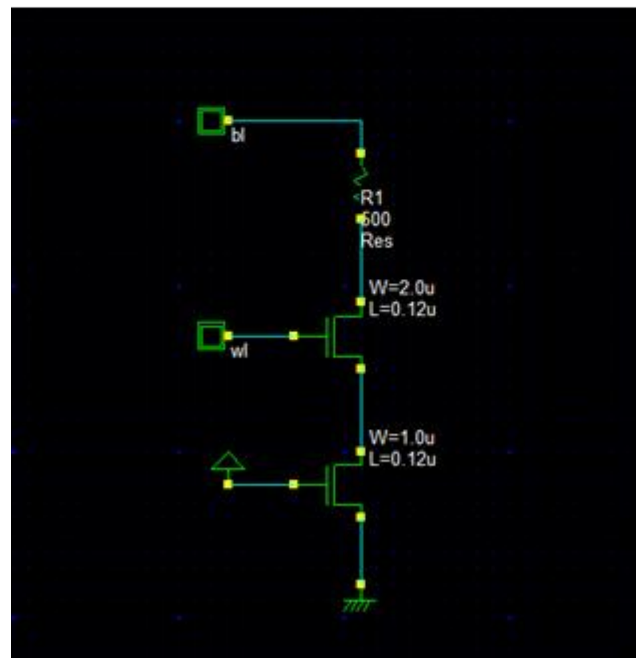


Figure 3: schematic of MTJ MRAM

Basically an MTJ changes its resistance depending upon change in magnetic orientation of the “free layer” with respect to “fixed layer” or “reference layer”. In order to exploit this variation in resistance and build a memory cell this can be addressed with reliable read and write operation with the help of switching elements. Generally, CMOS transistors, semiconductor diodes or Bipolar Junction Transistors are various choices available for this purpose in order to read the MTJ state (resistance). These switching elements also isolate the MTJ device from the word line when that particular device is not addressed.

These cells are programmed by sending a pulsed current through word line and bit line. The whole

memory has to be designed in such a way that the field from a single pulse on either line is not adequate to flip the orientation of the MTJ "free layer" but the combination of fields generated by these two lines is large enough for switching to occur. MTJ can be modeled as shown in figure 3, the circuit is designed using cadence tool in 45nm and also 90nm Technology.

4.1 Case 1: Storing Logic "1"

When the current pulse is given to MTJ through a transistor called cell select transistor, the current pulse varies the charge orientation, depending on the strength of the current pulse produced by the second pulse produced. The current pulse generated from current source is given to MTJ through cell select transistor and when word-line is high and the other pulse is produced by bit-line i.e. when word-line and bit-line are equal to "1" then the "free layer" of MTJ is oriented in a direction which is opposite to that of the "fixed layer". Both the layers of MTJ are aligned in opposite direction and they are said to be in Anti-Parallel state offering high resistance. Therefore, when word-line and bit-line are equal to "1" the MTJ stores Logic "1" in the memory cell.

4.2 Case 2: Storing Logic "0"

The current pulse is given to MTJ through a cell select transistor controlled by word-line and the second pulse is applied through bit-line. The current pulse through the bit-line given to MTJ changes the orientation of charge carriers in the "free layer". Due to the alignment of charges in two layers the layers are now said to be in Parallel state offering low resistance. Hence when word-line is high "1" and bit-line is low "0" the MTJ stores logic "0" in its memory cell.

V. RESULTS

Using the design flow in cadence virtuoso schematic tool, the MTJ one transistor and one MTJ element design was done. Also Flash and SRAM circuits were designed using cadence virtuoso schematic editor and finally the analysis was done in various aspects for all the designed circuits. The waveforms for bit line, word line and output for MTJ-MRAM, NOR-Flash and SRAM are shown in figure 4, figure 5 and figure 6. It is observed from the output waveforms that when word line (access transistor) is powered the output follows the data i.e. bit line for MTJ-MRAM and for NOR-Flash circuits showing Non-volatile feature. While when the access transistor is powered in SRAM, the output follows the data only when Word-line is high else when word-line is low the output follows the previous output only.

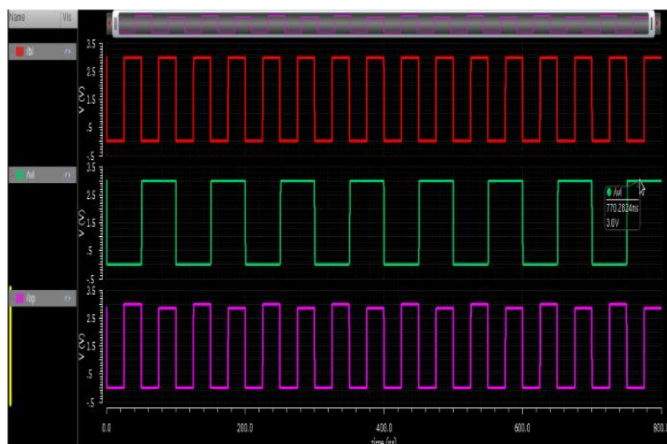


Fig 4: Behavioural waveforms of MTJ- MRAM

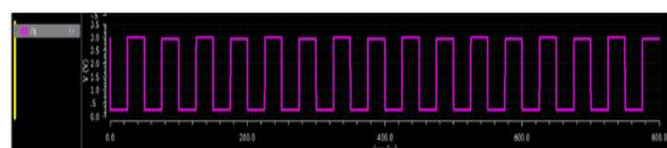


Fig 5: Behavioural waveforms of Nor Flash

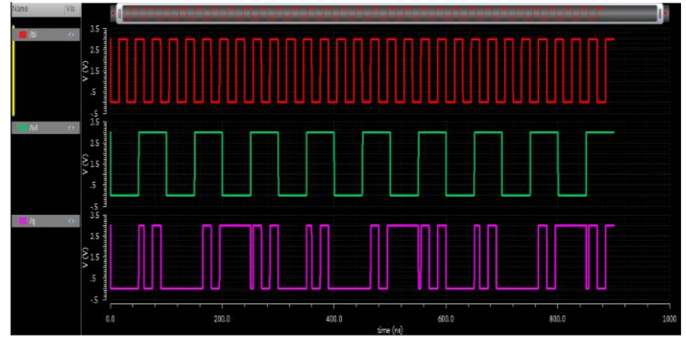


Fig 6: Behavioural waveforms of SRAM

The circuits are designed in 90nm Technology and power and delay are estimated. For the designed MTJ-MRAM circuit on 90nm and 45nmTechnology, the power and delay are estimated. The power consumption is found to be ~19.97nW and Time Delay is found to be ~15.14fs for 90nm. While the power consumption is found to be ~11.73nW and Time Delay is found to be ~71.85fs for 45nm. The power consumption, circuit delay time and its prominent feature in comparison with existing volatile and non-volatile memory circuits are recorded in table 1.

A detailed comparison between different SRAM, NOR-Flash and MTJ-MRAM memories designed in 90nm technology is shown in table 1. The observation shows that MTJ-MRAM exhibits Non-Volatile feature offering good speed and low power consumption.

Table 1: Comparison of SRAM, FLASH and MRAM memory circuits

Memory	Delay	Power	Feature
SRAM (90nm Technology)	$64.11x10^{-9}s$	151.3nW	Volatile
NOR-Flash (90nm Technology)	$4.568x10^{-12}$ s	5.4nW	Non-Volatile
MTJ-MRAM			
180nm Technology			Non-Volatile
90nm Technology	$15.14x10^{-15}$ s	19.97nW	Non-Volatile
45nm Technology	$70.85x10^{-15}$ s	11.73nW	Non-Volatile

VI. CONCLUSION

From the behavioral analysis of circuits and the timing analysis of the simulations carried out in the paper the following conclusions can be made:

1. The VLSI design of MTJ-MRAM shows that there is a significant delay reduction of about 3 times i.e. the speed is increased by 3 times (both in 45nm and 90nm) compared to Flash Non-Volatile memory. The VLSI design of MTJ-MRAM of 45nm shows power consumption is reduced to half of that required in 90nm design.
2. The design of MTJ-MRAM also shows significant power and delay reduction of about 6 times compared to volatile SRAM circuit designed in 90nm technology. The design of 45nm MTJ-MRAM also shows a bottleneck of delay in the circuit which is increased ~55fs compared to 90nm design.
3. The design of MTJ-MRAM also offers Non-Volatility feature. By designing

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MTJ-MRAM in 90nm technology for FPGA architecture, the configuration time of FPGA decreases and speed up overall FPGA process with added advantage of minimized power consumption compared to SRAM based FPGA.

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