A Novel RF CMOS Ultra-Wide-Band LNA at 2.66 - 3.75 GHz in 180nm Technology

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Abstract: The designed UWB LNA is exhibits a less Noise and large Gain with better input and output matching. The designed Low Noise Amplifier simulation by using Cadence tools in 180nm CMOS Radio Frequency using TSMC technology. The designed LNA is of Common Gate (CG) with Cascade stages are used in different communication applications. Like WiMAX, Wi-Fi and WLAN. This (USB LNA) Low Noise Amplifier achieved a gain of Above 20 dB and Noise Figure (NF) achieved a 3.782 dB at frequency of 3.0642 GHz to 3.211 GHz. The simulation result attains with bandwidth is1.0921 GHz with the center frequency (f0) at 3.132 GHz and it consumed 13.234 mW of power from a 1.8 V power supply and 1 dB compression point of -16.223dBm is attained.

Index Terms: COMS, LNA, 1dB COMPRESSION POINT, NOISE FIGURE, TSMC, WiMAX.

1. INTRODUCTION

Wireless Communication is playing an important role in modern communications like Wi-Fi, WiMAX, WLAN systems. The high speed and high data rates are demand in wireless communications and it is increased day by day. According to IEEE 802.16b standard the data rate is 11Mbps and for IEEE 802.11g standard the data rate is 55Mbps at operating frequency 2.4 GHz [1][2][3]. The modern UWB Systems can handle large data rate for wide frequencies with short ranges with low power consumption. The IEEE 802.153a standard UWB frequency is 3.1 to 10.6 GHz [4]. The LNA is the important block for any wireless communication transceiver front end. The best designed low noise amplifier can provide better input, output matching, minimum return loss, high Gain and low Noise parameters for increasing sensitivity of receiver. The LNA also offer less power consumption and less area occupied on the die. These total literatures are available in references [2]-[12]. To design UWB LNA at 2.4 GHz is possible with several topologies; the conventional distributed topology has the drawback of power consumption [5]. The resistive feedback topology is better for UWB LNA, but maintain of the high Gain and low Noise Figure simultaneously is difficult [6]. To achieve all requirements of WiMAX receivers for CMOS technology with better performance. The present design first stage is Common gate topology the second stage is common source-common gate topology cascading. So that it attains better performance of less power consumption, broadband matching with few resistances and with two inductors.

II. PROPOSED DESIGN PROCEDURE

The proposed design has two stages, the first stage is Common Gate topology and second stage has Common Source with Common gate topology. The M1, M2 and M3 transistors are used in designed circuit as shown in figure1a,1b. The designed topology can attains better input output matching with low power consumption by common source, better power matching and wideband provide by common gate stage. By neglecting parasitic component of resistance at source inductor Ls, and loading effect of second stage in the design. Therefore the input impedance Zin provide by the circuit is

\[ Z_{in} = \frac{sL_{s1}}{1 + (g_{m1} + sC_{gs1})L_{s1}} \]  

(1)

Where g_{m1} is trans-conductance, C_{gs1} is gate to source capacitance of first stage of transistor M1. At DC lower 3dB frequency the impedance is zero. The Ls1 offers low impedance at ground for lower frequencies. The common gate offers wideband input matching, it compensate with narrowband frequency response. The transfer function of the first stage given as

\[ V_{f1} = \frac{(1 + g_{m1}r_{ds1})R_{L1}}{(1 + \frac{R_{S}}{sL_{s1}}) + (r_{ds1} + R_{L1})(1 + g_{m1}r_{ds1})R_{S}} \]  

(2)

The value of RL1 is very important since to determine the value of gain and gate biasing for both first and second stages. The size of M1 is playing an important role for proper input matching. In proposed design the value of Ls1 is 8.3nH and the impedance matching value is 280Ω for total design it is acceptable value for the designed model.

The next stage is Common Source –Common Gate cascaded configuration and offers high frequency Gain and estimated higher 3dB bandwidth for low noise amplifier. The cascade transistor M3 offers better isolation, high Gain and high frequency response. The peaking inductor Lp with 10nH is resonating with parasitic value of C_{D3} at drain of the M3 transistor. The transfer function for second stage is shown in equation 3.
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\[ V_{in} = \frac{(1 + g_{m}r_{ai})R_{L}}{(1 + \frac{R_{S}}{sL_{C}} + sR_{C}C_{p}) + (R_{i} + R_{L})(1 + g_{m}r_{ai})R_{S}} \]  

(3)

The \( M_3 \) transistor size should minimize in-order to minimize parasitic capacitance of the proposed design. The quality factor \( (Q) \) values of inductors chosen high in order to achieve maximum Gain and narrowband characteristics. In the proposed design the Quality factor value for the \( L_{D1} \) is selected as achieves flat Gain of entire design. An extra resistor \( R_{S2} \) is added as 50\( \Omega \) to decrease the quality factor \( (Q) \). By keeping the value of the blocking capacitor \( C_{dc} \) as approximately 180 fF and \( L_{dc} \) as 0.05 nH as series connection to block any unwanted DC current. The 100k\( \Omega \) resistor \( R_o \) is added as shunt to make output open.

![Circuit Diagram](image1.png)

Figure 1.a. Circuit diagram of designed CMOS USB LNA

![Schematic Diagram](image2.png)

Figure 1.b. Schematic diagram of designed CMOS USB LNA

### III. RESULT ANALYSIS

#### A. \( S \)-parameters

The designed low noise amplifier (LNA) simulation results are shown in figure.2. The \( S \) parameters input reflection coefficient \( S_{11} \) of proposed LNA remains always negative and from frequency of UWB of 1.392 GHz onwards attains below -10 dB point. The minimum value as -23.43 dB at frequency of 3.12 GHz and at 4.152 GHz. The parameter \( S_{11} \) is lower than -10dB for proper input matching. In proposed design the \( S_{11} \) is -23.2 dB is obtained for perfect input matching at 3.132GHz of center frequency.

![Parameter Graphs](image3.png)

Figure 2. Parameter, \( S_{11}, S_{22}, S_{21} \) and Noise Figure for an ultra wideband LNA.

The input-output isolation parameter \( S_{12} \) is attained -47dB and it can maintain stable value of -52dB after 3GHz. It offers the -51dB of input --output isolation at center frequency 3.13GHz. The forward gain \( S_{21} \) parameter value is reaches positive value at 1.2 GHz and at frequencies 2GHz to 5.4GHz it attains above 10dB. The forward gain parameter \( S_{21} \) is 20dB from 3.061GHz to 3.23GHz. Therefore it is comfortable gain of the proposed design. The bandwidth is 1.09 GHz from frequencies 2.66 GHz to 3.75 GHz, but it is compromised parameter. The Output reflection coefficient parameter \( (S_{22}) \) is also negative. It is achieved below -5.2 dB for frequency 2.81 GHz.
GHz to 3.4 GHz. The $S_{22}$ is -9.85dB is -10 dB at 3.1 GHz it is within the specifications of IEEE standards.

b. Noise Figure

The Noise Figure as lower than 4dB according to IEEE standard specifications of cascade topologies. The proposed design achieved a 3.442dB at center frequency of 3.132 GHz. The Noise Figure(NF) maintained low value at frequency range from 3.132GHz to 3.927 GHz and it maintain small value of Noise figure(NF) is 3.132 dB at 1.425 GHz and it also maintain 3.72dB at 428 MHz to 3.72GHz. The noise figure (NF) remains 4 dB that is 1.882 GHz to 6.432 GHz. The proposed design common gate (CG) characteristics have supported in order to maintain this less (NF) noise figure.

![Noise Figure](image1)

Figure 3. Noise Figure for an ultra wideband LNA

c. LINEARITY

The linearity of the LNA is calculated by the 1dB compression point. The calculated and measure 1dB Compression point is -16.2dB. The power consumption is 13.4mW for overall performance of the proposed work.

![1 dB compression point](image2)

Figure 4. 1dB Compression point is -16.2dB for an ultra wideband LNA.

IV. CONCLUSION

The proposed LNA design achieved a better performance with respect to design complexity, low noise, high forward gain, and less power consumption which is used for (UWB) ultra wideband WiMAX Applications. An UWB CMOS LNA has been proposed in a 180 nm RF CMOS technology process of TSMC using common gate, common source –common gate cascade topology. The forward Power gain is above 20 dB. The input matching is $> -17.2$ dB in the bandwidth region with nearly -23.12dB at center frequency $f_c$. The output matching is -10 dB at center frequency $f_c$. The 1 dB compression point is -16.122dBm and the other parameter Noise Figure (NF) is 3.852 to -3.782 dB with 3 dB BW of 2.662 - 3.752 GHz.

REFERENCES


AUTHORS PROFILE

**First Author**: Srinivasa Ramana Reddy, a graduate in ECE from IETE, New Delhi and M.Tech (I&C) from JNTUK, Kakinada. He is currently as an Assistant Professor in the ECE dept., at CRIT, Hyderabad since 2004. His key area of research is VLSI Design in analog and digital systems, and has 8 publications in peer-reviewed international journals and conference proceedings. As a facilitator for continuous learning, he has brought together Faculty, Researchers, students and Industry.

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