Implementation of Power Optimized Binary Multiplier Based On Fast Binary Counters Using Symmetric Stacking

J.Selvakumar, S.Siddharth

Abstract: ***The objective of this work is to introduce a high speed binary counters based on symmetric stacking which is used to design the modified booth multiplier for generation of fast partial products. Using the proposed fast binary counters technique we have devised a strategy for partial product reduction in complex multiplier circuits. By reducing the multiplier partial product complexity, which lead to significant reduction in area and power of the proposed multiplier design.The implementation of 8-bit and 16-bit booth multiplier has been carried out using 90 nm technology in cadence Innovus environment . The Synthesis results states that using proposed fast binary counter technique the area is reduced by 12% and the power is optimized by 8%.***

Index terms: counter, multiplier, netlist, Physical design

I. INTRODUCTION

Multipliers are mostly used in the present digital signal processors, microprocessors and many other applications. In the microprocessors and signal processing domain the speed and power are most important parameter in the performance. In the digital signal processing, the multiplier circuits are used to perform the convolution (repeated Multiplication and addition operation) and filtering operation and also the multiplier circuits are mainly used in the arithmetic logic unit.

Many advance technology are there now a days for multiplier circuits, either they concentrate in reduction in area, power or high speed. High Speed and low power designs are the main objectives for next generation multiplier circuits.

There are many types of multipliers available today in use, but one of the main multiplier that was used for the digital circuit implementation is binary multiplication. The widely and most commonly used multiplier algorithm is "ADD and Shift" algorithm. In this work we have utilised the modified booth algorithm that has an advantage of reducing partial products, so there will be less area and power. It is widely accepted for the signed multiplication operation, in this algorithm both the negative and the positive value are not modelled as a different value, but they are treated as same value.

In out proposed methodology we have introduced a new type of fast binary counters based on symmetric stacking as partial product generator in the modified booth multipliers technique. Use the proposed technique we have implemented a binary multiplier circuits for 8-bit and 16-bit multiplication operation. Since we aim at partial product reduction ultimately our proposed technique provide higher percentile of savings in area and power when compared with existing method. The proposed multipliers are functionally verified for prelayout simulation using ModelSim software. The advantage of our proposed method is concluded with arithmetic metric in the result section..

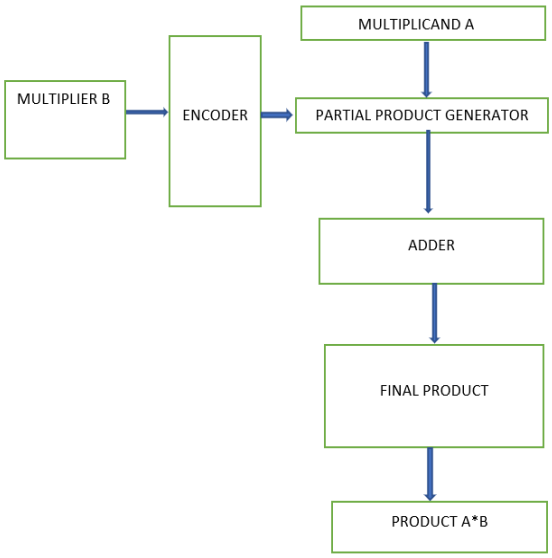

Fig. 1. Block diagram for modified booth multiplier

After pre-layout simulation the netlist was done by synthesis process using Cadence EDA RC Compiler. In synthesis part we are taking netlist for 8-bit and 16-bit multiplier circuits, which was one of the inputs to the back-end process of VLSI and we are done implementation for proposed multiplier circuits with tape-out of 90nm. This includes the floorplan power plan, placement, routing and this back end process can done in Cadence innovus.

II. PREVIOUS WORK

Wen-Chang Yeh et.al., **[2]** have proposed an algorithm called Three-Dimensional Reduction Method(TDM) is proposed to improve the performance of traditional Modified Booth Encoding(MBE) method, which shows better results ,where speed of the circuits is high and delay of the circuits is less

S. Kuang et.al., **[3]** have discussed the proposed method called regular partial product array, which reduces the partial product stage, reducing the partial product stages reduces the area and power.

Ravindra P Rajput et.al., **[4]** have proposed a method called Signed-Unsigned Modified

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Booth Encoding (SUBME), modified booth encoder circuits generates only half the partial product and both signed and unsigned number executed by the same multiplier unit, So area of chip and power is reduced.

Chandrika Santhosh et.al., **[9]** has implemented Wallace tree multiplier using fast binary counters based on symmetric stacking which shows better results.

III. INTRODUCTION TO SYMMETRIC STACKING

Symmetric stacking technique based on fast binary counters [1], here the basic idea is to use stacking circuits for 3-bit digital circuit and there by grouping the 1-bit and the same have been extended proposed some method to combine the pairs 3-bits into 6-bits stacking. These are converted into the binary counters and it produces the 6:3 fast binary counters, the main advantage in this circuit is, in the critical path there was no XOR gates were presented. If there was no XOR gates it will increases the speed of the circuits and utilizes the area efficient.

This counter used to generate partial product, which we are going to implement in modified booth multipliers for less power consumption and less area.

IV. MODIFIED BOOTH MULTIPLIER

Normally, we are implementing the many operations like subtraction, addition, division and multiplication. These operation of arithmetic is performed in the daily life. Here every operation has different techniques, In this work we are going to implement multiplier circuits, there are many types of algorithm is existed to do for multiplication operation, among many multipliers, Binary multipliers is commonly used in digital circuits. There are many methods to implement the binary multipliers, one of the most used method is booth multiplier.

4.1. Introduction to Booth Multiplier

Booth multiplication was invented by Andrew Donald Booth. Booth multiplication is defined as method of multiplication of binary numbers in two's complement. It was the easier method to do multiplication operation of the two binary numbers and this was implemented with repeat addition operation, and we are implementing the booth multiplier algorithm and again there was some modification in booth algorithm and it was termed as modified booth multiplier algorithm.

4.2. MODIFIED BOOTH MULTIPLIER

Booth multiplier consists of three methods (i) partial product generator (ii) reducing the partial product (iii) final adder. Modified booth algorithm is also known as bit-pair algorithm or Radix-4 algorithm. Here we are implementing the modified booth algorithm operation to reduce the number of summands in the multiplier circuits, generally in the normal multiplier for the n-bit we need n-summands, but for the modified booth multiplier algorithm for the n-bit we requires only n/2 summands, Here half of the summands were decreasing in this algorithm, so the operation of the modified booth multipliers speed is high due to reducing the number of summands, so this multipliers is considered as one of the fast multipliers. In this radix-4 algorithm, multiplier column which means second column was to be recoded and this can be multiplied by 0 +1,-1,+2,-2 and after doing this we are pairing the two bits, so it also called as bit-pair algorithm. By pairing these bits we are reducing the partial product, so operation of speed is increased. The truth table of radix-4[6] is given in table-1.

Table .1 Truth Table for Radix-4 Booth Multiplier

B0	B1	B2	operation
0	0	0	0
0	0	1	+1
0	1	0	+1
0	1	1	+2
1	0	0	-2
1	0	1	-1
1	1	0	-1
1	1	1	0

4.3 Modified Booth Multiplier Based On Fast Binary Counters using Symmetric stacking technique

In Previous Work[3] they used some techniques called Regular Partial Product Array, to reduce the partial product stage in the multiplier, and It also reduces area and power, but Some Advance technique came now a days to reduce the partial product stages, One among the method is called Fast binary counters Using Symmetric Stacking [1]. This method is already used in wallace tree multiplier [9], which shows better results. In this proposed work we are implementing modified booth multiplier using fast binary counters based on symmetric stacking. It reduces the partial product stages.

Normally for reducing partial products we are using the full adders or compression techniques to reduce the partial product, this shows better results, however, some advance techniques are existed now a days to reducing the partial product, which are better than the compression techniques in-terms of reducing the partial product, Here we are using one of the better technique called fast binary counters based on symmetric stacking which reduces the partial products and the area occupied and power consumption is less when compared to the existing one.

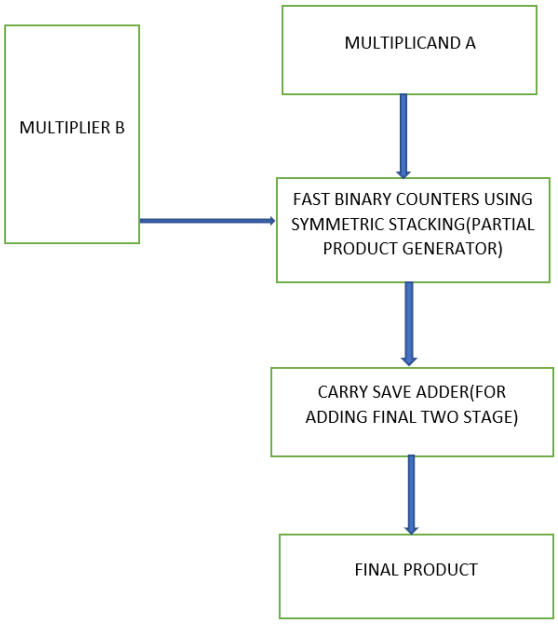


Fig. 2. Block Diagram for Modified Booth Multiplier Using Fast Binary Counters Based On Symmetric Stacking.

Fig 2. represents the block diagram of modified booth multiplier using Fast Binary Counters based on symmetric stacking, Here we are using the above counters as partial product generator this reduces the partial stages and Carry save adder [8] is used for adding the final two stages.

Fig 3 represents the stage reduction diagram of 8-bit multiplier, Here we going to reduce the partial stage,
In this diagram it denotes how stage were reducing, We are using 6:3 fast binary counters using symmetric stacking to reduce the partial stages, though it was 6:3 counter this take six product stage taken as input and gives output as sum,carry1,carry2, Here we reduces six stages of the partial product stages is reduced into three stages and later for some stages we are using 5:3 counters, 4:3counters we are reducing some stages and finally using full adders and half adders, we are reducing the remaining stages. This reduction have to be done up-to the stage was reduced in to the two rows and after stages was reduced we are doing final addition and that was done using the carry save adder[8]. The same method we are applying for the 16-bit multiplier, here all the fast binary counters like 7:3,6:3,5:3,4:3 counters and these fast binary counters were used to reduce the partial stage of 16-bit multiplier.

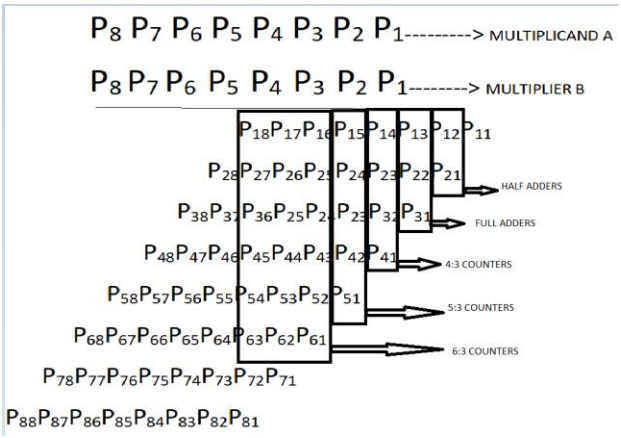


Fig.3 Stage Reduction Diagram For Modified booth Multiplier Using Symmetric Stacking.

Simulation of this proposed 8-bit and 16-bit multiplier using the fast binary counters which reduces the partial product and this work is done in the model sim software, which has better results compared to existing one. The simulations results for the proposed work is described in fig.4 and fig.5.

V. RESULTS AND DISUCSSION :

Fig.4 Simulation Results of 8-Bit Multiplier

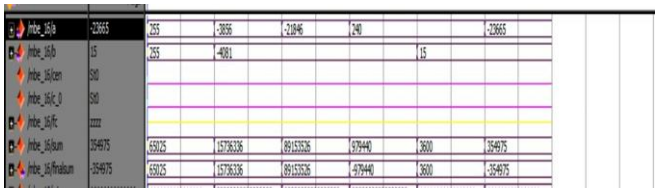


Fig.5. Simulation Results of 16-Bit multiplier

TABLE:2-SIMULATION RESULTCOMPARISION

No. of Bits	MULTIPLIER	AREA [LUT'S]	POWER [uW]
8	Conventional Booth multiplier[2]	295	452.78
	Existing[3]	286	440.56
	Proposed	216	416.5
16	Conventional Booth multiplier[2]	1015	2867
	Existing[3]	990	2778
	Proposed	910	2367

Synthesis is the process of changing your RTL design in to the gate-level netlist. As we are doing Physical design flow for the above circuits, we must synthesis the above circuits for taking the netlist, netlist is nothing but connections of gates. Netlist is the one of the main Inputs to the Physical design implementation. Here we are using Cadence RC for taking the netlist. The RTL schematic view for 8-bit and 16-bit multiplier is described in fig.6and 7.

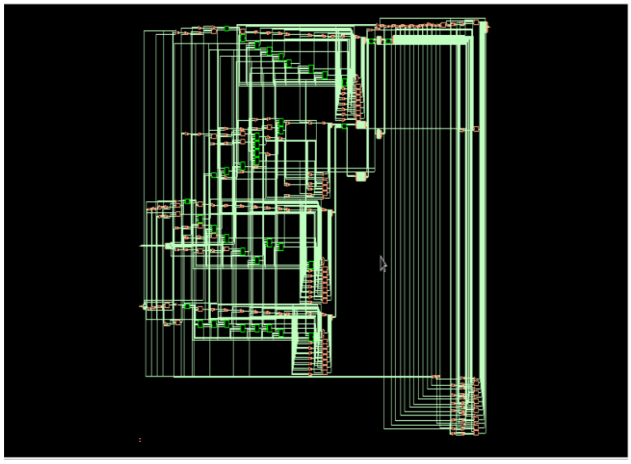


Fig.6. RTL Schmatic View for 8-bit Multiplier

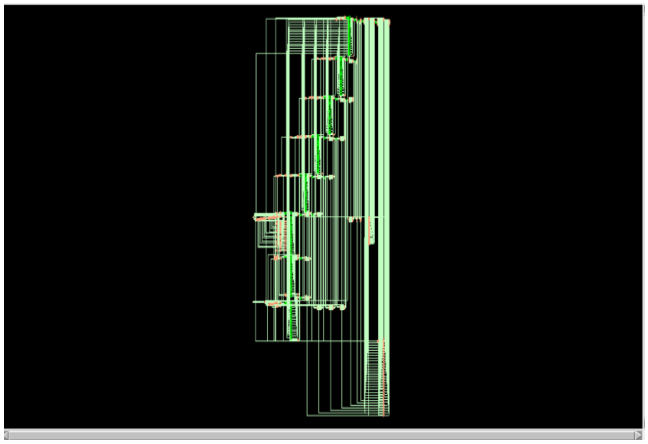


Fig.7. RTL Schematic view for 16-bit Multiplier

VI. PHYSICAL DESIGN IMPLEMENTATION

Physical design is the back end process in the VLSI Here we are designing the chip including placing all the cells into the core area and do the routing.

6.1 Design Import Format

It was the first stage in the physical design. In synthesis process the RTL code is converted into netlist. In the design import all the input files that required for physical design are read by tool. By using this info the design process will starts.

Various inputs to the physical design can be explained below

- Netlist
- SDC
- DEF
- LEF

Here we are using 90nm technology to implement the physical design process.

6.2 Floorplan Details

Floorplan is the process of determining the macro placement into the core/chip area. The floorplan stage of proposed work is described in fig.8 and 9

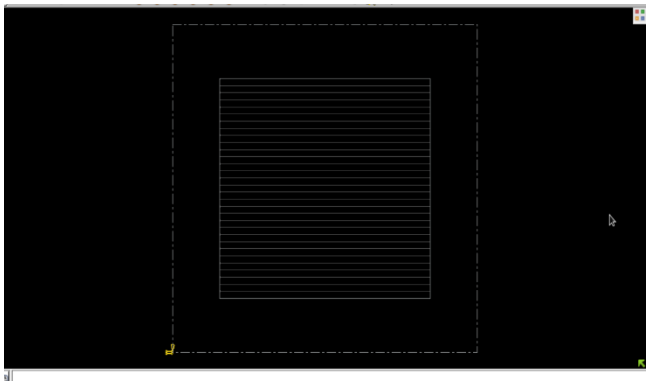


Fig.8. Floorplan for 8-bit Multiplier

Here no macros were placed because there was no macros present in the 8-bit multiplier circuit.

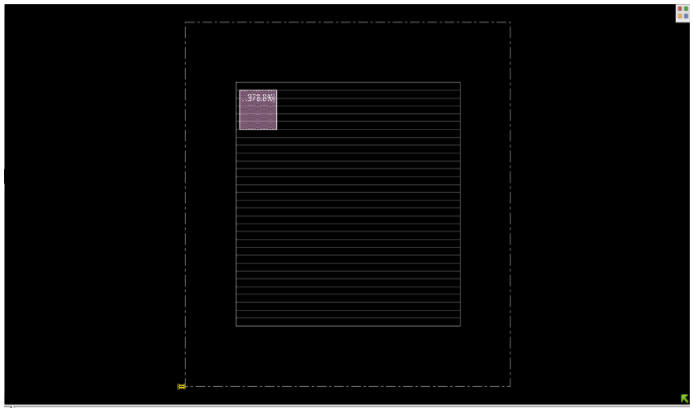


Fig.9. Floorplan for 16-bit Multiplier

6.3 Power Plan Analysis:

Power planning is done to provide uniform supply voltage. VDD and VSS rings are formed around the core and macros. Power straps are created in the core Rings. Standard cells rails are create to tap power from power straps to standard cell power or ground pins. Power plan stage for proposed work is described in fig 10 and 11.

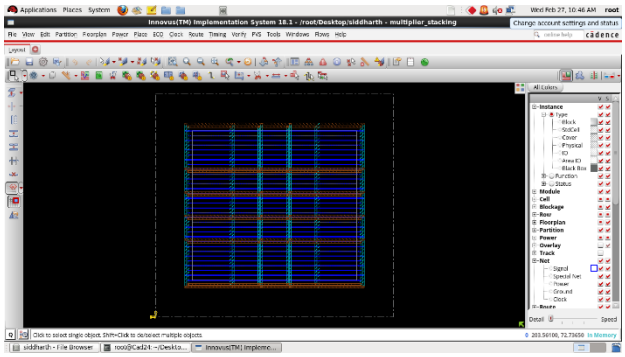
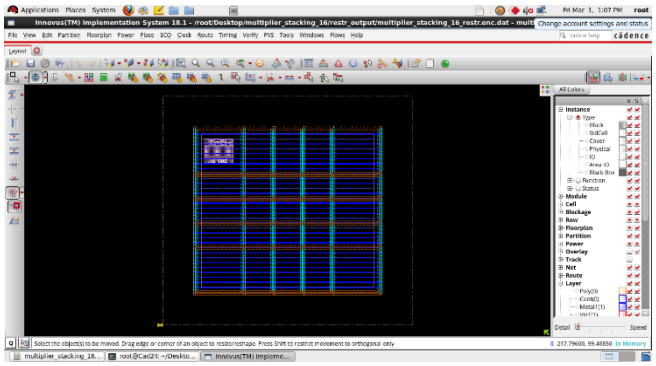


Fig.10. Power Plan for 8-bit Multiplier



6.4 Introduction to Placement aspects

In placement we are giving legal location to all standard cells in design. Exact placement of modules(modules can be gates, standard cells)can be done in placement stage. The placement stage of proposed work is described in fig 12 and 13.

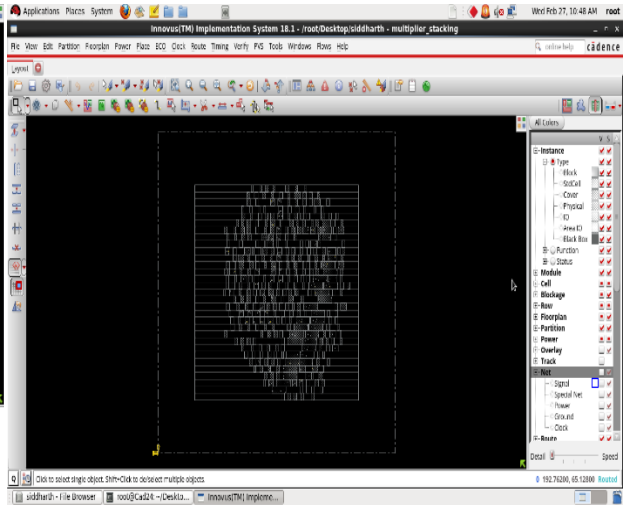


Fig.12. Placement Stage for 8-bit Multiplier

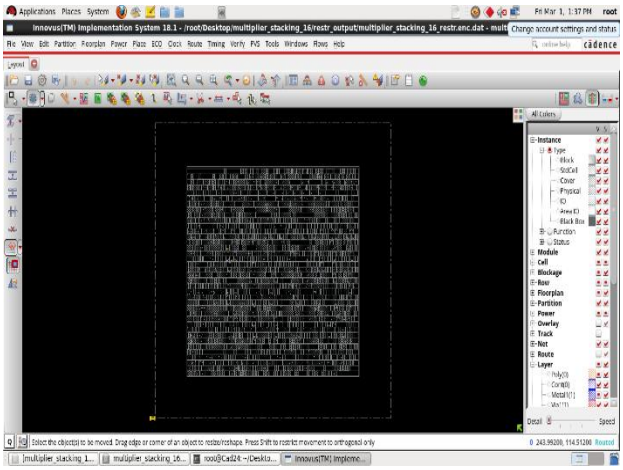


Fig. 13. Placement stage for 16-bit Multiplier

6.5 . Clock Tree Synthesis :

CTS mean clock tree synthesis which means delivering the clock to all sequential elements. Meeting clock constraint requirements like clock skew, insertion delay.
Though our circuits are combinational so it doesn't require any clock. Hence there is no CTS stage exists.

The routing stage of proposed work is described in fig.14 and 15.

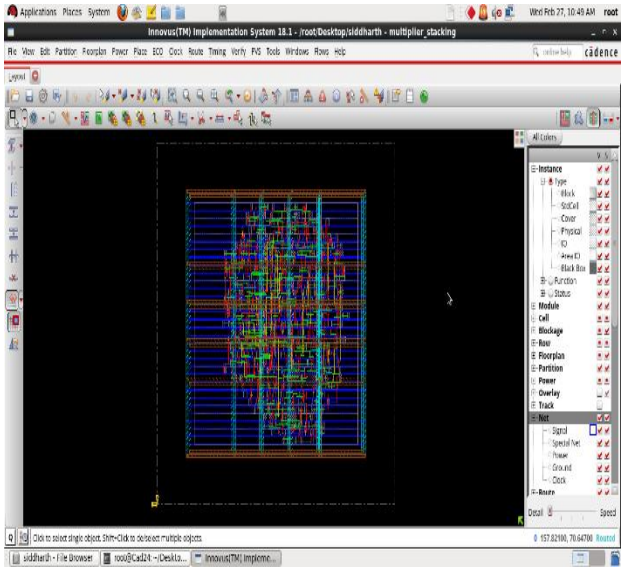


Fig.14. Routing Stage for 8-bit Multiplier

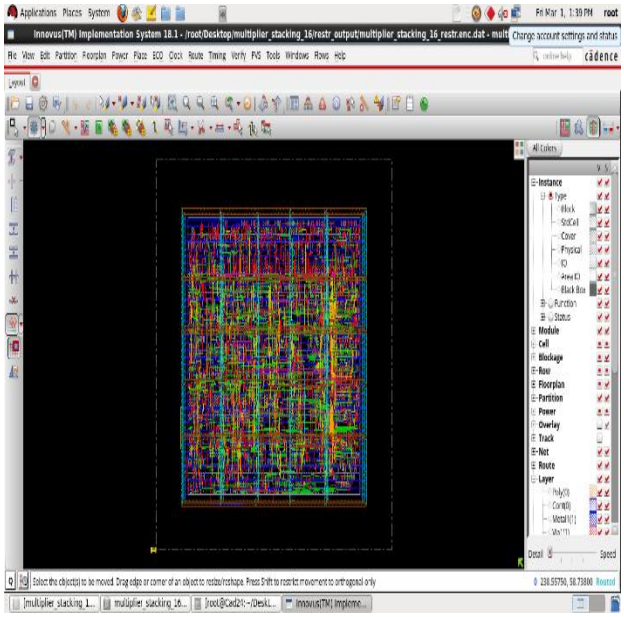


Fig.15. Routing Stage for 16-bit Multiplier

Table.2. Power and Area Report after Physical Design:

MULTIPLIER	**AREA(um^2)**
8 bits	1971
16 bits	7682
MULTIPLIER	**POWER(mw)**
8 bits	3.2
16 bits	6.9

VII. CONCLUSION AND FUTURE WORKS

Thus we conclude proposed low power optimization binary multipliers using fast binary counterspower and area are reduced 12% and 8% respectively compared to existing and this work caried out carried out using 90 nm technology in cadence Innovus environment.

In case the proposed technique is extended for 24-bit and 32-bit booth multiplier, the percentage of saving will be more than 15% for area and power.

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