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Efficient Realization of a Novel Barrel Shifter in Cadence SoC Encounter

K. Murali Chandra Babu, P. A. Harsha Vardhini

Abstract*: Reversible logic has the current development for the reason it consumes low power, which is the minimum requirement in the design of VLSI. A barrel shifter is the one which shift, rotate the data it is designed by using reversible gates. A novel Barrel shifter was designed in which it occupies less area with less delay. The proposed reversible barrel shifter was designed in VERILOG HDL and is simulated in XILINX ISE 12.4 simulator and chip level design was implemented in SoC encounter.

***Index Terms*: Barrel shifter, SoC, reversible gate, garbage ouputs.**

I. INTRODUCTION

A. *Reversible Logic*

If the inputs can always be traced at the outputs is called reversible computation. Reversibility is the one which has one to one mapping between the inputs and outputs that is each input has the unique output and vice-versa.

B. *Reversible Gates*

A reversible gate consists of n number of inputs and n number of outputs with one to one mapping. It contains more number of floating outputs to make equal with the inputs and to maintain the reversibility property these outputs are called garbage outputs. Therefore data can be retrieved from these garbage outputs. There are several reversible gates are Fredkin gate which acts as AND gate and Feynman Gate is used to copy the output and avoids the fan-out problem in reversible logic

C. *Barrel Shifter*

Barrel shifter is a combinational circuit where the data can be shifted towards the left, right. It consists of n-inputs, n-outputs, k selection lines which controls the shifting operation of data bit. Barrel shifter is a unidirectional which allows the data to be shifted towards right (or left) and bidirectional where the data can be rotate or shifted both sides. A barrel shifter can be denoted as (n, k) barrel shifter. Section II presents the design of reversible barrel shifter, section III illustrates the simulation results, implementation of the proposed design on SoC encounter is presented in section IV and concluded in section V.

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II. DESIGN AND IMPLEMENTATION OF REVERSIBLE BARREL SHIFTER

A conventional reversible barrel shifter can be modeled by using multiplexers. is designed by using Fredkin gate and the outputs can be produced by using Feynman gate. The architecture of conventional Reversible Barrel shifter is shown in fig.1

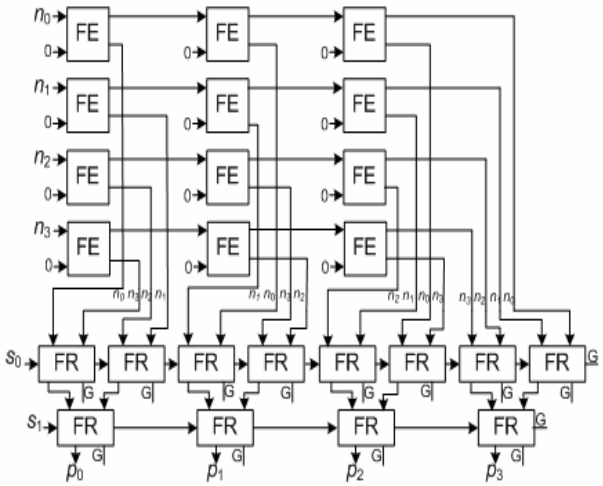

Fig.1. Conventional architecture of Reversible Barrel Shifter

The number garbage output is depends on the number of multiplexers as (2:1) MUX is used in reversible barrel shifter. 2x1 MUX is modeled by using Fredkin Gate which as 2 Garbage outputs for each MUX.

A. Proposed (n, k) Reversible Barrel Shifter: Algorithm

Algorithm Shift/Rotate operation of an (n, k) barrel shifter is used in the proposed design

Input: Data Input Set *I* (i_o, i_1 … i_{n-1}), n = total number of data input bit.

Control input Set S (s_0, s_1,s_k), k = $\log_2$ (n).

Output: Desired shift/rotate output set O(o_1, o_2,o_i).

Begin
Step 1: for k is 0 to $\log_2$ (n)
Step 2: do if s_k = 1
Step 3: then left shift /rotate *I* 2k times
Step 4: else *I* remains same
end.

The proposed design circuit is depicted in Fig.2.

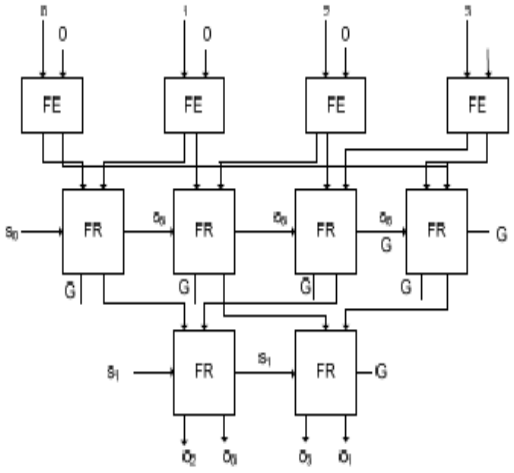

Fig.2. Design with minimum number of gates.

Each stage of the Fredkin gate shifts the input according to the control value of Sk. The proposed model with minimum number of reversible gates.

B. Implementation

The reversible barrel shifter is designed in VERILOG HDL and implemented in XILINX ISE. RTL schematic and chip level module are depicted in fig.3 and fig.4 respectively. Table I compares the reversible barrel shifter delay with existing design at different inputs.

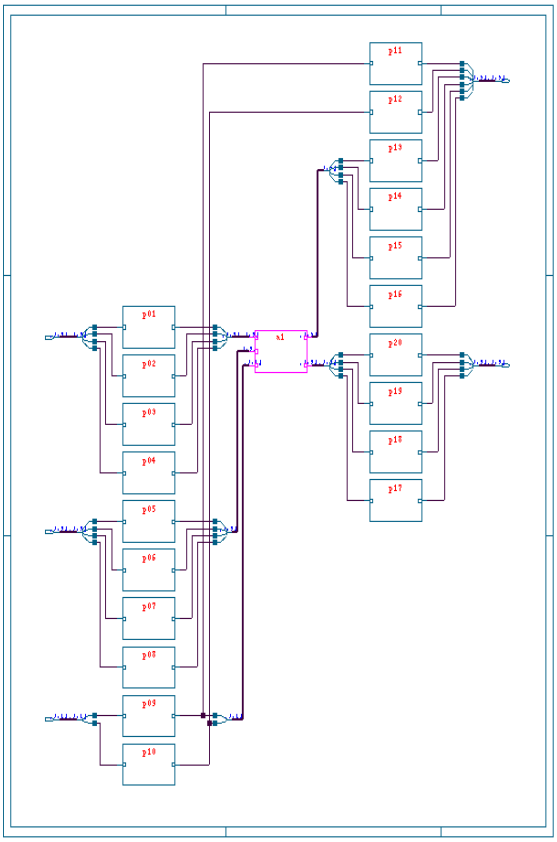

Fig.3. RTL Schematic of Reversible Barrel Shifter

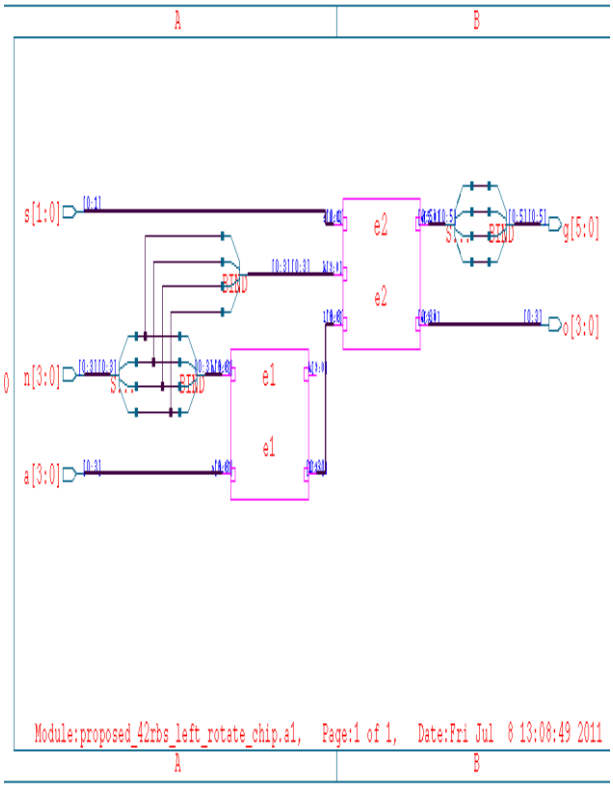

Fig.4. Chip level module design

Table I. Comparative delay of reversible barrel shifter

Reversible Barrel shifter	DELAY (ns)	
	Existing design	Proposed design
(4, 2)	10	6
(8, 3)	35	14
(16, 4)	135	28

III. . RESULTS AND COMPARATIVE ANALYSIS

The conventional and novel design is simulated in XILINX ISE 12.4 simulator and the output wave forms for the proposed (4, 2) Reversible Barrel shifter for left rotate, right rotate, left shift, right shift is shown from fig.5 to fig.8 and the corresponding values are tabulated from Table II to Table V.

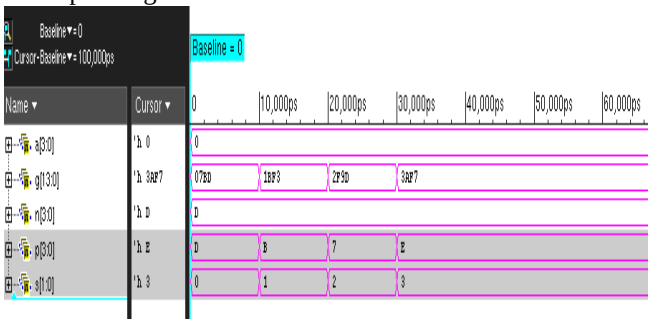

Fig.5.Waveform of (4, 2) reversible barrel shifter for left rotate

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Table II. (4, 2) reversible barrel shifter for left rotate

Input $n_3 \ldots n_0$	Select Line $s_1 s_0$	Output $p_3 \ldots p_0$	Garbage Outputs $g_{13} \ldots g_0$
1101	00	1101	00011110111101
1101	01	1011	01101111110011
1101	10	0111	10111110011101
1101	11	1110	11101011110111

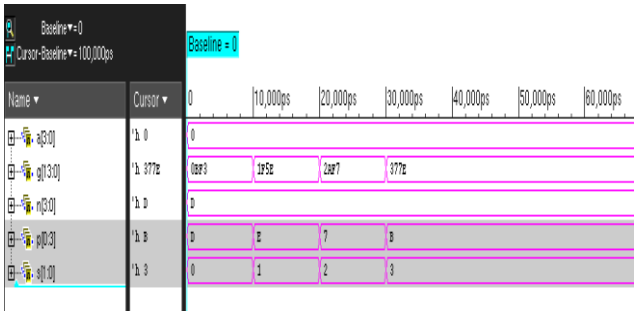

Fig.6.Waveform of (4, 2) reversible barrel shifter for right rotate

Table III. (4, 2) reversible barrel shifter for right rotate

Input $n_3 \ldots n_0$	Select Line $s_1 s_0$	Output $p_3 \ldots p_0$	Garbage Outputs $g_{13} \ldots g_0$
1101	00	1101	00101111110011
1101	01	1110	01111101011110
1101	10	0111	10101011110111
1101	11	1011	11011101111110

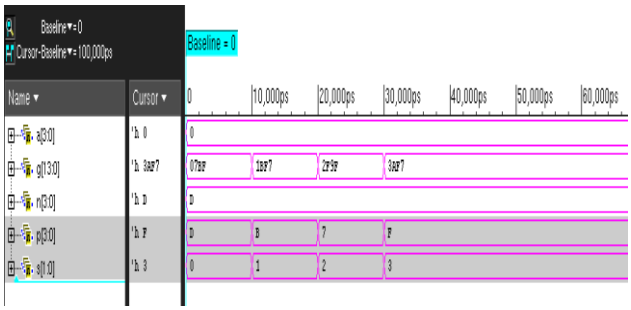

Fig.7. Waveform of (4, 2) reversible barrel shifter for left shift

Table IV. (4, 2) reversible barrel shifter for left shift

Input $n_3 \ldots n_0$	Select Line $s_1 s_0$	Output $p_3 \ldots p_0$	Garbage Outputs $g_{13} \ldots g_0$
1101	00	1101	00011110111111
1101	01	1011	01101111110111
1101	10	0111	10111110011111
1101	11	1111	11101011110111

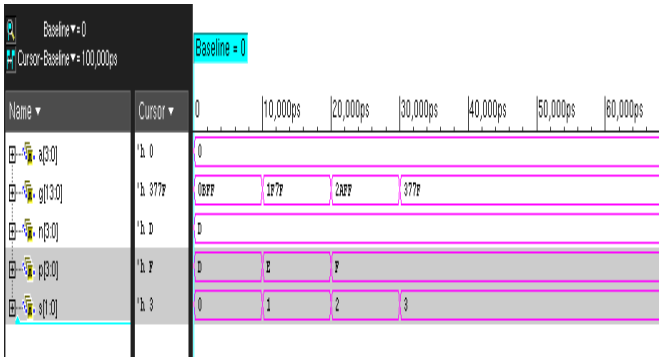

Fig.8. Waveform of (4, 2) reversible barrel shifter for right shift

Table V. (4, 2) reversible barrel shifter for right shift

Input $n_3 \ldots n_0$	Select Line $s_1 s_0$	Output $p_3 \ldots p_0$	Garbage Outputs $g_{13} \ldots g_0$
1101	00	1101	00101111111111
1101	01	1110	01111101111111
1101	10	1111	10101011111111
1101	11	1111	11011101111111

Comparative analysis of (4,2) barrel shifter, (8,3) barrel shifter and (16,4) barrel shifter is shown in Table VI.

Table VI. Comparative Analysis

(n, k)	Criteria	Existing Design	Proposed Design
(4, 2) Barrel shifter	Fredkin	12	6
	Feynman	12	4
	Garbage	14	6
	Delay	10	6
(8,3) Barrel shifter	Fredkin	56	20
	Feynman	56	16
	Garbage	59	19
	Delay	35	14
(16,4) Barrel shifter	Fredkin	240	56
	Feynman	240	48
	Garbage	244	52
	Delay	135	28

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IV. DESIGN ON SOC ENCOUNTER

The novel design is implemented in Cadence physical design using SoC encounter tool. The physical design which follows after the circuit design where components of design is converted into the geometrical shapes in the corresponding layers of materials which provides functioning of the components. IC can be design in front-end design using HDL simulation and backend Design. After physical design the layers of materials information can be send to wafer fabrication house where the manufacturing of process can be done. The tool is used for backend design where the circuit or gates of the design can be floor planned, place and route, power and clock distributions. Steps involved in SOC encounter design are presented

Step1: It is to import design, after importing the configuration file has the information about I/O pads, power pads

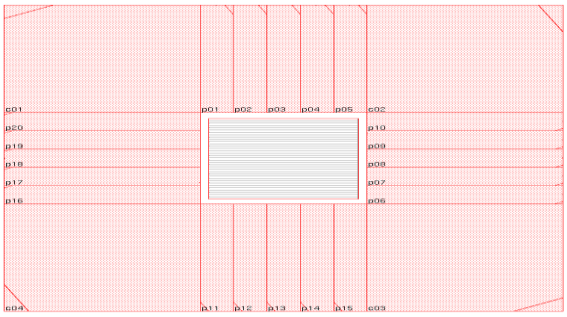

Fig.9. Import design

Step2: Generates Floor plan where IO pads can be placed around the boundary

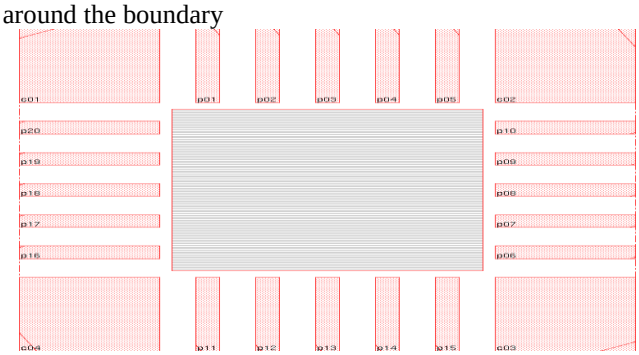

Fig.10.Floor plan Report

Step3: Generates power plan, which includes power rings and power strips.

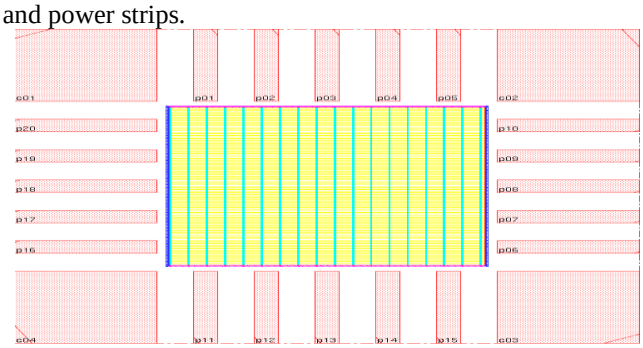

Fig.11. Power plan Report

Step4: Performing timing optimization on placed design before the clock tree is built. Where our design is placed in the selected area

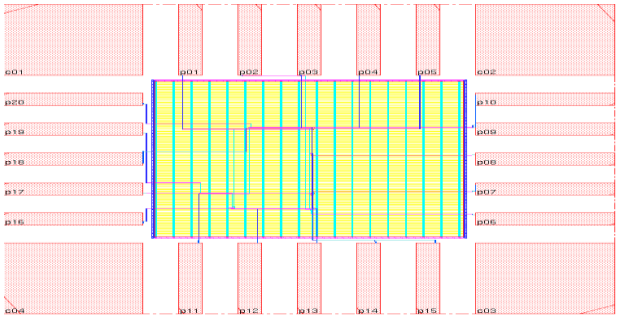

Fig.12. IOP1 Report

Step5: In this mode, while running useful skew and have already detail routed the clock, the EDI system (Encounter Digital Implementation) software performs ECO routing using the nanoroute router.

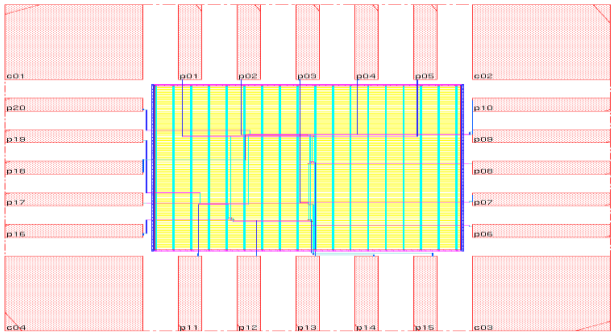

Fig. 13.IOP2 Report

Step6: Power Route where the VDD and GND stripes are routes to the design

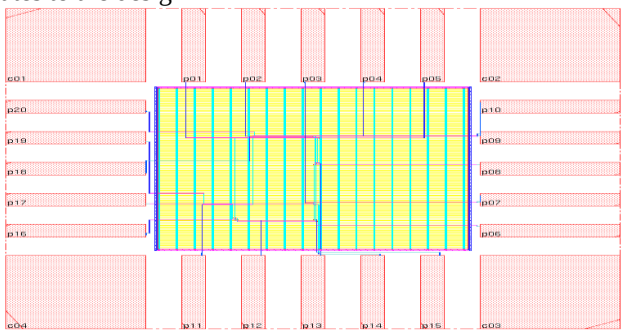

Fig.14. Power Route Report

Step7: Routing the components which are placed are routed through different metal layers

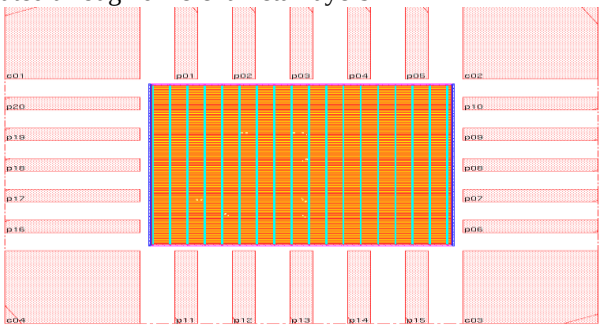

Fig.15. Routing Report

Step8: Generate GDSII (Graphical Data Storage Information Interchange) which is used to design IC by manufacturing Process

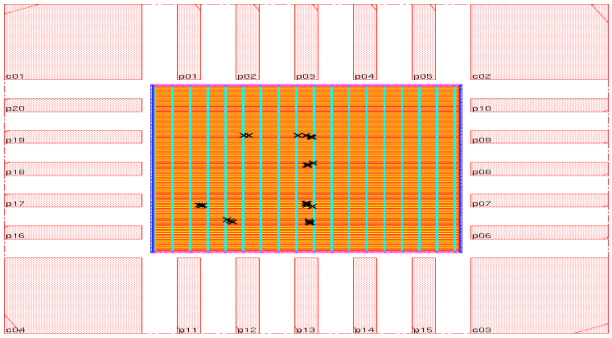

Fig.16. GDSII Report

V. CONCLUSION

A reversible logic is used to retrieve the data from its outputs. A proposed reversible barrel shifter is designed with minimum number of garbage outputs and reduced delay. A novel Barrel shifter was designed in which it occupies less area with less delay. The proposed reversible barrel shifter was designed in VERILOG HDL and is simulated in XILINX ISE 12.4 simulator and chip level design was implemented in SoC encounter. This design benefits with minimum delay and efficient area utilization.

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Dr. P.A.Harsha Vardhini, professor in the Department of Electronics and Communication, Vignan Institute of Technology and Science, Deshmukhi has 18 years of teaching experience. She pursued her Ph.D in VLSI Design from the department of ECE, JNTUH. Her research interests include Low Power Mixed Signal VLSI Design, FPGA architectures, IoT Embedded Applications & Wireless Communication. She is an IEEE & WIE member and life member of IEI, ISOI, IAENG, IAOE. She has more than 75 publications in various journals and conferences at national and International level including SCI, SCOPUS, IEEE, Springer, Elsevier and UGC.